Usage of SCOC3 ASIC + BSW in Science Missions

(or why SCOC3 + BSW is your next option for computer design)

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Contents

Introduction

Activity:

- ESA TRP Contract 4000104797
- 350 K activity + CCN-1 (45K).
- 18 months activity
- Developed by DELTA Consortium (DELTA + TELETEL + M3 Systems)

Goal:

- A good processor ASIC is nothing without good SW
- Develop boot and drivers for SCOC3 ASIC on top of Edisoft RTEMS 4.8 (qualified) according to ESA ECSS standards
- Put at disposition of ESA Community

PART 1: SCOC3 ASIC + BSW

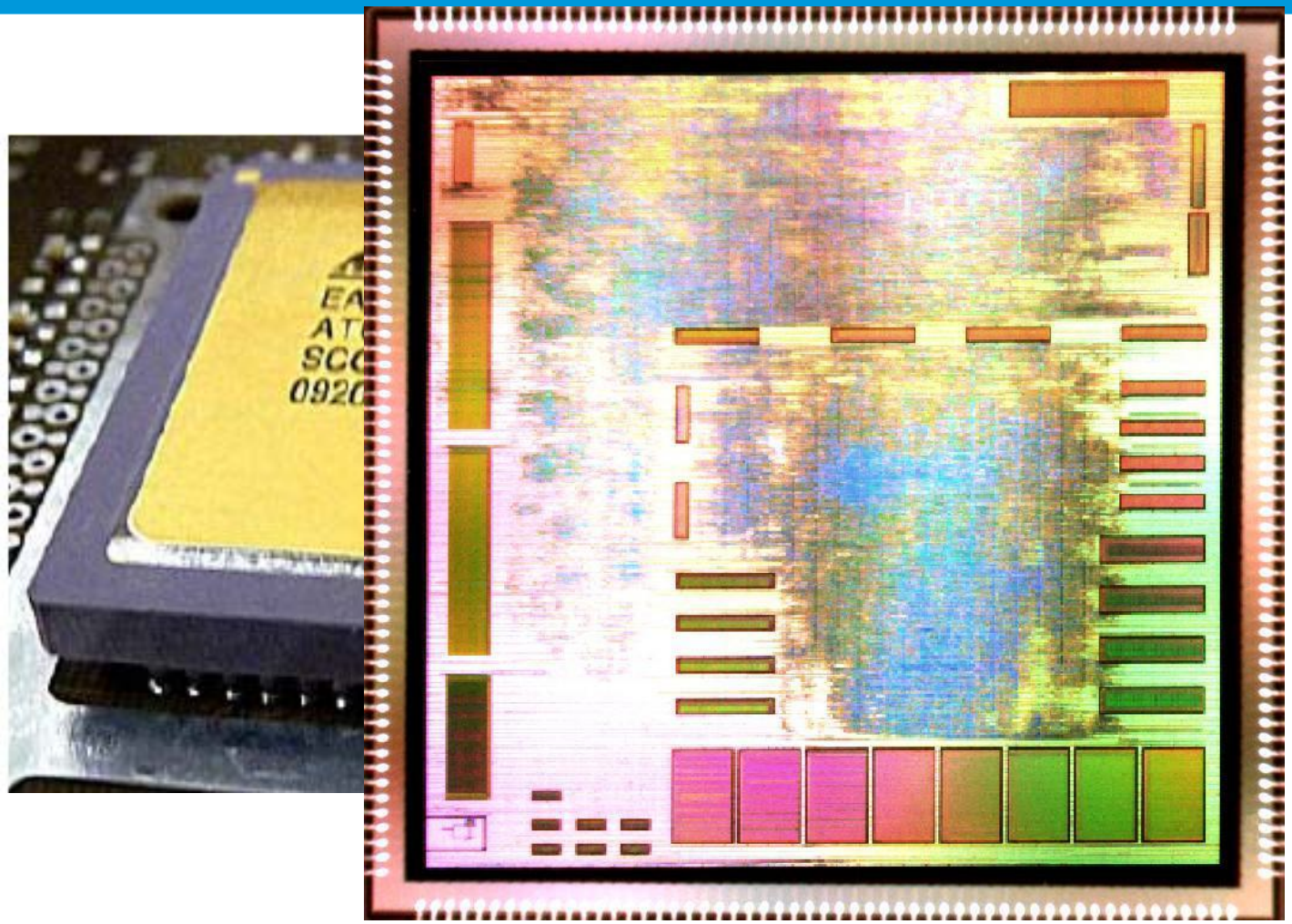
SCOC3 ASIC: HW features

- Developed by Astrium with ESA and CNES funding
  - Used in OSCAR (Astrium Observation and Telecomm On-Board Computer)
  - Flights in SPOT6 since 2012/09/09
  - Selected for SEOSAT, SPOT7, KRS, Sentinel 5, etc.

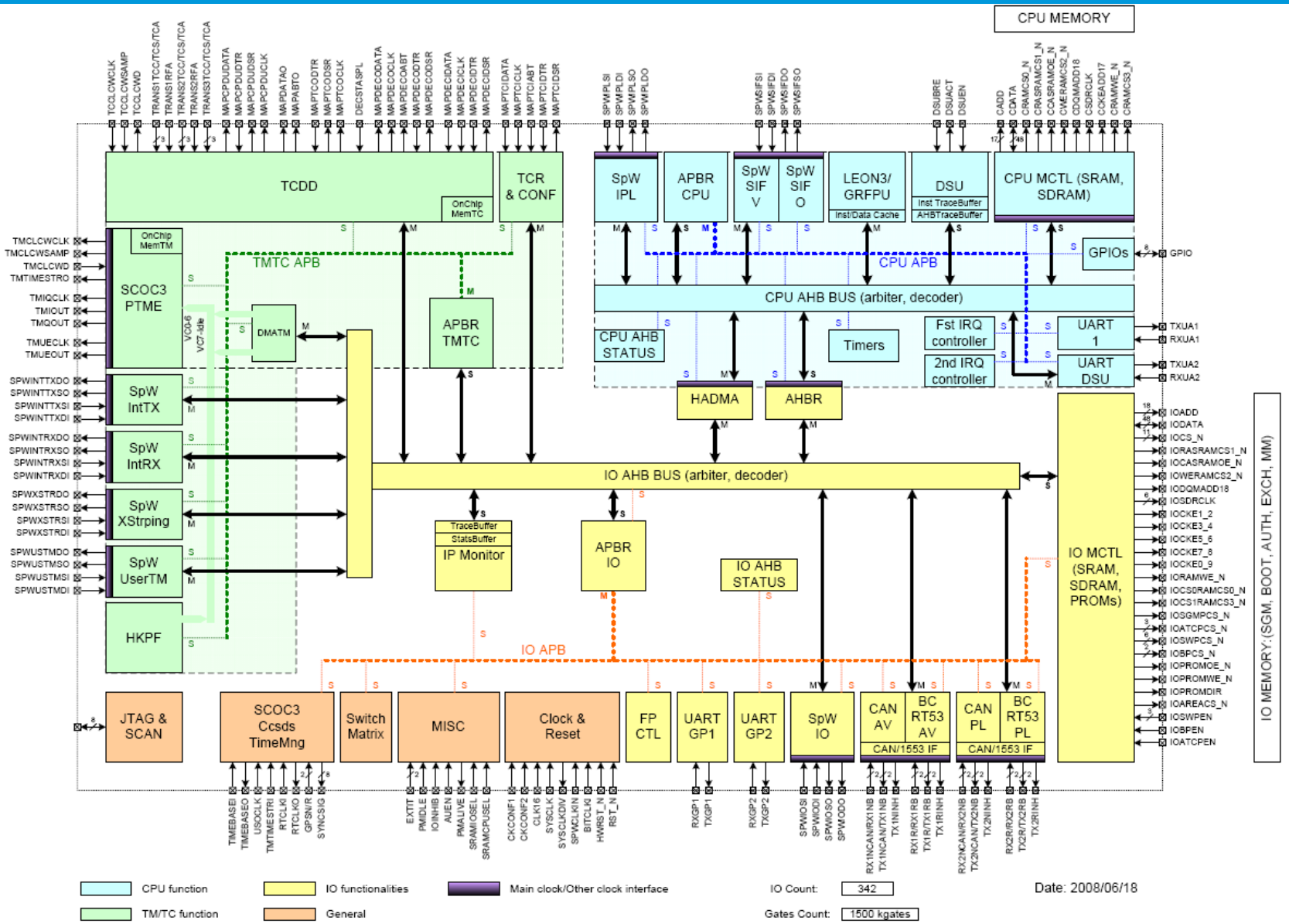
- SCOC3 is a standard product, commercially available to all users:
  - http://www.scoc3.com

- SCOC 3 is: LEON3-FT plus comm IPs (1553 x 2, CAN x 2, SPW x 7) plus CCSDS TM/TC
  - Up to 80 Mhz (60 MIPS)
  - Compatible with SDRAM and SRAM
  - 100 krad total dose. SEU < 10-5 per day (for LET > 30 MeV)
  - Latchup free (LET up to 80 MeV)
- IPs in SCOC3:
  - Astrium IPs: BCRT53 (x2), HDMA, TCDD, STME, MAPTCR, IPMON, etc.
  - Gaisler IPs: Leon3-FT, GRFPU, GRGPIO, IRQMP, ICTL2, AHB, APB, DSU, etc.
  - ESA IPs: SpW-RMAP (x7), CAN (x2), SCTM

SCOC3 ASIC: HW features (2)



SCOC3 ASIC: HW features (3)



SCOC3 ASIC:
STARKIT Development Board

- Developed by Astrium with CNES funding
  - Implements the SCOC3 design in a FPGA
  - Up to 32 MHz (foreseen to increase to 64 MHz)
- Available right now. Competitive cost (consult Astrium)
- http://www.astrium.eads.net/media/document/astrium_pdh11_mdef.pdf

SCOC3 Basic Software (BSW)

- ESA TRP Contract 4000104797
- Developed by DELTA Consortium (DELTA + TELETEL + M3 Systems)

Objectives:

- Develop boot and drivers for SCOC3 ASIC on top of Edisoft RTEMS 4.8 (qualified) according to ESA ECSS standards

- Development cycle:
  - From Technical Specification to Validation in Breadboard (STARKIT)
  - Code design (metrics) and unit coverage according to CAT-B criteria (100% statements, 100% branch)
  - Note however no official qualification: according to ESA CAT-B standard qualification shall be done in the representative HW (not only the processor, but the full computer)

SCOC3 Basic Software (BSW) (2)

SW Features: boot library + drivers

- Boot library:
  - Contains the building blocks for writing a boot SW (autotest functions, etc.),
  - Building blocks to be combined and adapted to your specific computer design
  - => Note: a final, complete boot cannot developed, as the architecture of the final computer (redundancy or not, etc.) is not know
- Drivers: Edisoft RTEMS 4.8 based drivers for:
  - SpW, 1553, CAN, UART
  - Interrupts, timers
  - SWMA, IPMON, HDMA, WD, GPIO
  - TMTC (basic)

SCOC3 Basic Software (BSW) (3)

SW Drivers Architecture:

- Usual libbsp – libchip – libcpu approach
  - libchip / libcpu DO NOT use RTEMS services
  - libbsp USES RTEMS services
  - no usage of ioctl() paradigm but dedicated config functions
    - (ioctl approach for configuring avoids parameter checking by compiler)
  - All synchronization is managed internally in the libbsp services:
    - E.g.: 2 tasks can send simultaneously on the CAN Bus (no FIFO server of petitions needed at ASW level)
    - However this create contention (one of the task will wait until the other has send the message)
    - Safety oriented (not performance oriented)
- SW is designed to run on top of Edisoft RTEMS (ESA preferred version)
  - Other RTEMS versions are not (and will be not) tested

SCOC3 Basic Software (BSW) (4)

Code statistics:

- LOC 12800
- UT: 100% statement, 100% branch coverage achieved

Validation test bench:

- About 80 test cases
- Types of tests:
    - Loopback in 1553, SpW, CAN
    - External (with external test EGSE: 1553, CAN, SpW – at several speeds)
    - Errors injection
    - Performance
- Combined IFs (e.g.: 1553 + CAN + SpW)

- Processor always run at 32MHz (limitation: STARKIT maximum speed at today)
- Validation Test Bench available, needs HW license (iSAFT Test Runner).
    - Contact DELTA and TELETEL

SCOC3 Basic Software (BSW) (docs)

- The standards ECSS required docs are available
  - From SRR to CDR (i.e. we stop at CDR, validation wrt TS)
- Except:
  - PA report, RAMS (HSIA) documentation not available
  - Qualification docs (QTP, QTR) not available

File	DL Item	Name
TS	SDP	Software Development Plan
	SRS	Software Requirements Specification
	ICD	Software Interface Control Document
DDF	SDD	Software Design Document Specification
	SReID	Software Release Document
	SUM	Software User Manual
DJF	SValP	Software Validation Plan w.r.t. TS
	STR-TS	Software Validation Report w.r.t TS
	STP-U	Software Unit Test Plan
	STR-U	Software Unit Test Report
	STP-I	Software Integration Test Plan
	STR-I	Software Integration Test Report
	SPR/ NCR	Software Problems Reports and Non-conformance Reports
SoC		ECSS E-ST-40C and ECSS Q-ST-80C Statement of Compliance

SCOC3 Basic Software (BSW) Roadmap to Qualification (as CAT-B SW)

How to re-use the SCOC3 BSW in your Project:

Proposal for CAT-B SW:

- Write a SW Reuse Plan:
  - Detailing why the BSW is selected
  - How do you plan to achieve the SW qualification in real target
  - Which SW modifications shall be done (if any) and how will be tested
- Add to your SSS (System SW Specification) high level requirements for the low level SW
- Write RAMS doc (HW/SW Interaction Analysis - HSIA)
- Write a Qualification Test Specification
  - Run the Qualification test campaign on your computer (possibly an EM or QM model)
  - Write the Qualification test report
- Write a overall SW Verification Report
- Hold a QR/AR as needed

SCOC3 Basic Software (BSW) (License)

IPR of BSW is ESA, that has decided to provide the BSW as...

- ESA Community License, Type 3, permissive
- Companies from ESA Member States can reuse / adapt the SCOC3 BSW for projects developed for ESA Member States customers
    - Usage outside space domain is possible, but always inside ESA Member States
    - But not military usage!
- You are encouraged to provide improvements, feedback on bugs...
    - But you are not enforced by the License to do so (no further redistribution of your SW is required)

- SW and documentation will be provided in a dedicated Web Site. Register (free) will be needed. License shall be distributed with the SW.

- Reminder: Usage outside ESA Member States requires specific “ESA Authorization Transfer Board”)

SCOC3 HW & SW: Warnings

HW limitations:

- SCOC3 has 2 x 1553 and 2 x CAN. But pins are shared. Usage combinations are:
  - (2 x 1553) **OR** (2 x CAN) **OR** (1 x 1553 plus 1 x CAN)
  - (i.e. not possible to use 2 x 1553 + 2 x CAN simultaneously)
  - Changing it needs processor reboot
- CAN HW limitation (due to CAN IP limitations)
  - CAN buffer is only 1 CAN message. Multi-master scenarios can be difficult to manage
- SpW limitations
  - Most of SpW ports are attached to the IO bus. Transferring data from CPU mem to SPW core mem takes time
- UART limitations
  - Run at speed higher than 57600 bps can occasionally corrupt the communication

SCOC3 HW & SW: Warnings (2)

BSW Limitations:

- Basic TM/TC SW Driver. The provided TM/TC driver is very basic and does not provide encryption, advanced options, dual TM/TC configurations, etc.
- SpW Data and RMAP supported. Mixed mode not supported.

Development environment:

- Astrium can provide DSUMON (similar to GRMON but simpler). Contact Astrium for details
- Astrium provides a SCOC3 simulator (similar functionalities to tsim) but more expensive

We remark again:

- SW **is validated** against the Technical Specification
- SW **is not qualified** against a SW System Spec. This requires your particular spec and your particular computer

SCOC3 BSW: Remaining activities

- SCOC3 BSW validation has been performed with STARKIT
  - STARKIT runs at 32 MHz max at today
  - SCOC3 implemented in a FPGA
- **Task 5 of the TRP**: re-execute a subset of the Test Validation campaign in ESTEC premises
  - To be run in KERTEL board
    - Implements the SCOC3 ASIC
    - Runs at 32 Mhz, 64 Mhz, 80 Mhz
  - Choose a sub-set of test cases from the Validation Test Spec
  - Execute at different processor speeds
  - Activity supported by DELTA Consortium
  - Foreseen first half of 2014

PART 2: USAGE SCENARIOS

SCOC3: Usage Scenarios (exercise)

ESA OBC “State of the art design” at today:

- ERC32/TSC695 + FPGAs or ASIC (with comm interfaces, glue logic)
  - ASIC memory mapped into processor memory
- LEON2/AT697 + FPGAs + ASIC (with comm interfaces, glue logic)
  - Linked with a PCI bus

Examples:

- VEGA OBC LN1 SW: Example of simple central computer
  - 1 ERC32 at 40 MHz
  - 1 complex communication ASIC (COCOS)

- Exomars CTPU: Entry Descent Module central computer, example of complex computer.
  - 1 LEON2 at 64 MHz, Serial, 1553, Can, SpW IFs.
  - 1 FPGA with several IPs: 1553, CAN, SPW
  - 1 FPGA with Mass Memory logic

- Exomars Radar: Example of instrument computer.
  - 1 LEON2 at 80 MHz
  - 1 FPGA with CAN IP, radar numerical algorithms

SCOC3: Usage Scenarios (warning)

WARNING:

FIGURES ON NEXT SLIDES TO BE TAKEN WITH CARE!

ONLY ROUGH ESTIMATIONS!!!

INTENTION IS JUST TO PROVIDE ONLY QUALITATIVE INDICATIONS

Costs

- Costs that cannot be avoided:
  - Implementation of mission dependent algorithms
  - SW specific logic (e.g. EEPROM, flash drivers)
  - HW specific logic (e.g. radar management and filtering)

- Costs that can be avoided:
  - Re-design of boot basic functions (e.g. RAM, cache, EDAC tests)
  - Re-design of glue logic for “communication IPs”
  - Re-design of SW drivers for “communication IPs”
  - Testing of previous!

- **For non recurrent missions, costs are driven by engineering hours, more than by HW costs!!!**

Estimated effort: VEGA OBC LN1 SW

Current design:

- **HW Cost:**
  - ERC32 (TBC cost), 1 x COCOS ASIC (1553 comms, OBT)
  - HW Design cost: COCOS reused
- **SW Design cost** (rough estimation as CAT-A/B):
  - boot (1000 loc at CDR) => 2000 h
  - drivers (500 loc at CDR) => 1000 h... (applying 0.5 loc/hour CAT-A/B)

Alternative design with SCOC3 + BSW:

- **HW Cost:**
  - SCOC3 (cost TBC Astrium). No specific ASIC needed
  - NOTE: COCOS ASIC provides frame management 1553 capacities. These are also present on SCOC3 1553 IP but is TBD if real time performances are similar
- **SW Design Cost:**
  - boot (provided by SCOC3 BSW) => needs adaptation / integration (20% of 2000 h)
  - drivers (provided by SCOC3 BSW) => needs adaptation / integration (20 % of 1000 h)
  - Qualification in EM OBC computer (1000h. 1 month x 5 persons)

Remarks:

- Reduction SW engineering hours (3000h to 1600h)
- Reduction HW engineering hours (N/A: 0% if COCOS reused. Very high if new ASIC)
- **HOWEVER recurrent COST is a KEY FACTOR for Launchers**
- HW cost: SCOC3 vs (ERC32 + COCOS ASIC)
- **To be further analyzed: difference in board complexity (mass, power, components...)**

Estimated effort: Exomars EDM CTPU

Current design:

- **HW Cost:**
  - LEON2 AT-697F (≈20k), 1 x FPGA RTAX-2000 for comms (≈14.5k), 1 X FPGA RTAX-2000 for mass memory, 1 x TMTC ASIC (cost TBC)
  - HW Design cost: let's name 'HW_design_hours'
- **SW Design cost** (rough estimation as CAT-B):
  - boot (6500 loc at CDR) => 6500 h
  - drivers (7800 loc at CDR) => 7800 h... (applying 1 LOC/hour CAT-B)

Alternative design with SCOC3 + BSW:

- **HW Cost:**
  - SCOC3 , 1 FPGA RTAX-2000 (for mass memory);
  - Saved HW cost: comm IP FPGA not needed, TMTC ASIC not needed
  - HW Design cost: (TBC) of 'HW_design_hours' (No FPGA comms, no TMTC ASIC)
- **SW Design Cost:**
  - boot (provided by SCOC3 BSW) => needs adaptation / integration (50% of 6500 h)
  - drivers (provided by SCOC3 BSW) => needs adaptation / integration + specific drivers (mass memory, SGM, PCI... 2045 loc) (40 % of 7800 h)
  - Qualification in EM CTPU computer (2000h. 2 month x 5 persons)

Remarks:

- Reduction SW engineering hours (14300 h to 8370h)
- Significant reduction HW engineering hours (to be quantified)

Estimated effort: Exomars EDM Radar

Current design:

- **HW Cost:**
  - LEON2 AT-697F (≈20k), 1 x FPGA RTAX-4000 (≈45k) (CanOPen HW IP and radar algos)
  - HW Design cost: 'HW_design_hours' (TBC)
- **SW Design Cost** (rough estimation). CAT-B:
  - boot + drivers (4000 loc at CDR) => 4000 h (applying 1 loc/hour CAT-B)

Alternative design with SCOC3 + BSW:

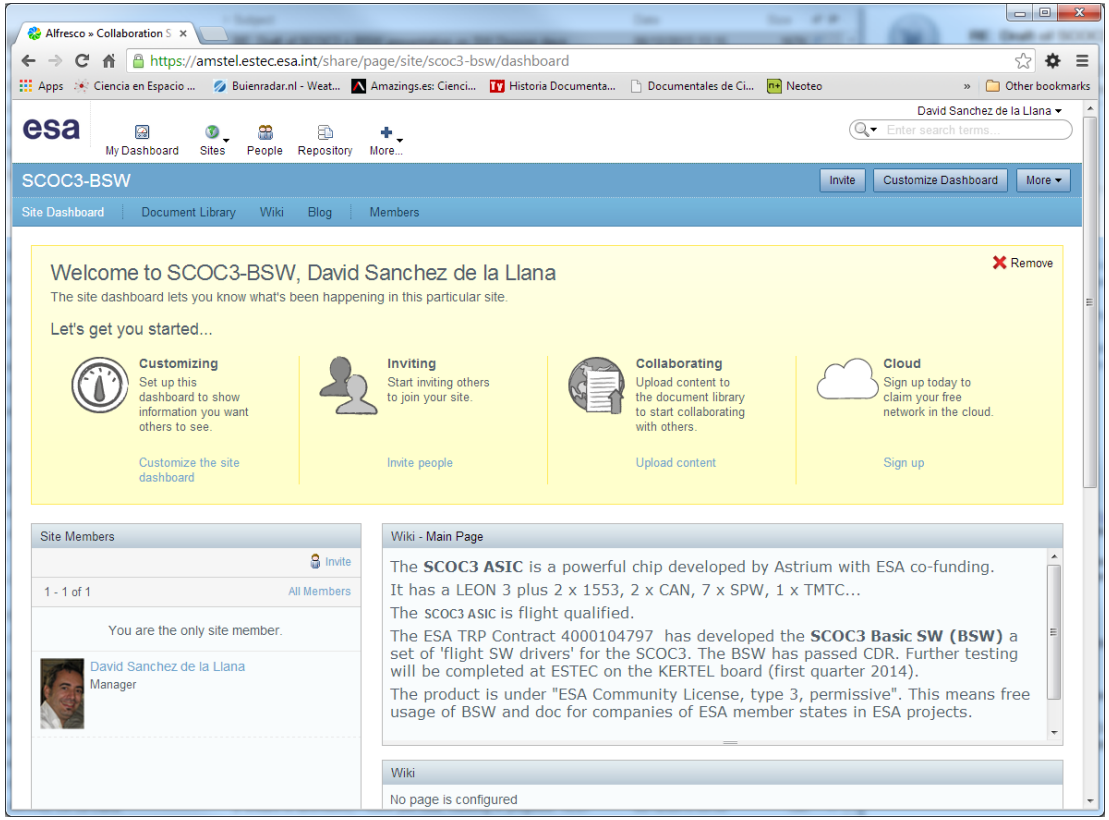
- **HW Cost:**
  - SCOC3
  - 1 FPGA RTAX-4000 (if only for radar algos, could be RTAX-2000? => 14.5k)
  - HW Design cost: TBC% of 'HW_design_hours' (as radar algos shall be implemented)
- **SW Design Cost:**
  - boot (provided) => needs adaptation / integration (10% of 4000h)
  - drivers (provided) => needs adaptation / integration + pci driver (30% of 4000h)
  - Qualification in EM CTPU computer (1000h. 1 month x 5 persons)
  - But CANOpen Stack shall be implemented in SW (TBC loc)

Remarks:

- Reduction SW engineering hours (4000h to 2600h) **(TBC but CanOpen stack to be included)**
- Significant reduction HW engineering hours

SCOC3 BSW Distribution

- Documentation and SW available to registered users in Alfresco web site: https://amstel.estec.esa.int/share/page/
- Contact us for getting an user



Conclusions

- SCOC3 ASIC is a powerful chip, already space qualified, flight proven
- SCOC3 ASIC is a standard product, commercially available to all users
- SCOC3 BSW is a validated SW building block
- The combination SCOC3 ASIC + BSW can save engineering hours, in particular for complex computers, with several buses
- Depending on the interest of the users (usage on ESA Projects) ESA can support improvements of the product, further maintenance, etc.

- Further information:
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Questions

Thank you for your attention!!!

QUESTIONS?