New ECSS standards for ASIC, FPGA and IP Core engineering and product quality assurance

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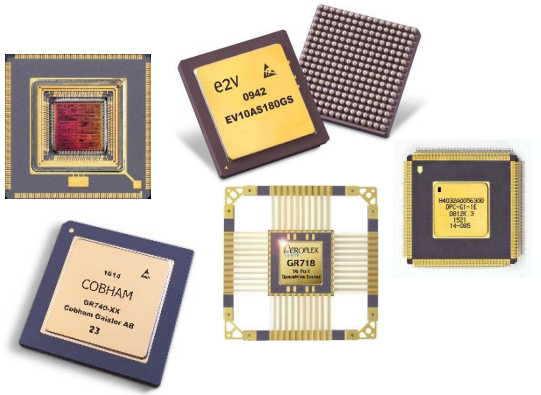
ESA ESTEC TEC-E
Ref.: ESA-TECE-HO-2022-003286
ADCSS 2022 25/10/2022

Contents

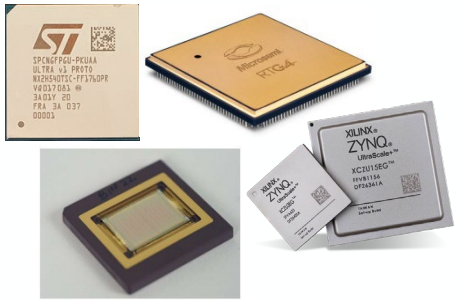
1. Scope of the new ECSS standards for ASIC/FPGA/IP Cores
2. History of ASIC/FPGA ECSS standards
3. How did the WG work, starting points
4. Main FORMAT changes and goals in new standards
5. Table of contents of new standards, the annexes
6. Engineering and Product Assurance requirements: to be applied in parallel
7. Focus on **E-ST-20-40 standard:**
    - **main differences** vs. **old** ECSS-Q-60-02C engineering chapter
    - Terminology: term definitions, conventions, equivalence between engineering and management std terms
    - generic development flow and variations, phases and reviews name differences vs old standard
    - DEVICE criticality pre-tailoring
    - Distribution of requirements according to DEVICE type
8. How to submit “change requests” during Public Review (deadline Nov 18th 2022)

ECSS standards for ASIC, FPGA and IP Cores

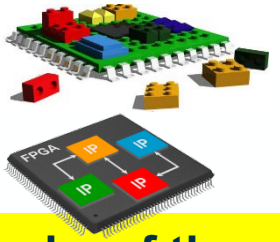
Applicable in **R&D activities** and **projects**, setting high level requirements for the successful **engineering** and **product assurance** of the development by the supplier, and the supervision By the customer of:



- [**ASICs**] Application Specific Integrated Circuits
  - Sometimes ASICs are developed to be Standard Products ("**ASSP**"), sold and used by different companies
  - Can be digital, mixed-signal or analog
  - Microprocessors, µC, DSPs, GPUs are a special "general purpose" group of ASICs



- [**FPGAs**] Field Programmable Gate Arrays
  - Customer "programmed" devices. (e.g. designs programmed onto Microchip, NanoXplore or Xilinx FPGAs).
  - "blank" devices (e.g. European BRAVE FPGA family by NanoXplore).
  - Can embed "processing" cores (will use SW to operate!)



- [**IP Cores**] Intellectual Property Cores
  - "soft" models of integrated circuits,
  - reused as "building blocks" to develop ASICs and FPGAs faster

All ESA missions use tens, sometimes hundreds, of these complex microchips and IPs

Timeline: ECSS ST and HB for ASIC and FPGA

2000 ECSS-Q-ST-60-02C **WG kick-off** (led by TESAT(DE))

2007 ECSS-Q-ST-60-02C ASIC and FPGA development

SUPERSEDED in Q1 2023 by 2 new standards…

2012 ECSS-Q-HB-60-02C **WG kick-off** (led by ESA, based on a draft created by TIMA(FR) under ESA contract)

2016 ECSS-Q-**HB**-60-02C Techniques for Radiation Effects Mitigation in ASICs and FPGAs

2019 ECSS-E-ST-20-40 & Q-60-02C Rev.1 **WG kick-off** (led by ESA)

Q1 2023 **ECSS-E-ST-20-40 ASIC, FPGA and IP Core engineering**

ECSS-Q-ST-60-02C Rev.1 ASIC, FPGA and IP Core product assurance

Timeline: NEW ECSS Stds for ASIC, FPGA and IP Core

Aug 2017 - preliminary list of 28 Change Requests proposed by ESA Microelectronics Section

Apr 2018 - 42 change requests proposed by 11 ASIC/FPGA experts from European companies and institutes (including TAS, ADS, RUAG, Arquimea, Cobham Gaisler, TESAT, IMEC, CNES) at a meeting at ESTEC

Oct 2019 - New ECSS-E-ST-20-40 & Q-60-02C Rev.1 WG kick-off : 10 members, 37 experts (TAS, ADS, OHB, GMV, TESAT, Cobham Gaisler, BSC, Ariane, RAL, CNES, DLR and ESA)

Aug 2022 - ECSS-E-ST-20-40 & Q-60-02C Rev.1 in Public Review between Aug 23rd – ~~Oct~~ **Nov 18th 2022**

Q1 2023 - Expected publication of new standards after WG processes all requests for changes

- ECSS-E-ST-20-40 ASIC, FPGA and IP Core engineering
- ECSS-Q-ST-60-02C Rev.1 ASIC, FPGA and IP Core product assurance

New standards: WG modus operandi

ECSS-E-ST-20-40 - engineering

starting points : All chapters and requirements of old ECSS-Q-ST-60-02C chapter 5 (ASIC and FPGA engineering), all requests for changes gathered from industry and ESA experts, reviewed item by item, improving/adding/superseding many requirements, having as reference a generic development flow that admits variations, different types of DEVICES, and 2 main criticality levels.

ECSS-Q-ST-60-02C Rev.1 – product assurance

A splinter sub-WG created the completely new draft, then reviewed with entire WG reviewed. Took inspiration from Q-ST-80 (SW Product Assurance), but adapted to DEVICE (IC and IP) developments, as PA complement to the new E-ST-20-40. Seeking compliance to ECSS-Q/M branches (Q-10, Q-20, Q-30, M-40, M-10).

The “old” ECSS-Q-ST-60-02C had engineering and PA

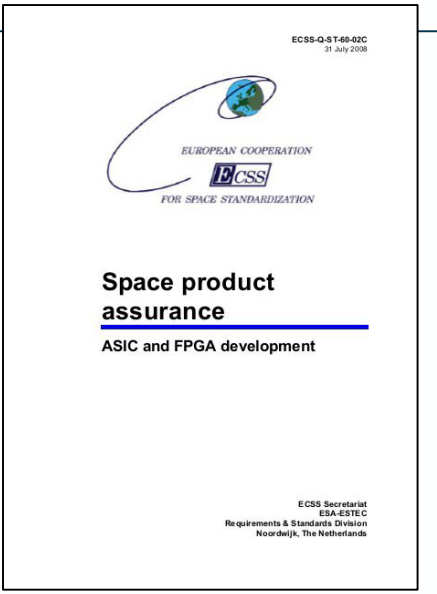


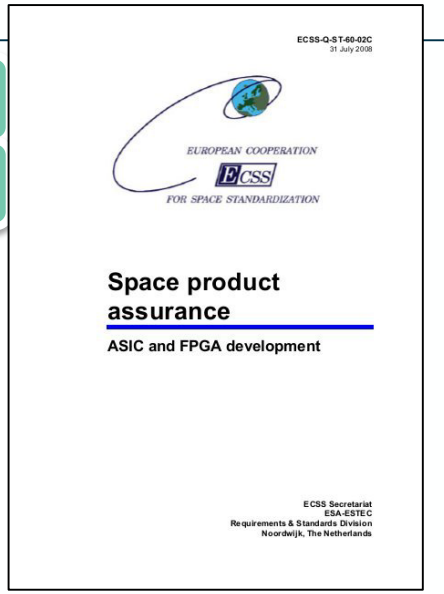
Table of contents

85% !!

The “old” ECSS-Q-ST-60-02C had engineering and PA

15% is product / quality assurance , dependability

But with simple references to other Q-branch stds – New Q-60-02C Rev.1 has expanded such requirements for clarity and coherence with Q-branch ECSSes



New standards: main FORMAT changes and goals

- **Separation** of **engineering** (in E-ST-20-40) versus **product assurance** requirements (in Q-ST-60-02C Rev.1)
- **Minimize dispersion** of requirements between main chapters and normative annexes (DRD = Document Requirements Definition). Most requirements are now in DRDs
- **Minimize redundancies** (particularly inside each std, E and Q).
- consistent **terminology** , also wrt new SW ECSS-E-ST-40 std,
- **better** and **new definitions** of terms used in the context of this standard.
- Improve the **quality** and **clarity** of requirements, the figures and tables used, the overall organization of the information

new standards separate engineering and PA requirements

ECSS-E-ST-20-40 (2022)

5 DEVICE engineering
- 5.1 General requirements
- 5.2 DEVICE Definition Phase
- 5.3 DEVICE Architecture Definition Phase
- 5.4 DEVICE Design and Verification Phase
- 5.5 DEVICE Detailed Design Phase
- 5.6 DEVICE Layout Phase
- 5.7 DEVICE Implementation Phase
- 5.8 DEVICE Validation, Acceptance and Maintenance Phase

6 Pre-tailoring according to DEVICE criticality and type

+ 12 Annexes (9 DRDs)

ECSS-Q-ST-60-02C Rev.1 (2022)

5 Product Assurance programme implementation
- 5.1 Organization and responsibility
- 5.2 DEVICE product assurance programme management
- 5.3 Risk management and critical item control
- 5.4 Supplier selection and control
- 5.5 Tools and supporting environment

6 DEVICE Process Assurance
- 6.1 DEVICE development lifecycle
- 6.2 Requirements applicable to all DEVICE engineering processes/phases
- 6.3 Requirements applicable to individual DEVICE engineering processes and activities
- 6.4 Process Assessment and improvement

7 DEVICE product quality assurance
- 7.1 Product quality objectives and metrication
- 7.2 IP Core or DEVICES intended for Reuse

8 DEVICE Configuration Management
- 8.1 DEVICE Configuration Management planning and control
- 8.2 Configuration Management implementation
- 8.3 Configuration Control

9 Tailoring by DEVICE criticality

+ 5 Annexes (3 DRDs)

Separation similar to
ECSS-E-ST-40 SW engineering and ECSS-Q-ST-80 SW PA, compliant to ECSS-Q-ST-10/20/30 Product assurance

E-ST-20-40 Annexes (when "normative", it contains requirements too !)

Annex A (normative) DEVICE **Requirements Specification** (DRS) - DRD

Annex B (normative) DEVICE **Development Plan** (DDP) - DRD

Annex C (normative) DEVICE **Verification Plan** (DVeP) - DRD

Annex D (normative) DEVICE **Validation Plan** (DVaP) - DRD

Annex E (normative) DEVICE **Support and Maintenance Plan** (DSMP) - DRD

Annex F (normative) **Feasibility and Risk Assessment Report** (FRAR) - DRD

Annex G (normative) **Architecture Definition Report** (ADR) - DRD

Annex H (normative) DEVICE **Data Sheet** (DDS) - DRD

Annex I (normative) **Experience Summary Report** (ESR) - DRD

And more…

Annex J (informative) **Generic Development Flow Variations**

Annex K (informative) DEVICE **Development Expected Outputs**

Annex L (informative) **Equivalence of phase and milestone terminology of ECSS-M-ST-10 and ECSS-E-ST-20-40**

Q-ST-60-02C Rev.1 Annexes (if “normative” contain requirements too !)

Annex A (normative) **Product Assurance Plan (DPAP)** - DRD

Annex B (normative) **Product Assurance Report (DPAR)** - DRD

Annex C (normative) **DEVICE Reuse File (DRF) – DRD**

Annex D (informative) **DEVICE Development Expected Outputs**

Annex E (informative) **Traceability from ECSS-Q-ST-60-02C to ECSS-Q-ST-60-02C Rev1**

VCD (Verification Control Document)	ECSS-E-ST-10-02 Annex B
EIDP (End Item Data-Package)	ECSS-Q-ST-20 Annex B
CMP (Configuration Management Plan)	ECSS-M-ST-40 Annex A
CIDL (Configuration Item Data List)	ECSS-M-ST-40 Annex C
ABCL (As-Built Configuration List)	ECSS-M-ST-40 Annex D
SCF (SW Configuration File)	ECSS-M-ST-40 Annex E

the thin line separating engineering from product assurance requirements

There are some requirements overlaps between the E-ST-20-40 and Q-ST-60-02 Rev.1 stds, as the Eng/PA borderline is at times blurry.

Also same or very similar things are called sometimes different names, and sometimes same words can have different meanings in the context of different standards (e.g. "verification", "validation" or "qualified", which needs context words : "ECSS PA qualified" vs. "ESCC qualified" vs. "MIL QML-V qualified"…)

Q-60-02C Rev.1 adheres strictly to other applicable ECSS Q and M standards, using their terminology, while E-ST-20-40 uses terminology that is widely used by ASIC and FPGA engineers – "Annex L" in E-ST-20-40 aims to facilitate the understanding of the equivalence of some phase and milestone terms used in E-20-40 and M-10

Both standards shall be applied, in parallel, and supervised by:
- an ASIC/FPGA/IP engineer (e.g. ESA technical officer or expert) and
- a Product Assurance responsible.

Customer "DEVICE acceptance" as **"fully verified and validated"** (E-20-40) and **"PA qualified"** (Q-60-02C Rev.1)
is subject to successful final reviews as defined in both standards

FOCUS now on

The DEVICE engineering standard

ECSS-E-ST-20- 40

Major differences between ECSS-E-ST-20-40 and old standard engineering chapter – (1/2)

1. **New term definitions** and several old ones improved
2. Many **NOTES** added with more **examples**
3. **Most requirements** are now **“first level” (can be tailored individually).** Only a few “level 2” sub-lists
4. **Tags** indicating the applicability of each requirement to 4 main DEVICE types: **[D-ASIC**, **A-ASIC, FPGA**, **IP]**
5. General Requirements covering:
    - **Tailoring** according to **DEVICE type** and **DEVICE criticality** (a single table in chapter 6 for both)
        - This table can be transformed in a “csv” or “XLSX” file to easily pre-tailor each specific case
    - Clearer DEVICE engineering **“generic development flow”** and introduction of **“flow variations”**
    - All **Phase Reviews** share a **common set of requirements**

Major differences between ECSS-E-ST-20-40 and old standard engineering chapter (2/2)

6. Improved and more **development flow figures** (in fig. 5-1 and figures in Annex J)
7. **New phase** and **review names** – more self explanatory and commonly used in DEVICE engineer community deviating sometimes from typical “system/equipment” milestone or document names as per ECSS-M-ST-10 (new annex L added to explain names equivalence with Management stds)
8. **Additional phase** added between old SRR and old PDR: **“DEVICE Architecture Definition Phase”**
9. New requirements added and some improved or superseded by new ones for:
    I. DEVICES that contain “**processing units**” (which will use SW to operate) to ensure better **HW-SW co-engineering**
    II. **re-use of “IP Cores” and “building-blocks”**
    III. **mixed-signal ASICs / analog IPs**
    IV. **More comprehensive sets of requirements** for DEVICE Requirements Specification, and for Development, Verification and Validation Plans

New standards: terminology

New term definitions:

Building block
Code
Deactivated function
DEVICE
DEVICE database
DEVICE model
FPGA Programming Test
Phase
Processing unit
Production test
Prototype
Software
Synthesis tool
System requirement
Unreachable function
Validation
Verification

Improved term definitions:

Design for test
Design iteration
(DEVICE) development flow
(DEVICE) technology
HDL model
IP Core
Macrocell
Netlist
Redesign

3.4.2 Companies involved in the DEVICE development :

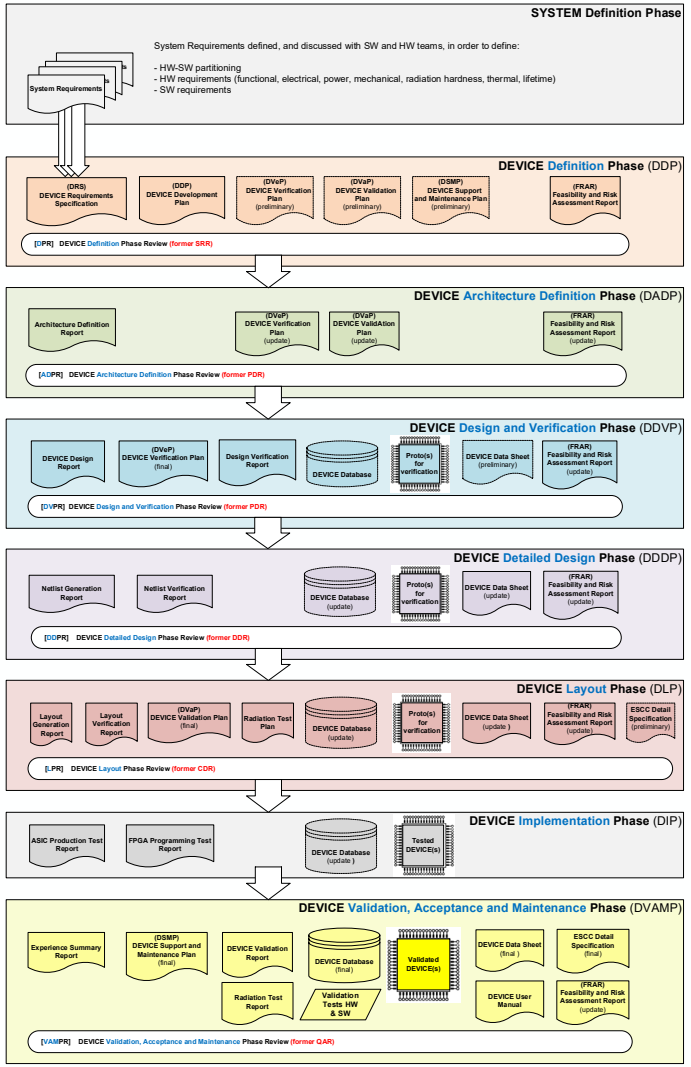
- Customer (ESA)
- Supplier (the company developing the chip or IP)

- FPGA or ASIC technology providers (CAD tools, Design Kits and libraries, IP Cores)
- ASIC manufacturers (masks, wafers, packaging)

Annex L in E-ST-20-40:
Equivalence of phase and milestone terminology of M-ST-10 and E-20-40

New development flow figures

ECSS-E-ST-20-40 (2022)



old ECSS-Q-ST-60-02C (2007)

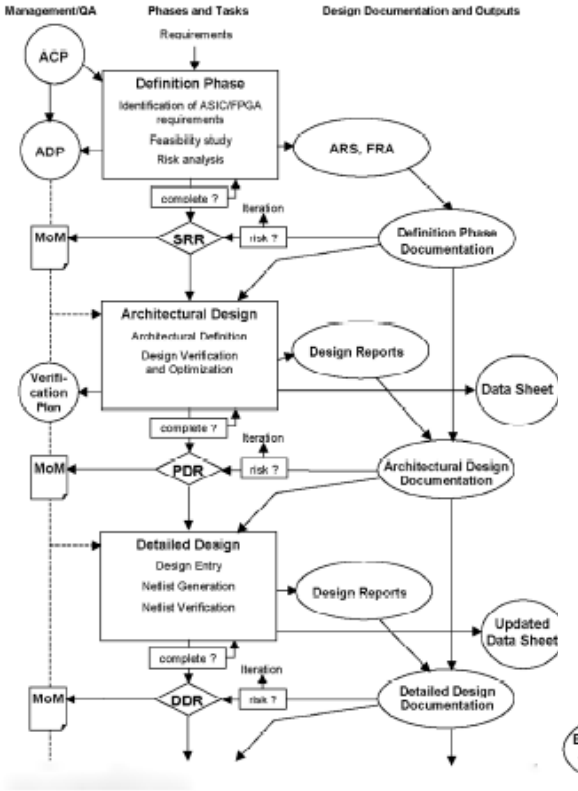


Figure 5-1: Development flow (example)

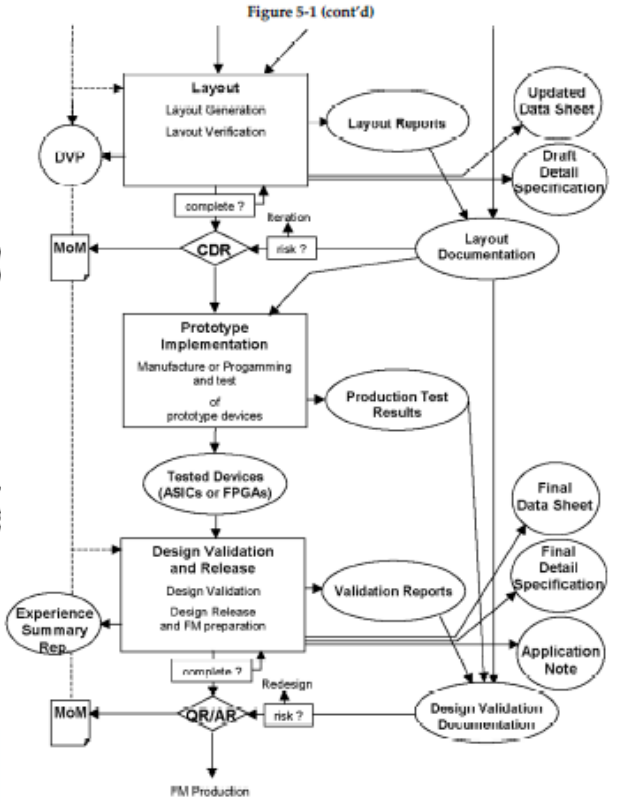
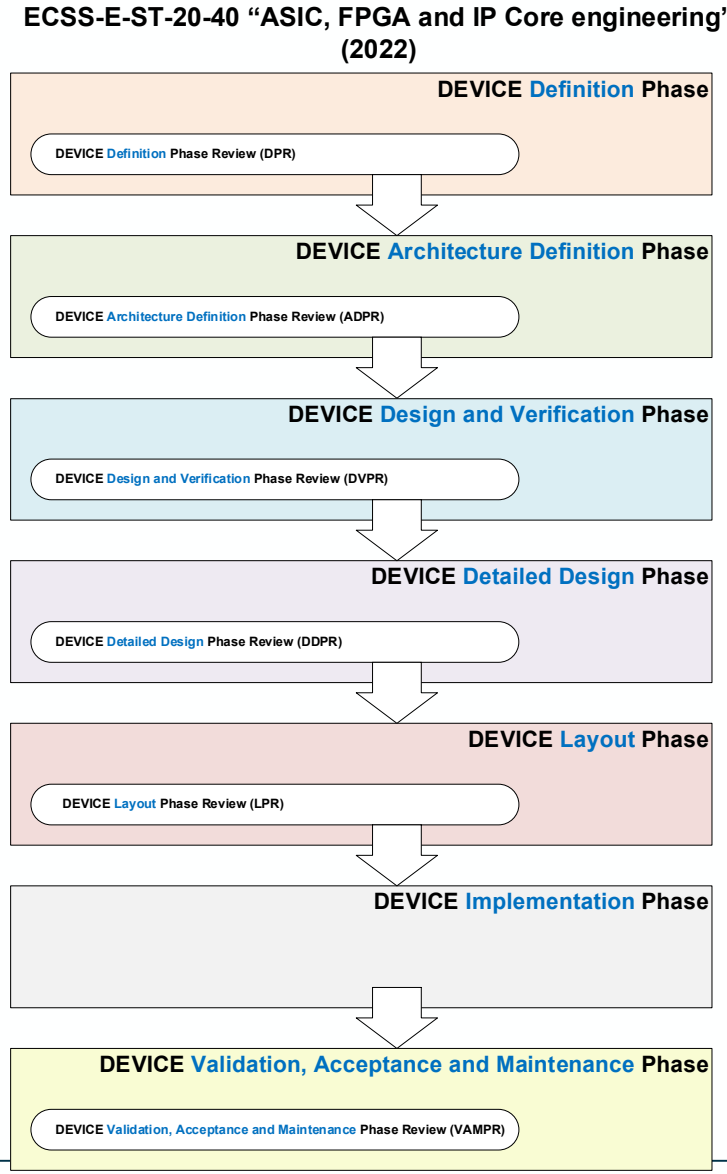
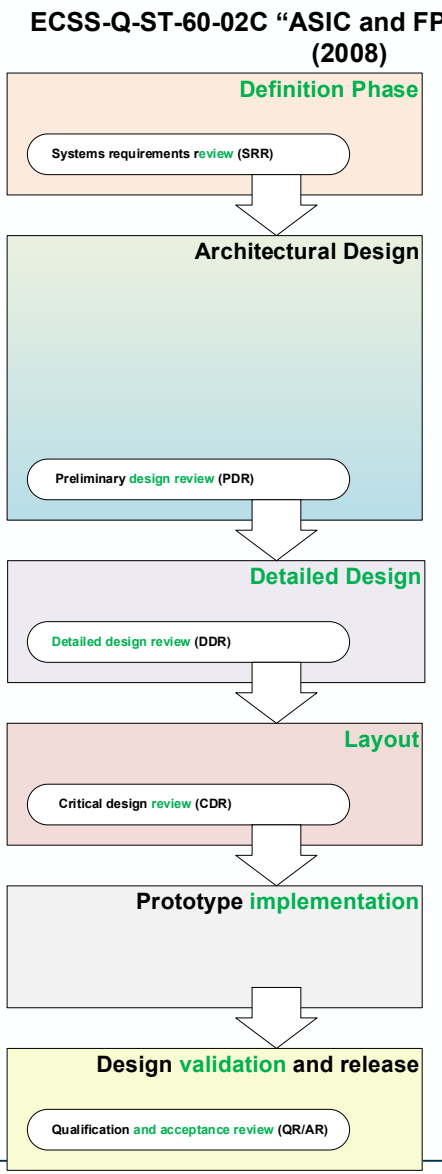


Figure 5-1: Development flow (example) – continued

Summary of name differences of phases and reviews

NEW



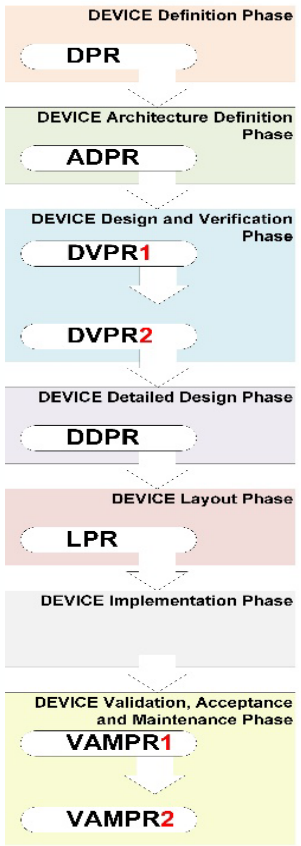


OLD

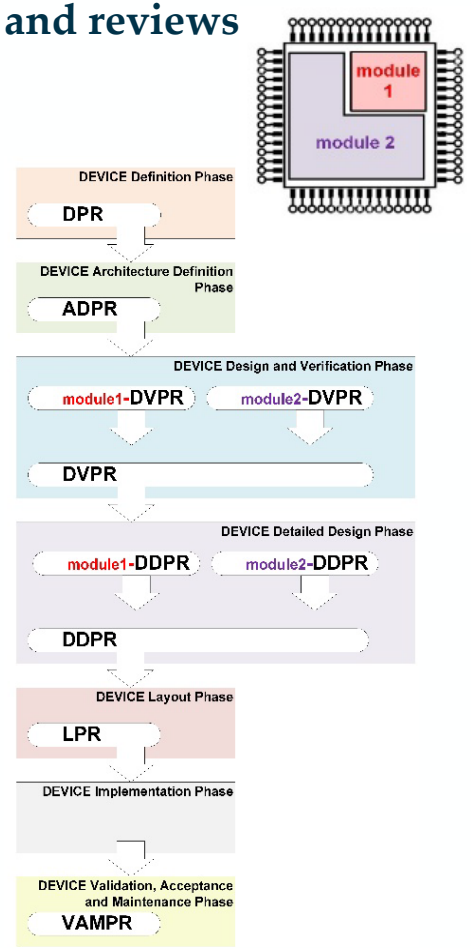
development flow variations

ECSS-E-ST-20-40 (2022)

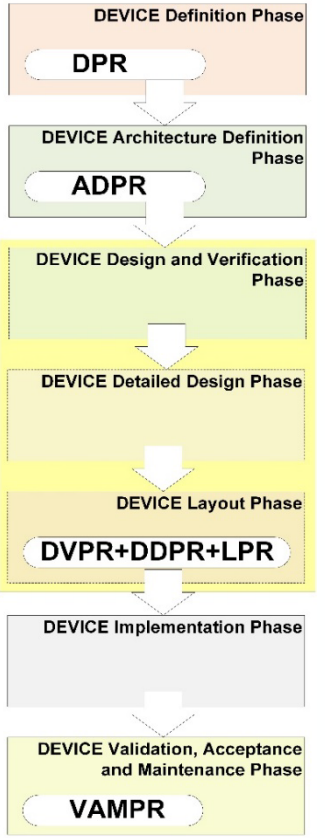
intermediate additional reviews



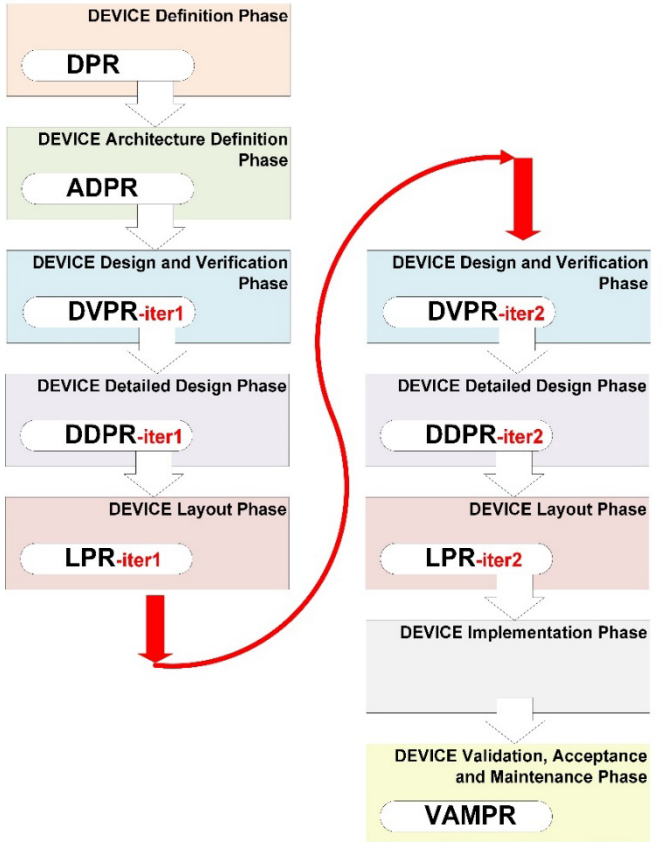
parallel modules developments and reviews



phases merging



iterations of phases



Pre-tailoring according to DEVICE criticality category

Two main **DEVICE criticality categories** (based on criticality categories defined in ECSS-Q-ST-30 Dependability clause 5.4, also used in ECSS-Q-ST-80 Software PA):

- **A** or **B** or **C** criticality (catastrophic, loss of mission or major effects) -> all requirements apply
- **D** criticality (minor effects) -> some requirements are waived or made lighter (e.g. less or no documentation requested)

Pre-tailoring table in new chapter 6

The same table indicates tailoring per DEVICE type and criticality

Approximately **20%** of all requirements are waived or relaxed for category **D** DEVICES (all R&D developments, minor impact to the mission where DEVICE will fly)

ECSS Source ID	Requirement main text	Requirement NOTES	ECSS Object Type	**Digital ASIC**	**Analog ASIC**	**FPGA**	**IP Core**	**CRITICALITY Category D** (minor consequences in case of failure)
4.3.4.2i	Development team, companies involved (designers, foundry, subcontractors, suppliers), indicating technical and administrative interfaces, and clear assignment of tasks. [ALL]		Requirement	yes	yes	yes	yes	yes
4.3.4.2j	The development methodology of any subcontractors in charge of developing any of the Building Blocks for the DEVICE shall be ascertained by the supplier and agreed with the customer. [ALL]	NOTE For example, whether deviations or tailoring to this standard will be applied.	Requirement	yes	yes	yes	yes	no
4.7.2c	The core and IO-pad ring power distribution shall be generated. [D-ASIC, A-ASIC, --, --]		Requirement	yes	yes	no	no	yes
4.7.2d	Test pads, if needed, shall be generated. [D-ASIC, A-ASIC, --, --]		Requirement	yes	yes	no	no	partial (no report required)

Distribution of requirements per DEVICE type

TOTAL NUMBER OF REQUIREMENTS

272

20% fewer "engineering" requirements than in the old standard which has 333 "engineering" requirements

D-ASIC	**A-ASIC**	FPGA	IP Core		
x	x	x	x	201	74%
	x			4	
x		x	x	8	
x	x			13	
x	x	x		20	

23

"conditional" requirements

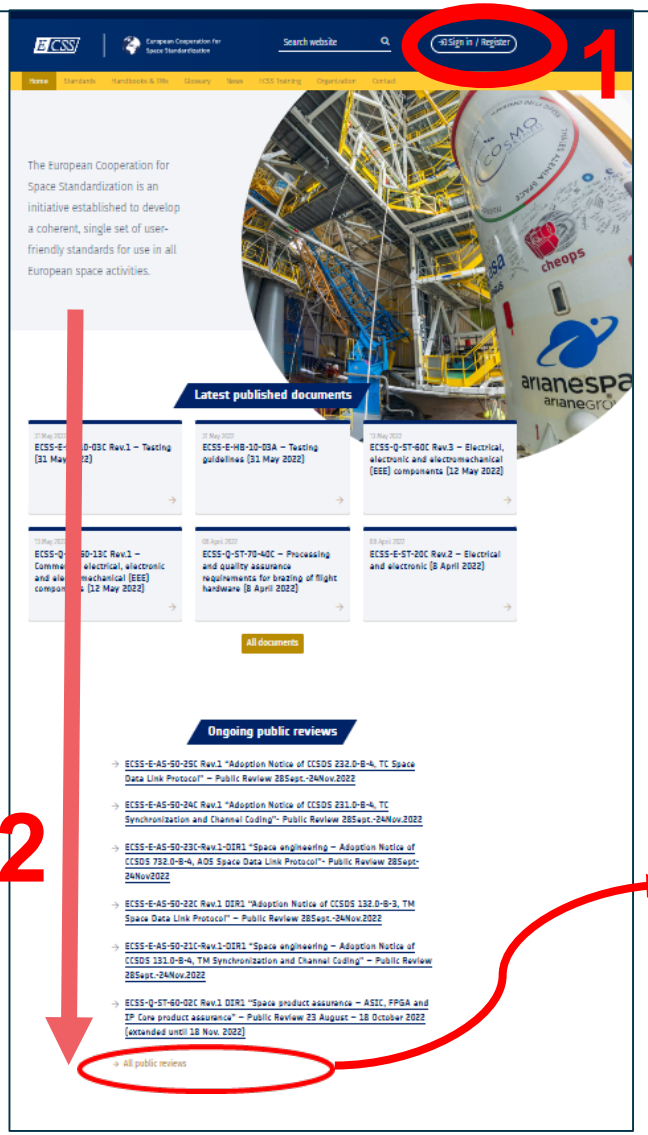
(start with "**If**" …)

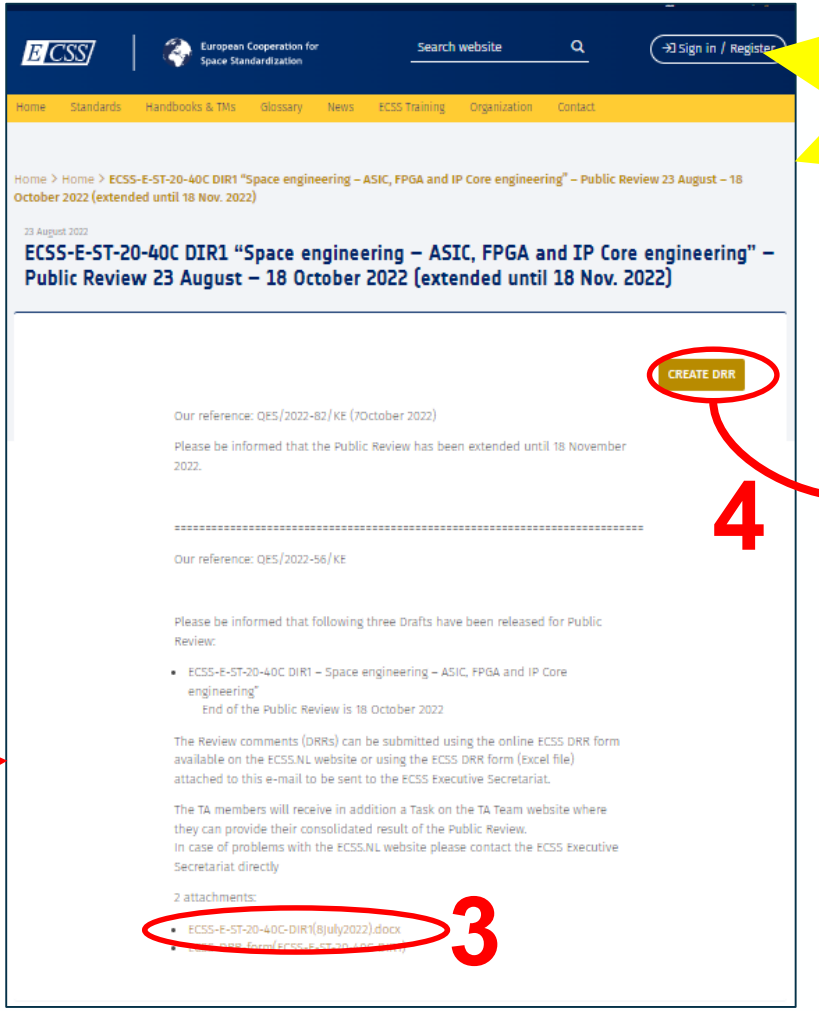
to be discussed and agreed between customer and supplier at the beginning of the DEVICE development

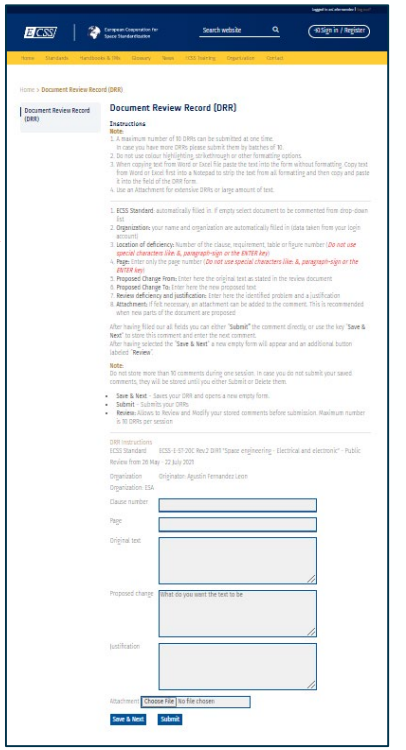
How to create Change Requests for ECSS standards in Public Review

Submission deadline Nov 18th 2022

1. https://ecss.nl/ : register and sign in
2. scroll down to find all “**Ongoing public reviews**” and select
3. read the standard
4. open the “Document Review Record” to create and submit a change request following the instructions







THANKS for your attention,

QUESTIONS?

ad-hoc info sessions for industry to get to know the new ASIC/FPGA/IP E and Q standards can be organized on demand agustin.fernandez-leon[at]esa.int

Backup slides

SW-HW co-engineering in DEVICEs embedding “processing units”

- There were no requirements specific to HW-SW co-engineering in “ old” std
- Definition of “software” and “processing unit” added
- Improvements to definitions of “IP Cores” and “building block” that can help to the better handling of ”processing units” used or put inside the DEVICE
- Several new requirements **interaction between HW and SW design teams** (outputs/inputs exchanged, scheduled milestones)

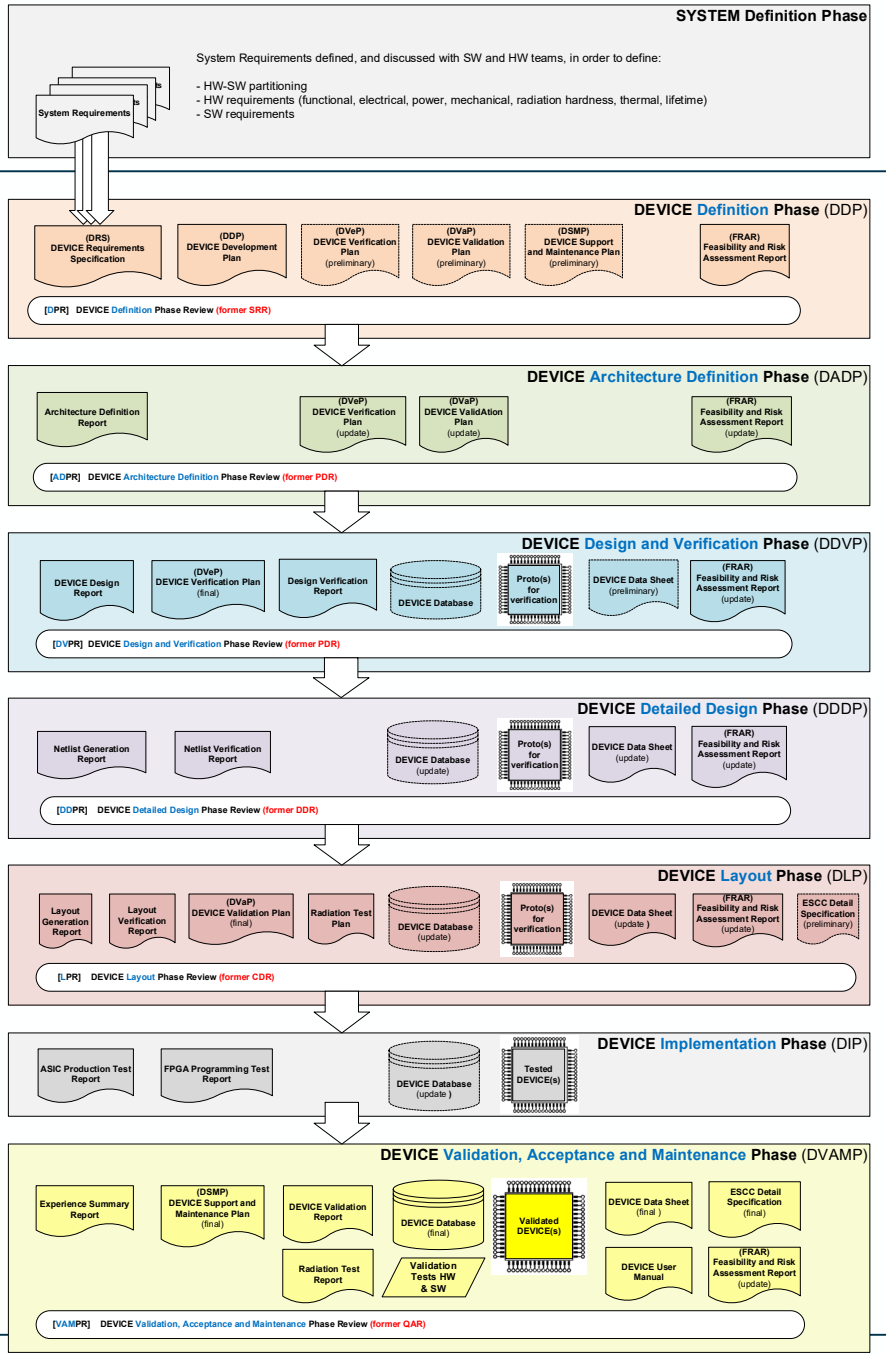
ANALOG / MS DEVICE developments

- Several new requirements on:
  - **tailored development flow variations** (phases/reviews merging, individual modules parallel flows, additional intermediate reviews, iterations if appropriate and agreed with customer) at the beginning
  - **interaction between digital and analog design teams** (outputs/inputs exchanged, scheduled milestones)
  - subcontracted design work to **third parties**, their design methodology and compliance to the ECSS standard
  - development and use of **Analog IP Cores**
- Several “old” requirements specific to A/MS ASICs **revised and improved** by WG analog experts in dedicated WG meetings

[**ACTION** for AMICSA 20XX attendees]
All experts, future users of the new standards, are kindly invited to help optimize the new standard, by reading the draft once it is published for ECSS **public review**, and submitting Change Requests

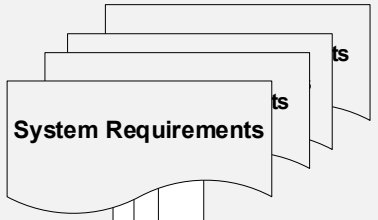
Phases, reviews, expected outputs

Generic development flow



phases, reviews and outputs

SYSTEM Definition Phase



System Requirements defined, and discussed with SW and HW teams, in order to define:

- HW-SW partitioning
- HW requirements (functional, electrical, power, mechanical, radiation hardness, thermal, lifetime)
- SW requirements

DEVICE Definition Phase

(DRS)
DEVICE Requirements Specification

(DDP)
DEVICE Development Plan

(DVeP)
DEVICE Verification Plan
(preliminary)

(DVaP)
DEVICE Validation Plan
(preliminary)

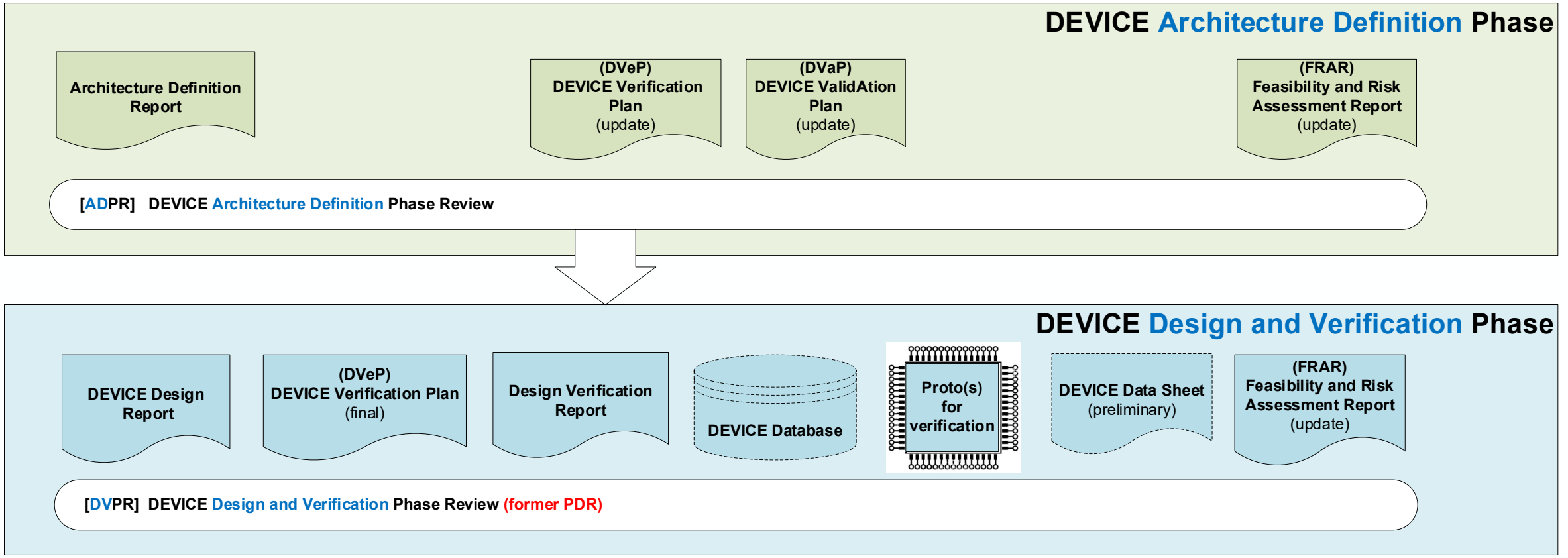
(DSMP)
DEVICE Support and Maintenance Plan
(preliminary)

(FRAR)
Feasibility and Risk Assessment Report

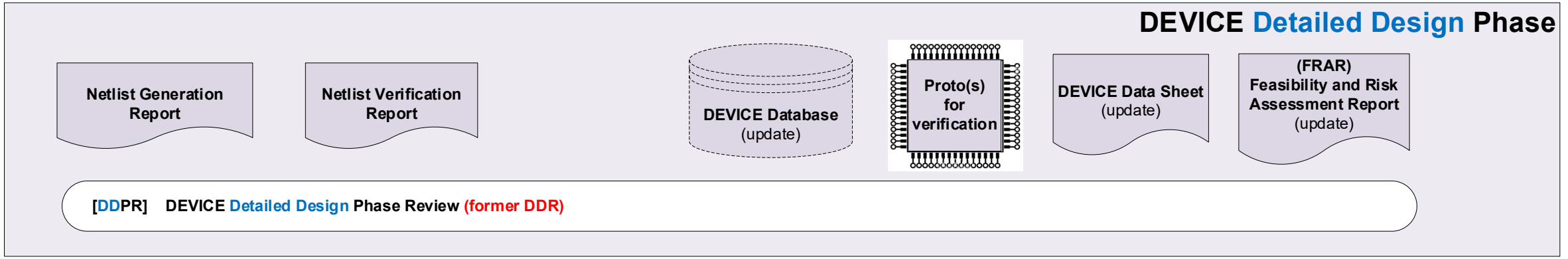
[DPR] DEVICE Definition Phase Review (former SRR)

phases, reviews and outputs

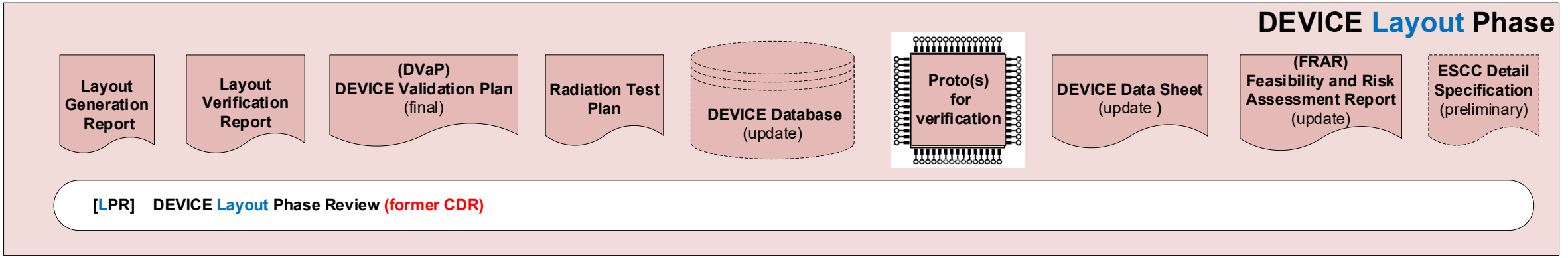
NEW PHASES + NEW REVIEWS resulting from splitting former “Architectural Design phase” into two phases !



phases, reviews and outputs

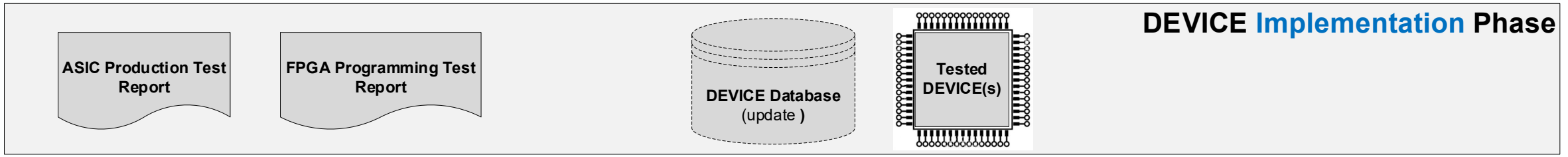


phases, reviews and outputs



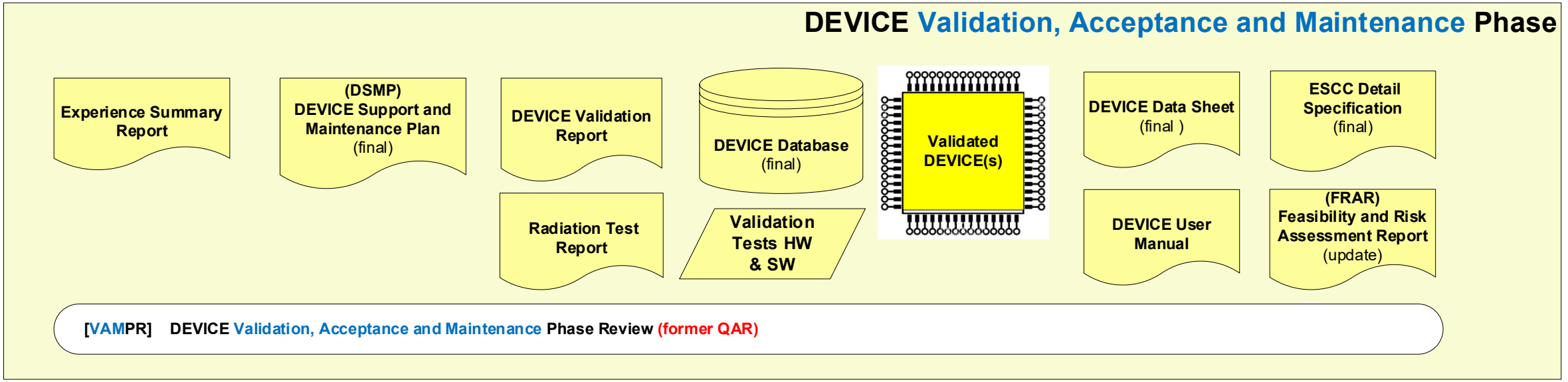
phases, reviews and outputs

former “Prototype implementation phase”



phases, reviews and outputs

former “Design Validation and Release phase”



Name differences of phases, reviews and outputs

ECSS-Q-ST-60-02C (2008)			ECSS-E-ST-20-40C (2022)		
phases	**reviews**	**outputs**	**outputs**	**reviews**	**phases**
Definition phase	System Requirements Review **(SRR)**	a. the definition phase documentation, containing: 1. ASIC and FPGA requirements specification (ARS); 2. Feasibility and risk analysis (FRA); b. ASIC and FPGA development plan (ADP); c. MoM of SRR.	a) DEVICE Requirements Specification (DRS) b) Feasibility and Risk Assessment Report (FRAR) c) DEVICE Development Plan (DDP) d) DEVICE Verification Plan (DVeP) (preliminary) e) DEVICE Validation Plan (DVaP) (preliminary) **f)** DEVICE Support and Maintenance Plan (DSMP) (preliminary)	**DEVICE Definition** Phase Review **(DPR)**	**DEVICE Definition** Phase
Architectural design	Preliminary Design Review **(PDR)**	a. Architecture definition report; b. Verification plan; c. Architecture verification and optimization report; d. Preliminary data sheet; e. Design database, containing: 1. Simulation models; 2. Verification results; f. MoM of PDR.	a) Architecture Definition Report (ADR) b) DEVICE Verification plan (update) c) DEVICE Validation Plan (update) d) FRAR (update)	**DEVICE Architecture Definition** Phase Review **(ADPR)**	**DEVICE Architecture Definition** Phase
			a) DEVICE Verification Plan (final) b) Architectural Design Report c) Design Verification Report d) Data Sheet (DS) (preliminary) e) DEVICE database f) FRAR (update)	**DEVICE Design and Verification** Phase Review **(DVPR)**	**DEVICE Design and Verification** Phase

Name differences of phases, reviews and outputs

ECSS-Q-ST-60-02C (2008)			ECSS-E-ST-20-40C (2022)		
phases	**reviews**	**outputs**	**outputs**	**reviews**	**phases**
Detailed design	Detailed Design Review **(DDR)**	a. Design entry report; b. Netlist generation report; c. Netlist verification report; d. Updated data sheet with pin-out; e. Updated design database, containing: 1. Pre-layout netlist; 2. Constraints for layout (i.e. floorplan and constraints for timing driven layout) as defined in the ADP; 3. Test vectors for production test; f. MoM of DDR.	a) Netlist Generation Report b) Netlist Verification Report c) DEVICE Data Sheet (update) d) DEVICE Database (update)	**DEVICE Detailed Design** Phase Review **(DDPR)**	**DEVICE Detailed Design** Phase
Layout	Critical Design Review **(CDR)**	a. Layout generation report; b. Layout verification report; c. Design validation plan; d. Updated data sheet; e. Updated design database, containing: 1. Post-layout netlist in the agreed format depending on the targeted technological approach (GDS II, FPGA P&R files or other); 2. Corresponding parasitic information; f. MoM of CDR.	a) Layout Generation Report b) Layout Verification Report c) DEVICE Validation Plan (final) d) Radiation Test Plan e) DEVICE Data Sheet (update) f) ESCC Detail Specification (preliminary) g) DEVICE database (update)	**DEVICE Layout** Phase Review **(LPR)**	**DEVICE Layout** Phase

Name differences of phases, reviews and outputs

ECSS-Q-ST-60-02C (2008)			ECSS-E-ST-20-40C (2022)		
phases	**reviews**	**outputs**	**outputs**	**reviews**	**phases**
Prototype implementation	n/a	a. Agreed number of tested devices (ASICs or FPGAs); b. Production test results and reports; [not applicable for FPGA designs] ; c. Burn-in or any other production test results, specifications and patterns.	a) Agreed number of tested DEVICES b) Production Test Report c) FPGA Programming Tests Report d) DEVICE database (update)	**n/a**	**DEVICE Implementation Phase**
Design validation and release	Qualification snf Acceptance Review **(QAR)**	a. Validation report; b. Radiation test report (if applicable); c. Release report; d. Experience summary report; e. Final data sheet; f. Final detail specification; g. Application note; h. MoM of QR/AR; i. Validation breadboard; j. Burn-in or screening test boards for FM parts.	a) DEVICE Validation Report b) Radiation Test Report c) Agreed number of validated DEVICES d) DEVICE Support and Maintenance Plan (final) e) Experience Summary Report (ESR) f) DEVICE Data Sheet (final) g) ESCC Detail Specification (final) h) DEVICE User Manual	**DEVICE Validation, Acceptance and Maintenance** Phase Review **(VAMPR)**	**DEVICE Validation, Acceptance and Maintenance** Phase

Pre-tailoring according to DEVICE type

Four DEVICE types (tags next to each requirement indicate applicability as explained in “Conventions” 3.4 section of ECSS-E-ST-20-40):

- **D-ASIC**: applicable to fully digital ASICs, or the digital part of mixed-signal ASICs
- **A-ASIC**: applicable to fully analog ASICs, or the analog part of mixed-signal ASICs
- **FPGA**: applicable to FPGAs
- **IP**: applicable to digital or analog IP Cores

ECSS-Q-ST-60-02C Rev.1 : some content highlights

- **ECSS-Q-ST-60-02C Rev.1 explicitly defines PA requirements from ECSS-Q-ST-60-02C in line with ECSS-Q-ST-10/20/30** -> **no new requirements wrt ECSS-Q-ST-10/20/30 since ECSS-Q-ST-60-02C**
- **New requirements** in ECSS-Q-ST-60-02C Rev.1 cover:
  - Tailoring by criticality (in line with ECSS-Q-ST-30/40), i.e. in line with severity of the consequence of DEVICE failure
  - Alignment to reviews definition in ECS-E-ST-20-40
  - Alignment to verification/validation activities defined in ECSS-E-ST-20-40
  - Security Assurance
  - Reuse: engineering, verification, legal (licence, IPR) requirements
  - Definition of deactivated and unreachable DEVICE functions
  - Definition of Metrication programme requirements
  - IVV – Independent Verification Validation by Third Party for criticality A and B
  - Qualification status assessment and maintenance, in line with ECSS-M-ST-10 and ECSS-Q-ST-20
  - Process assessment and improvement