EVOLEO TECHNOLOGIES

# Deterministic COTS based OBC for high performance and mixed criticality applications

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# Presentation Outline

1. Introduction and Background
2. CHICS OBC Architecture
3. Exploiting the Zynq Ultrascale+
4. Fault Detection, Isolation and Recovery
5. Conclusions and Outlook

## EVOLEO TECHNOLOGIES, Lda

- Created in Jan 2007 in Maia (Porto), **Portugal**
- SME - design of **reliable** electronic, electromechanical and software systems
- **Embedded**, **computational** solutions
- Monitoring, data processing, integrated intelligence SW
- Vertical system integration for small/medium size solutions
- Collaborations driven – European/Portuguese

## EVOLEO TECHNOLOGIES, GmbH

- Created in March 2018 in Munich, **Germany**
- SME starting upon the baseline capabilities of the parent company in PT, yet independent
- Focus on **Space and Monitoring** activities on **electronics** and **embedded computational** solutions
- Collaborations driven – European/German

# Key References, areas of Expertise and Solutions

**ALPHASAT TDP8**
(ESA)

Components Technology Test Bed

**Expertise**
OBC/PLIU
OBSW
PDCU
SCOE

TRL9

**ISS – ANITA2**
(ESA)

Analysing Interferom. for Ambient Air

**Expertise**
PSDU

TRL9

**ARIANE 5/6 VIKI**
(ARIANE)

Launcher Video Kit

**Expertise**
PDCU

TRL9

**ESAIL AIS**
(ESA)

AIS micro satellite

**Expertise**
OBSW
ADCS
EGSE

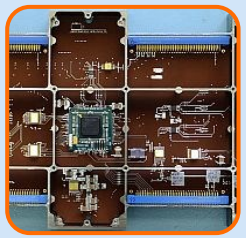
TRL9

**AOLTB/PBSA**
(ESA/EU FP7)

Optical link / Photonics Biosensor

**Expertise**
OBC/PLIU
OBSW
PDCU
SCOE

TRL6



**PLATO AEU**
(ESA)

Ancillary Electronics Unit

**Expertise**
Digital Controller
EGSE

TRL6

**GALILEO CPSU**
(ESA)

Power Supply Unit

**Expertise**
Digital Controller
EGSE

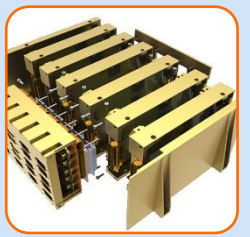
TRL4

**PATCU**
(ESA)

Payload Temperature Control Unit

**Expertise**
Analog design
EGSE

TRL4



**CHICS / PLANE**
(ESA)

COTS Computer System

**Expertise**
OBC/PLIU
SDR

TRL4

**Flight**

**Design**
- ELE/MEC/THM
- Digital HW
- Analog HW
- SW/FW

**Key Solutions**
- OBC/PLIU
- Digital Controllers
- PSDU/PDCU
- OBSW

**Key Solutions**
- EGSE
- SCOE
- Test & Reporting SW

**Verification**
- Test Procedures
- Functional Tests
- Environmental Tests
- Prototyping

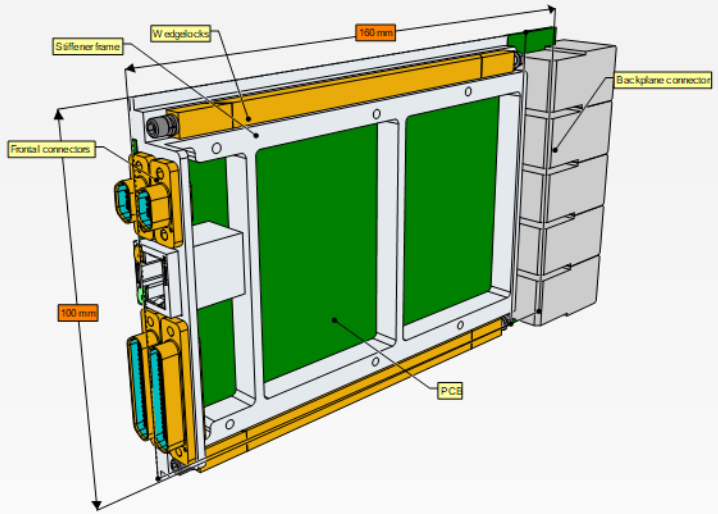
**V&V**

# Airbus Defence and Space, Ottobrunn

- Digital Payload Processing (including ADC/DAC)
- Space grade and COTS technologies
- Machine Learning & Artificial Intelligence
- Telecom processing / control platforms

# CHICS OBC

- **COTS based Highly Integrated Computer System for mini/nano satellites** ESA Contract 4000130743/20/NL/FE supported by DLR
- Small Satellites, LEO
- **Dual Lane, 3U**, **cPCI Serial Space (ADHA)**
- **SAVOIR** compliance
- **Radiation tolerant COTS** – XQ Zynq MPSoC + PolarFire
- **OBSW** - FreeRTOS + Petalinux with XEN Hypervisor
- **Applications** – Star tracker, GNSS, Anomaly detection using ML, AI for Noncritical Applications
- **CCSDS TM/TC** encoder and decoder
- **Connectivity** – SpW, CAN, UART, Ethernet
- **Memory** - TMR 32GB NAND Flash (Platform/SGM) and up to 1TB NAND Flash (Payload/Mission)
- **FDIR** – PUS based architecture





| | | |
|---|---|---|
| 6 CPUs + 2 FPGAs | Autonomous fault handling | COTS components |
| Multi-Gbps interfaces | Supervised operation | <100k€ avionics (10x less vs Legacy) |
| Up to 1TB storage | > 99% Availability | Fast "time-to-market" |
| >100Mbps downlink | >= 5 Years in LEO | Fast "industrial-inspired" implementation |
| Low mass, low Power | Inflight reconfiguration | |

# CHICS based projects

**ADAP** (Contact: Andreas C Koch, PhD Candidate, andreas.c.koch@airbus.com)

- Machine Learning-Based on board Autonomy, Failure Prognostic and Detection
- ESA contract ESA AO/1-10612/20/NL/AS
- Consortium consists of Evoleo Technologies, Airbus Defense and Space and Fraunhofer Institute
- Use Cases Evaluated
  - AOCS Sensor (Pitch and Roll)
  - Payload Antenna
  - Solar Array Degradation

**AI4NCA**

- AI for non-mission critical on-board data processing
- ESA contract ESA ITT AO/1-10711/21/NL/AS
- Consortium consists of Evoleo Technologies, Airbus Defense and Space and Technical University Munich
- Proposed Use Cases
  - Radar Autonomy
  - Optical Automomy
  - Data Compression or Analysis

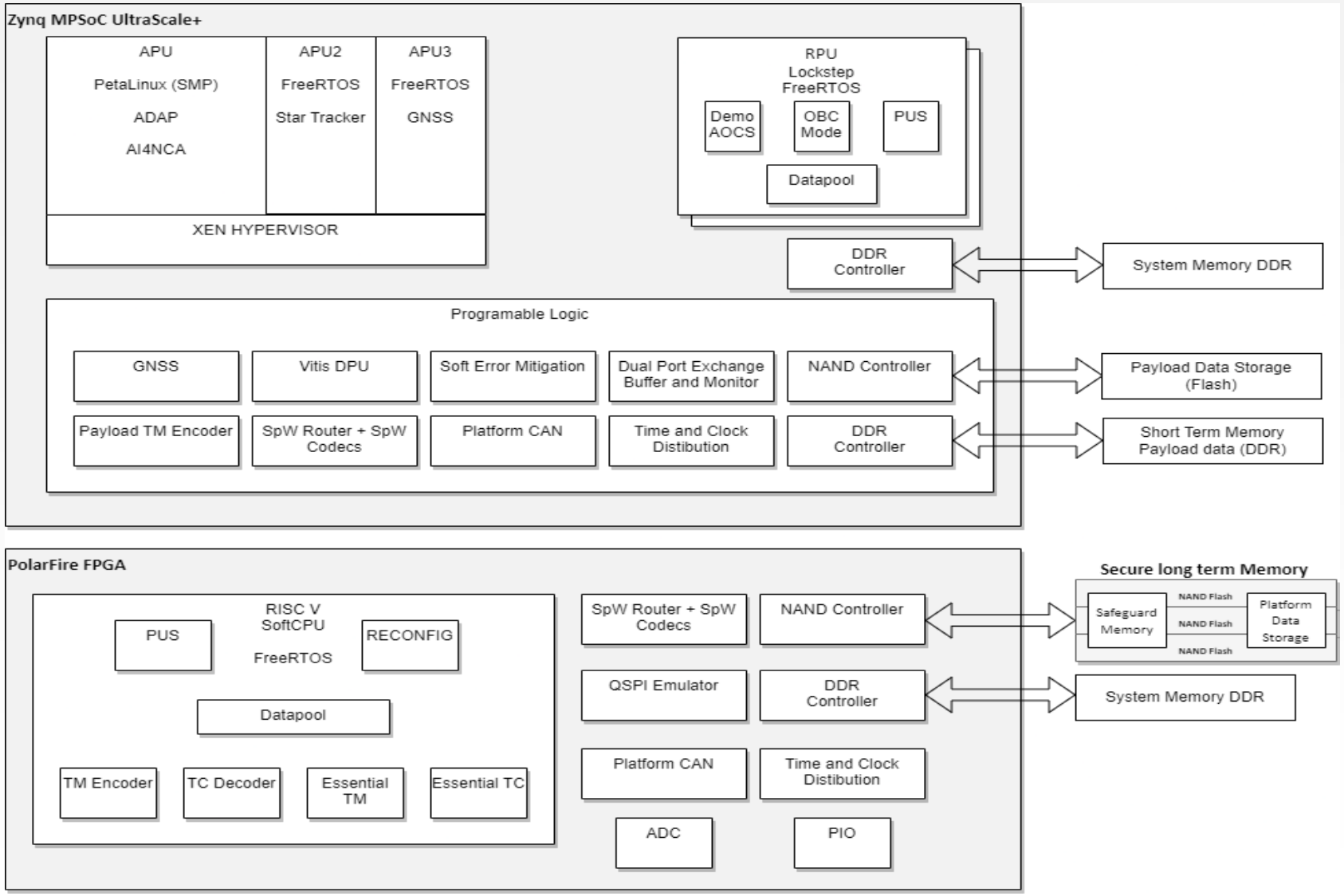
# CHICS Architecture

**XQ Zynq UltraScale +**

- High performance functions & interfaces
- OBSW + Payload applications
  - Mixed criticality of applications including AI/ML
- SpaceWire Router/ports for TM/TC data PUS packets
- PUS based FDIR

**PolarFire FPGA**

- Critical Functions – maintains controllability of OBC
- CCSDS TM/TC Encoder/Decoder
- SpaceWire Router for TM/TC  distribution
- PUS based complex board supervision & recovery
- Secure storage of critical datasets (TMR NAND Flash)



# CHICS MPSoC Overview

**Hybrid Multicore Software (AMP and SMP)**

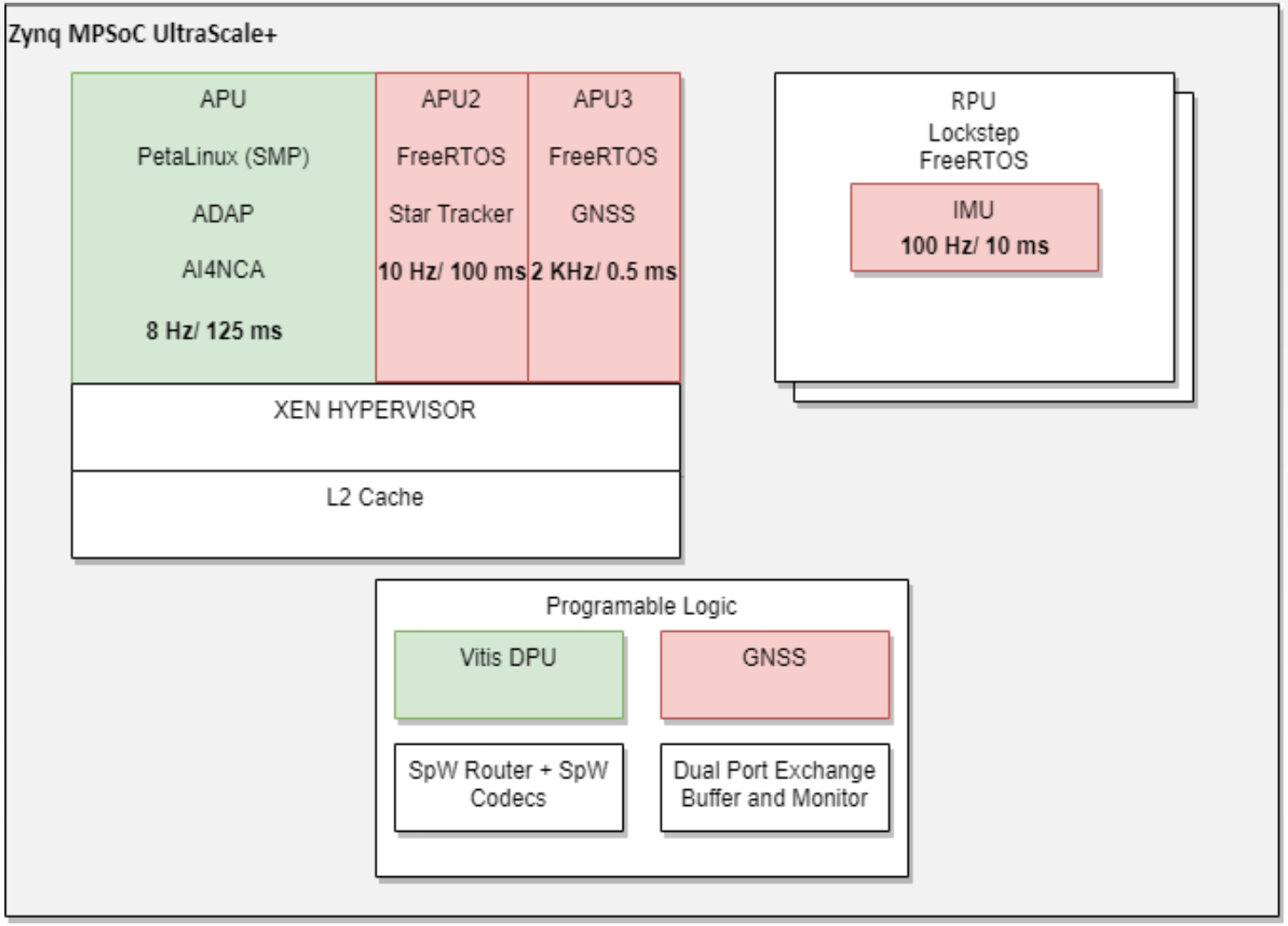
- Inter core communication framework
- Xen Hypervisor
- Access Violation
- System Protection

**Hybrid Multicore Hardware**

- QoS with low latency or high throughput
- Delegation to HW Accelerators

**Software Partitioning**

- Static Assignment
- Time and Space
- Interference reduction

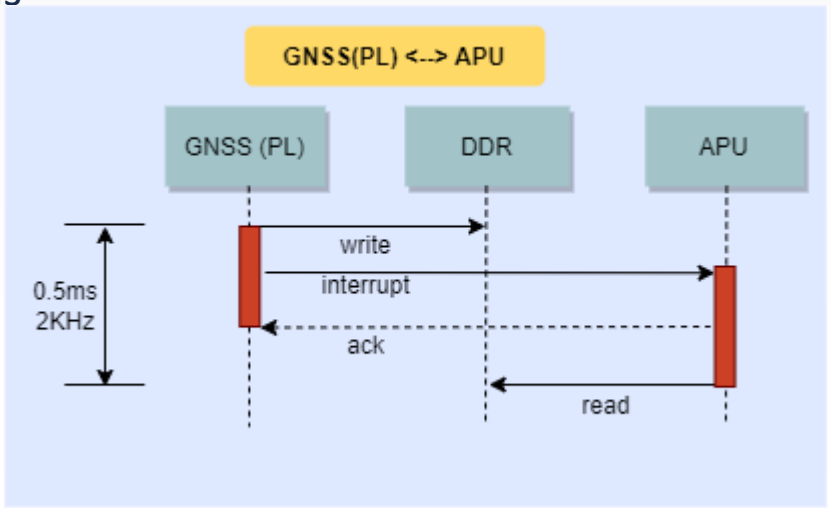


# CHICS Cache Coloring

- Each color represents 256 MB on the MPSoC DDR

**Test Setup**

- PL AXI master XEN guest writing DMA bursts on DDR and sending an interrupt to the APU at 2 KHz (0.5 ms)
- Bare metal guest inducing stress
- Interrupt latency with stress measured at 1800 ns



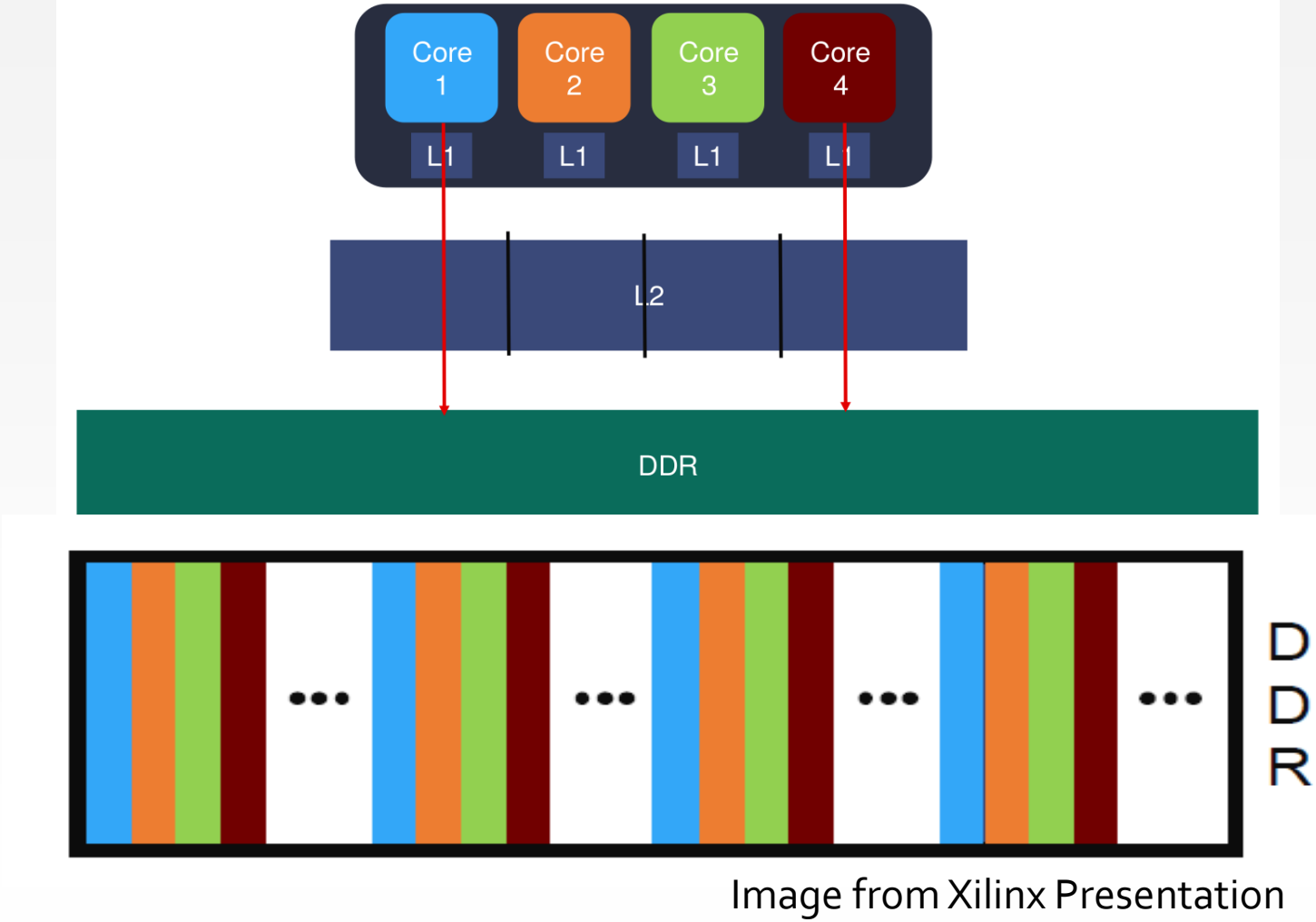




Image from Xilinx Presentation

# CHICS MPSoC Inter Processor Communication

**Secure Exchange Buffer**

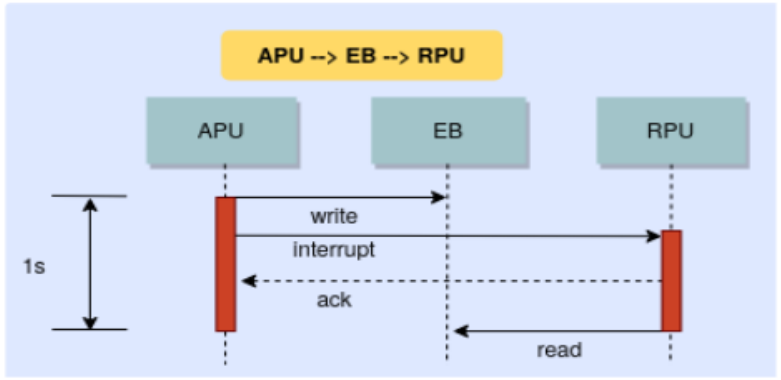
- Dual port BRAMs on PL
- ECC with SECDED

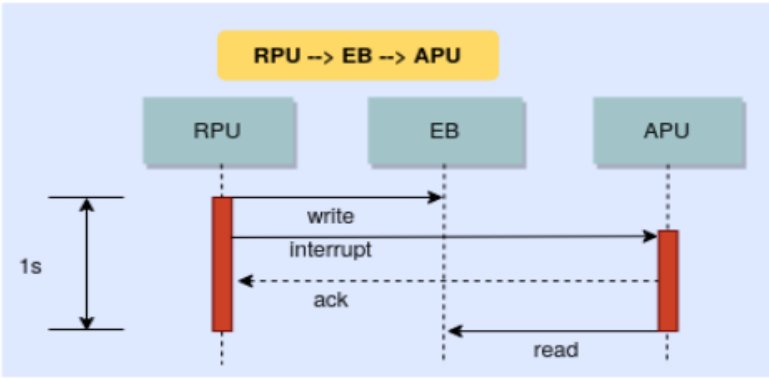
**Inter Processor Interrupts**

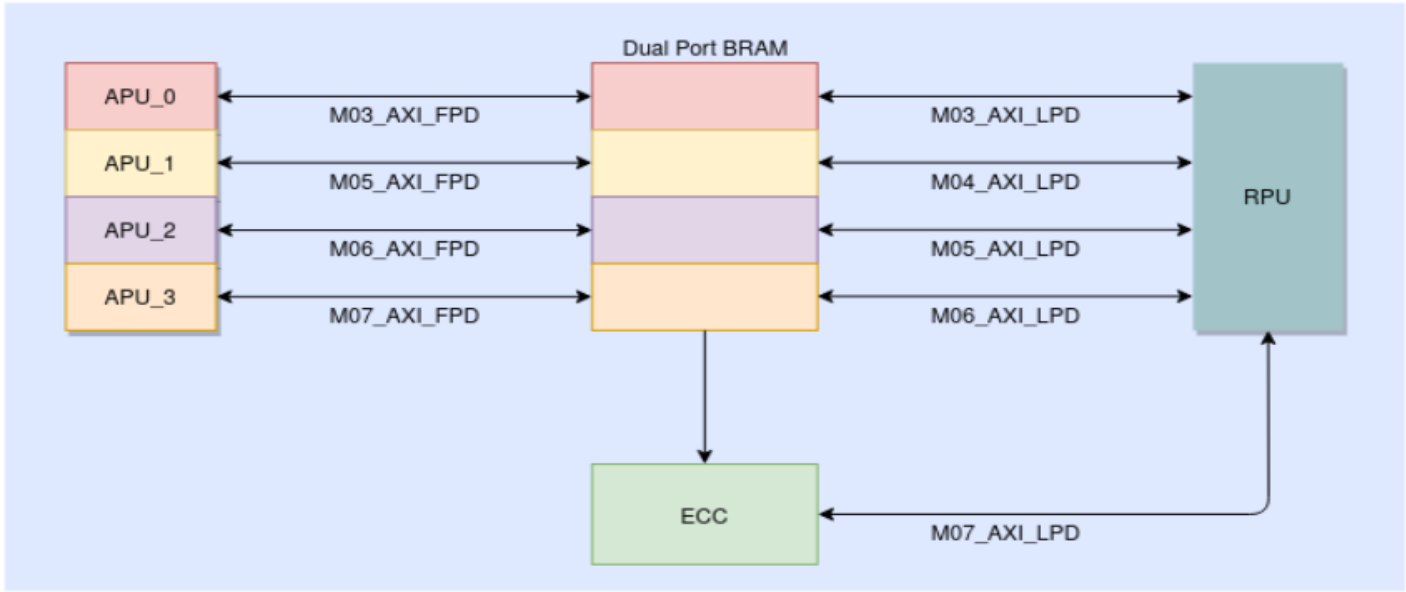
- Read/Write synchronization
- Short message service

**Shared memory region on DDR**

- XEN configuration
- Reserved memory for Linux kernel



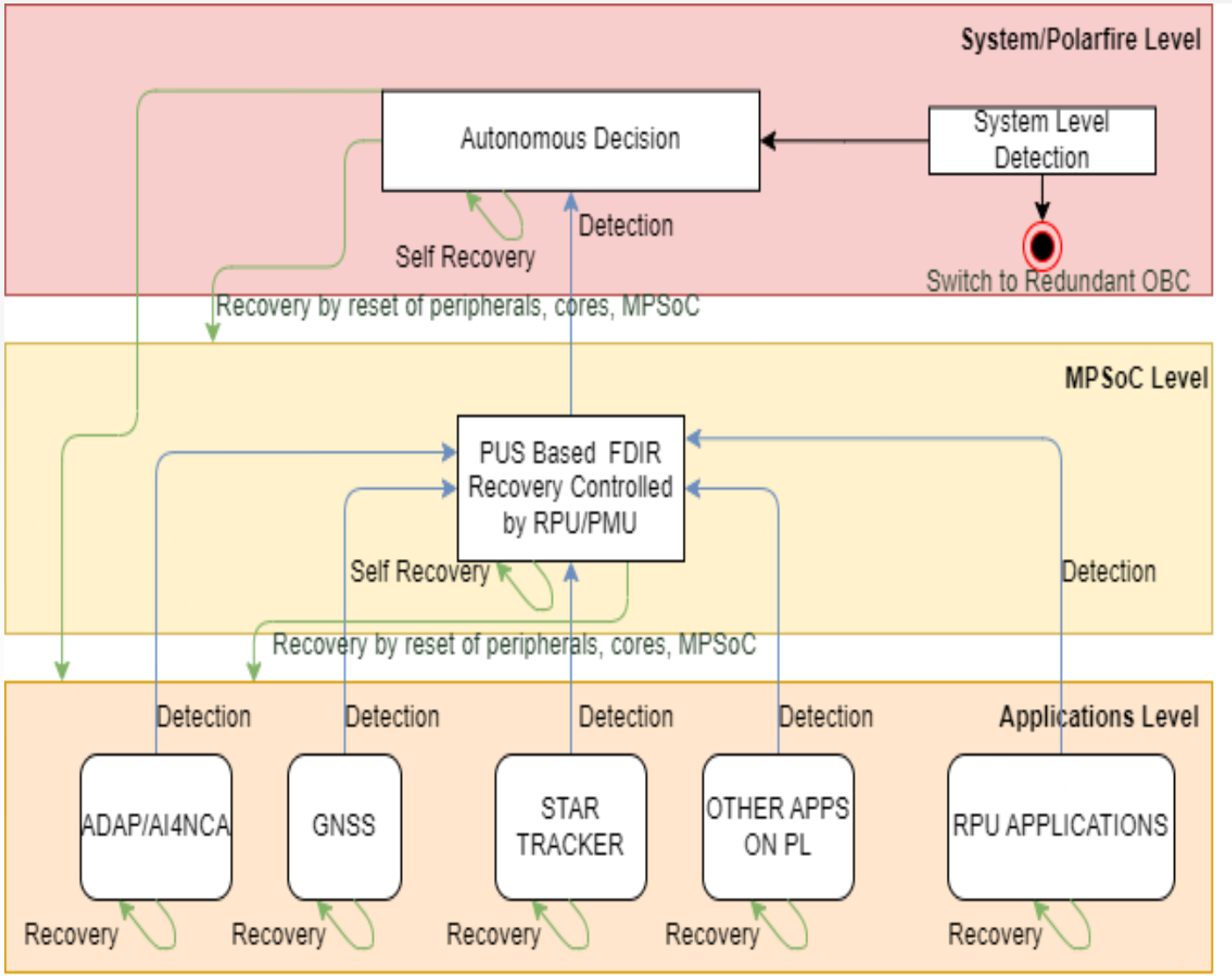
# CHICS FDIR Strategy

**Hardware Protection**

- LCLs, Switches, System Monitors for voltage, currents
- Software controlled power domains

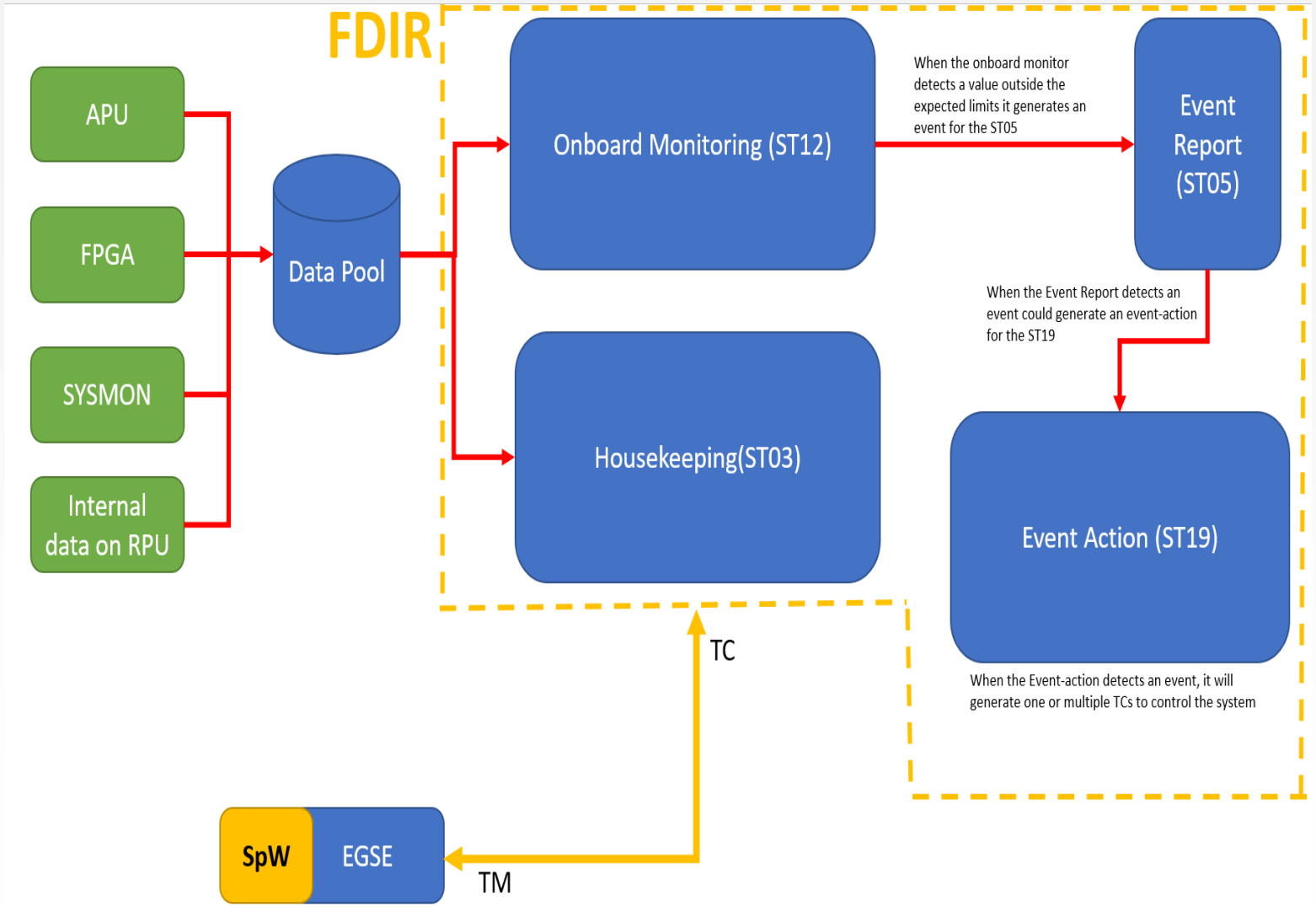
**Software Protection**

- Hierarchy based FDIR Architecture
- ECC checks
- Heartbeat monitoring, watchdog timeouts
- Self Tests and memory scrubbing
- Advanced AI/ML algorithms
- Context sharing for hot redundant operations
- Software controlled resets on a granular level
  - indvidual software routines
  - peripherals
  - processing masters



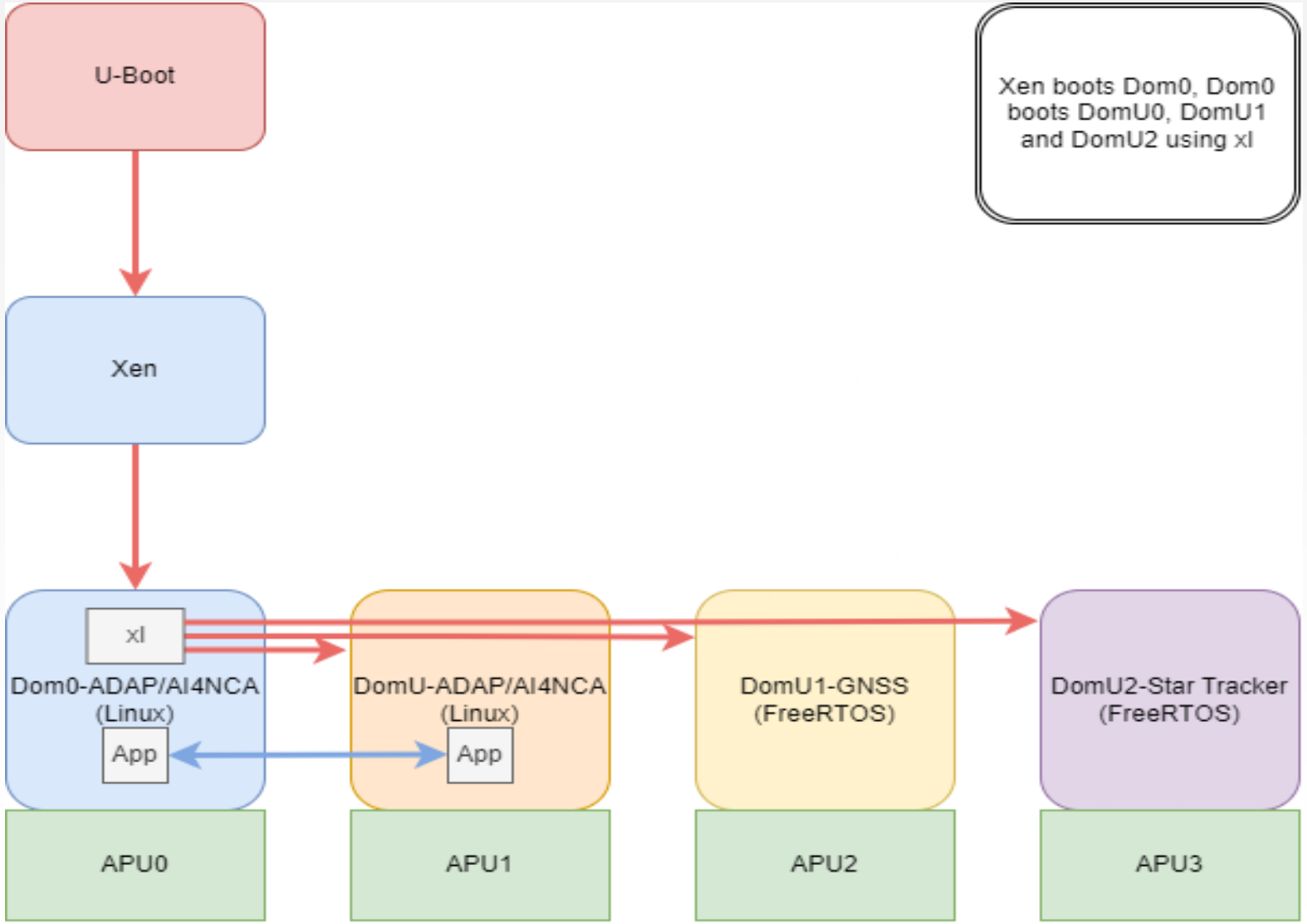
# CHICS PUS Based FDIR

- ECSS-E-ST-70-41C PUS packets
- Allocation on RPU and Polarfire Risc-V



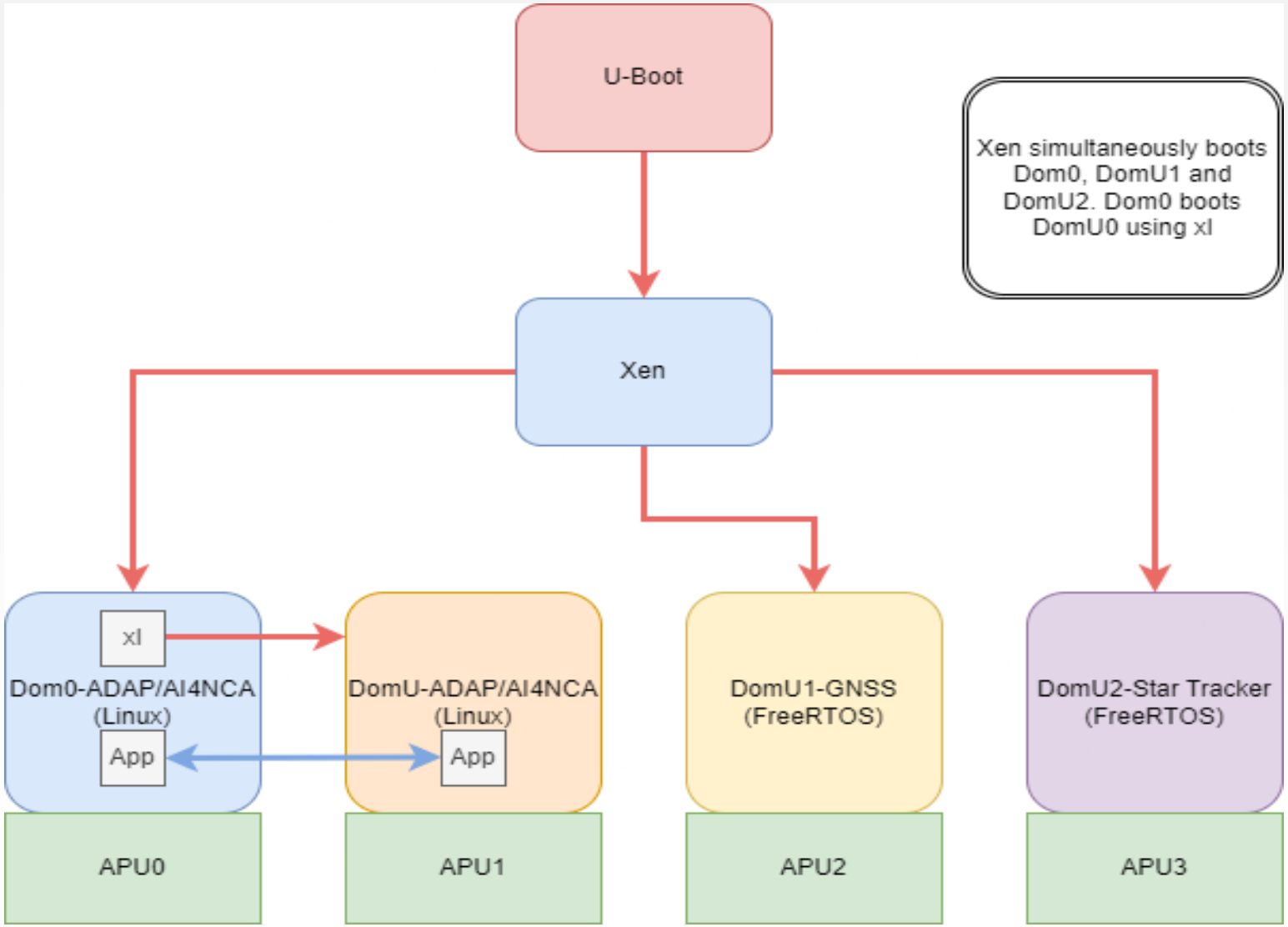
# CHICS Boot Configuration

- Default Boot Method
- Boot Time approximately 20 to 25 seconds depending on packages
- Finer control of guest applications
- Restarting guests quicker



# CHICS Boot Configuration

- Type 1 hypervisor
- Dom0less Boot
- Boot Time approximately 1 to 2 seconds
- Requires whole APU restart when in case SEU/data corruption irrespective of other healthy applications
- Downtime of non critical payloads higher



# CHICS Conclusion and Outlook

- Generic OBC with versatile payload integration capabilities without compromising on performance and determinism
- Compliant **oriented** SAVOIR, ADHA cPCI space
- Generic System Architecture supports flexible mission configuration also lowers the development effort and mission costs
- Granular FDIR architecture provides maximum availability

## Contact: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