FLASH-BASED MASS MEMORIES

ADCSS 2022

DEFENCE AND SPACE

Benoit LEROY, October 2022

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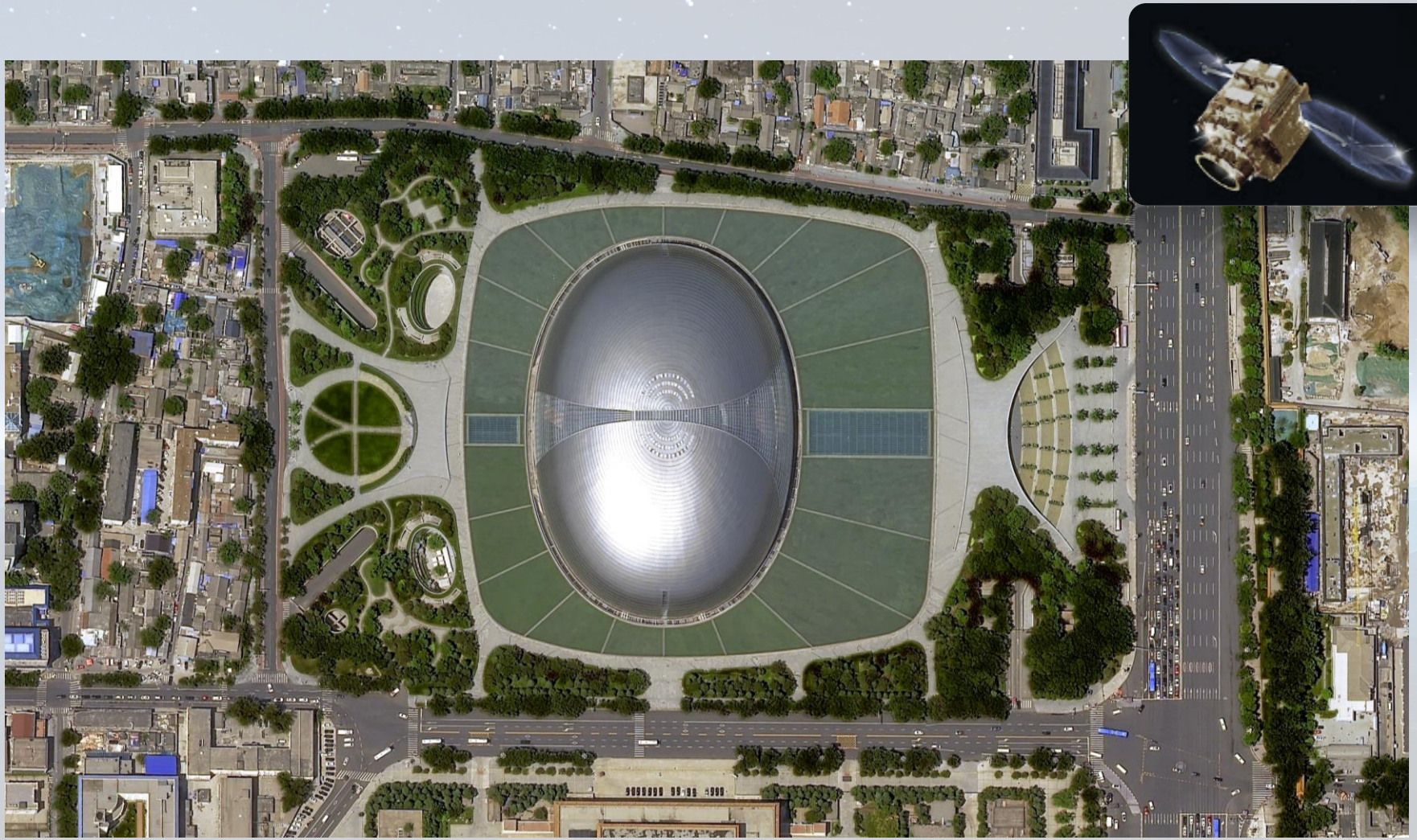
FLASH-BASED MASS MEMORIES



Beijing 15 June 2021 - Pléiades Neo image
File acquired, processed and downlinked by Airbus CORECI2 Memory unit

Agenda

- Introduction
- State of the Art Mass Memories
- Next generations of mass memories
- Airbus Space Electronics Roadmap

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Introduction to Mass Memory Units

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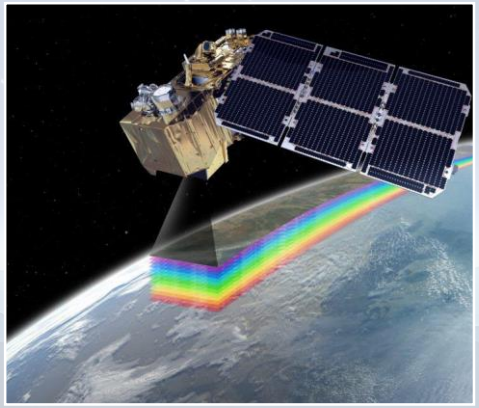
Introduction to Mass Memory Units

Many missions require mass memory units:

Earth Observation

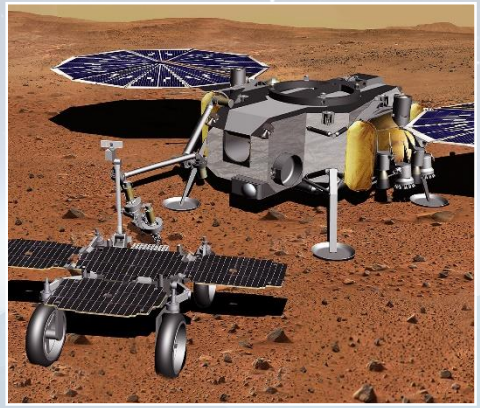


- Pléiades
- Spot
- Pléiades Neo
- Radars
- …

Science

- Metop (weather)
- Copernicus (climate)
- …

Exploration



- Rosetta
- MSR-ERO (Mars Sample-Return)
- …

- **Payload data storage**
  - Optical Instruments
  - Radar Instruments
  - Science Instruments
- **Platform data storage**

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Introduction to Mass Memory Units

Fills two main needs

- Data acquisition while satellite is out of sight of ground stations
- Data acquisition at a higher (or lower) rate than satellite downlink bandwidth : data-rate adaptation

Data are critical to the missions

Broad range of performances (as of 2022)

- Bandwidth storage + downlink: from 100Mbps to tens of Gbps
- Capacity for file storage: from 100Gb to tens of Tb
- x1000 between low-end and high-end

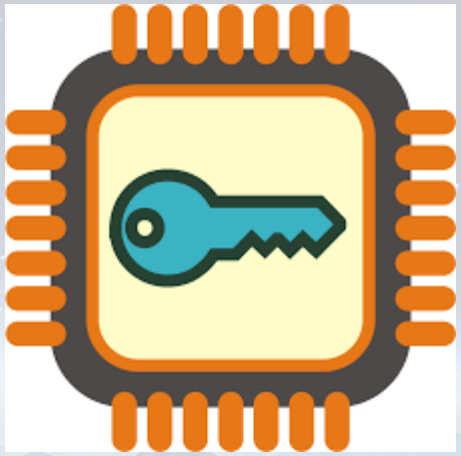
Communication Hub

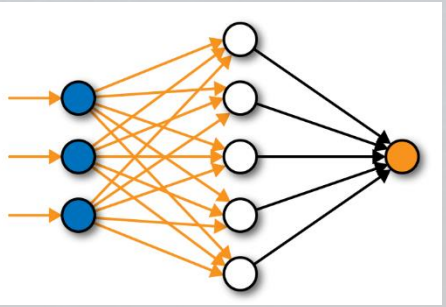
- 1 to 32 simultaneous acquisitions
  - Observation: one high-bandwidth instrument
  - Science: many small-bandwidth instruments
- 1 to 8 simultaneous downlink
  - RF: multiple bands
  - Optical (LCT): multiple wavelengths

Introduction to Mass Memory Units

Much more than a hard drive:

- Metadata (Input datation,…)
- Compression: signal, image, multi/hyper-spectral
- Data analysis, Artificial Intelligence
- Encryption
- Packetization: CFDP, CADU
- Router (eg. Spacewire, Spacefibre)





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State of the art Mass Memory Units

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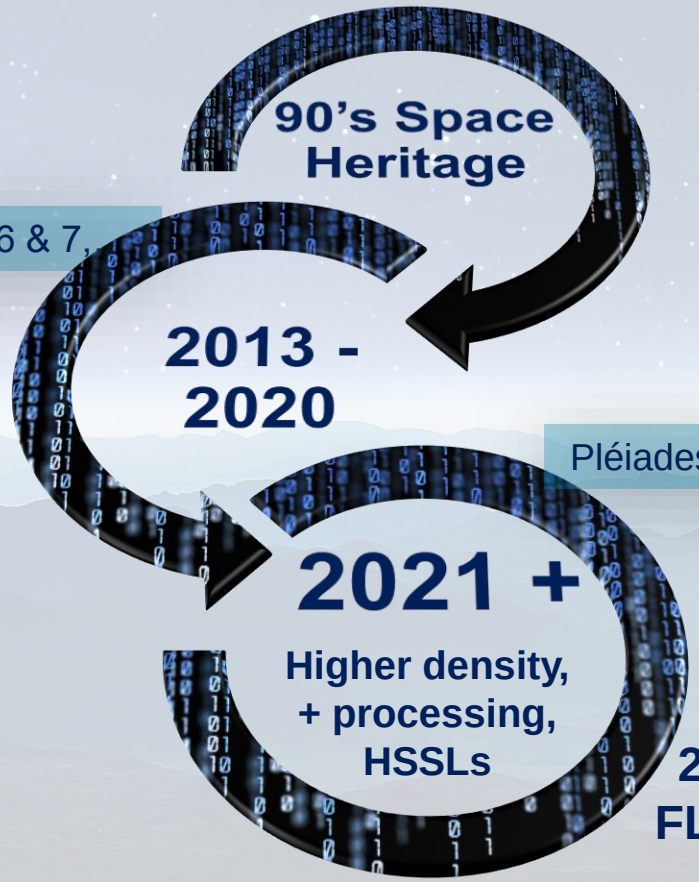
State of the art Mass Memories

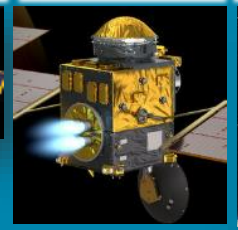
SRAM, SDRAM, DDR technologies

1st Generation FLASH Memories
(Up to 6Tb)



2nd Generation FLASH Memories
(Up to 24Tb)

- **More than 30 years "in-orbit" heritage**
- **Over 50 mass memories launched**
- **No failure recorded**
- **13 years of expertise in NAND flash introduction**

Pléiades NEO	NAOS	MSR-ERO	Copernicus CO2M
			

STATE OF THE ART

…3rd generation : working on it

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State of the art Mass Memories

TRL9

	SRAM, SDRAM, DDR Mass memories	1st gen. SLC Flash Mass memories	2nd gen. SLC Flash Mass memories
Memory capacity	[0,1 ~ 0,8] Tb	[0,4 ~ 6] Tb	[4 ~ 24] Tb
Aggregated data rate Input + outputs	[0,1 ~ 8] Gbps	[0,1 ~ 8] Gbps	[10 ~ 60] Gbps
Power consumptions per memory capacity	[200 ~ 440] W/Tb	[6 ~ 60] W/Tb	[6 ~ 15] W/Tb
Mass per memory capacity	[30 ~ 70] Kg/Tb	[5 ~ 40] Kg/Tb	[1 ~ 2] Kg/Tb

State of the Arts Mass Memories

Detailed on above topics provided in recent conferences :

« **Mass Memory: Status and Perspectives** » Christophe Le Lann, **DASIA 2022** / 2-C-1, May 18th 2022
Introduction to Mass Memory Units / Component Selection / Characterization and Qualification / Mitigation Strategy Elaboration / Memory Controller Development / Mass Memory Unit Buildup / Harvest Flight Heritage / Improve Performances

« **Image Compression on Pléiades Neo** » Christophe Le Lann, Guillaume Rozier, **OBPDC 2022 September 28th 2022**
Pléiades Neo Mission / CORECI2 Unit Architecture / Pre-Processings / Compression Algorithm / Mass Memory / Ciphering and Downlink / On-going Developments

State of the art Mass Memories - CORECI2

All in one box

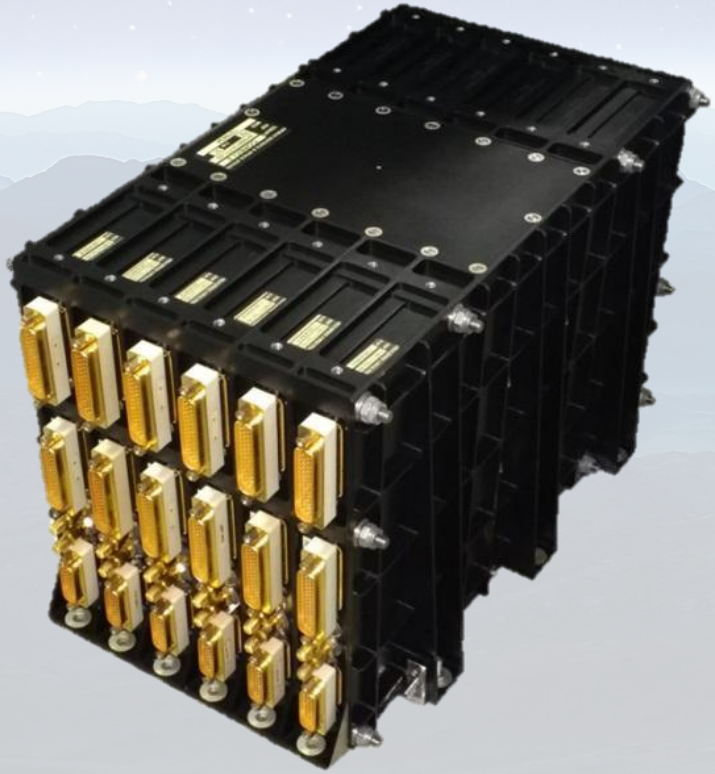
- **CO**mpression
- **RE**cording
- **CI**phering

Microchip RTG4-based

- Reprogrammable for other missions

Scalable architecture

- Slice-based, all identical
- Need more perf -> Use more slices
- Graceful degradation (swath reduction)



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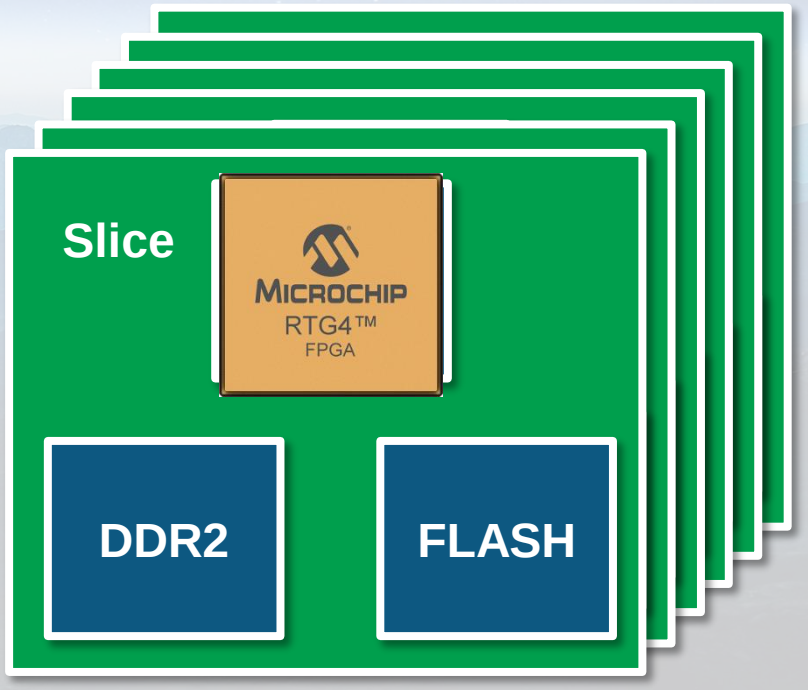

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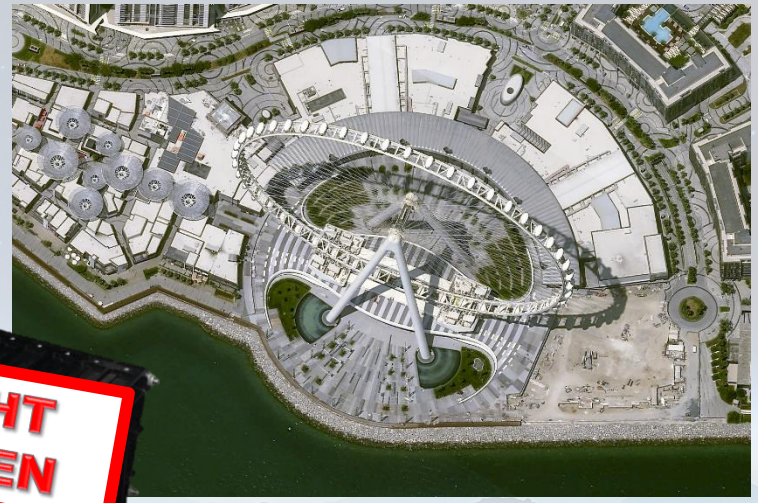
Results

Compression, Recording and Ciphering in a single box

- Better image quality at same compression rate than CCSDS 122.0
- 79% RTG4 filling rate at 90/180MHz
- Many RTG4 Warning Notices issued with Microchip collaboration



Constellation launch to be completed this year

- 2 launched 2021
  - **Already in commercial service**
    - Flight proven, TRL9
- 2 to be launched end-2022 by new VEGA-C (dual launch)

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State of the art Mass Memories – CO2M PDHU

Stand alone Mass Memory

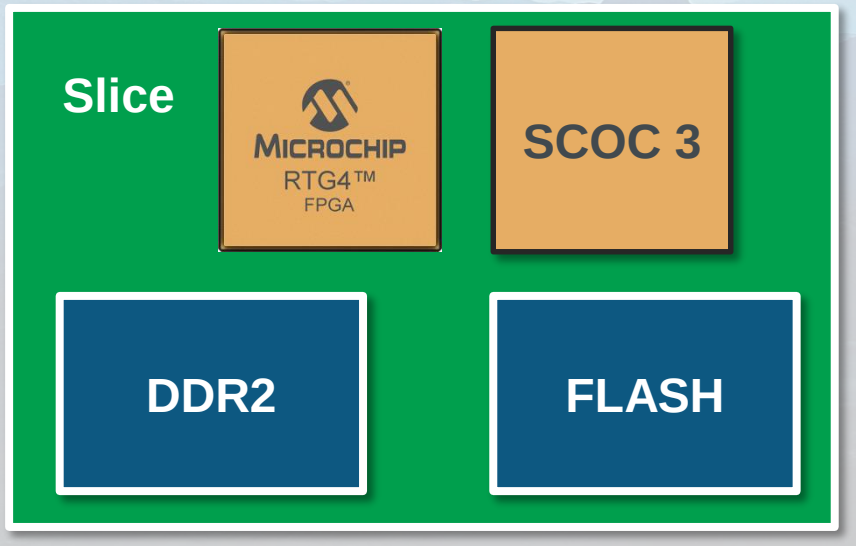
- NEMO2 family
- 2 identical slices

Microchip RTG4-based

- Reprogrammable for other missions

SCOC3 (LEON 3 SoC) based

- Reprogrammable for other missions



Flight proven 2nd generation of MM technologies

Flight proven technologies

Class1 qualification of commercial components :

NAND flash memory 256Gbit

Reprogrammable FPGA

NEMO2

CCGA 472, pitch 1,27mm

CCGA165, pitch 1mm

HDI board

BGA143, pitch ,27mm
BGA 100, pitch 1mm

BGA676, pitch 1mm

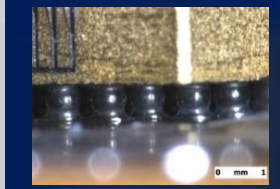
CORECI 2

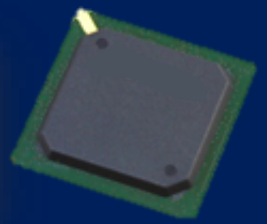
Strong heritage on **CCGA assembly** qualification up to CCGA 1657

HDI (high density interconnection) printed circuit board technology to answer high pin count package (CCGA1657) and small interconnection (BGA100)

Assembly qualification of different **plastic BGA** packages

2nd generation of Mass Memories technology pack





Next generation of Mass Memory Systems

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Next generation Mass Memory Systems

Are considering :

- **The improved performance of future instruments in all areas**
  - Optical EO and Radar EO
  - Science & multispectral instruments
- **The performance of future communication solutions / infrastructures**
  - Downlink capabilities and ISLs
- **The needs from on board processing**
  - Autonomy, reactivity
- **The necessary competitiveness**
  - At equipment and at satellite level
  - The cost of developing high performance Mass Memory Systems is very high and needs to be levered on several business areas
- **The European independence**
  - Sustainability of European technologies
  - Autonomous access to export markets

Next generation of High End Mass Memory Systems are :

- **Increasingly high in performance and complexity**
- **Critical to future missions**

Next generation Mass Memory Systems

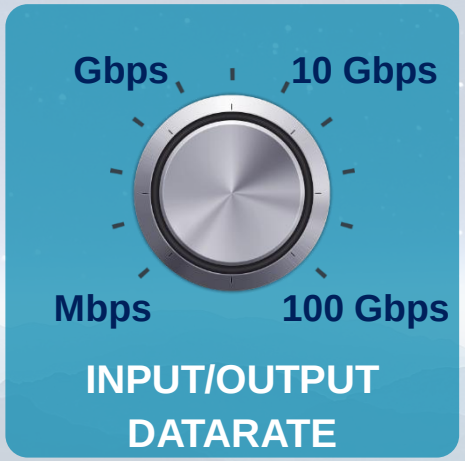
- **Expected gap in performances, compared to state of the art :**
  - **Data rates** **x 3 ~ 6** -> Toward 100's Gbps I/O datarates
  - **Storage Capacity** **x 4 ~ 16** -> Toward 100's Tb storage
  - **Storage computing x 4 ~ 6** (versus couple RTG4 + LEON3)
  - **Enabling advanced on-board data processing** and AI
- **Reliable mission data**
  - Radiations immunities, SEL, SEU, SEFI, SET
  - Data retention - read/write cycles to EOL, for various missions > 8y in LEO
  - Secure data access

- **Expected to fly by 2028**
- **Requires to focus on a new technologies and components pack**

Next generation Mass Memory – a large variety of mission needs

…With very large variety of key characteristics :

INPUT/OUTPUT LINKS



INPUT/OUTPUT DATARATE

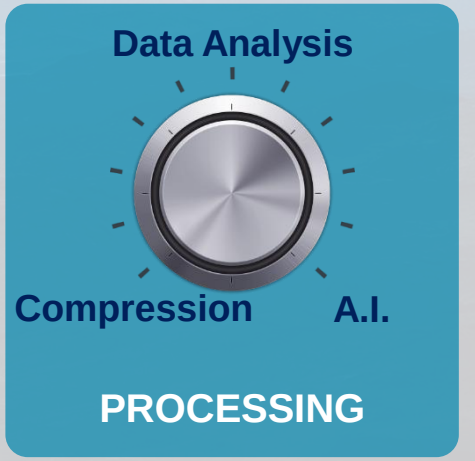
STORAGE CAPACITY

CONTROL

MISSION PROFILE

DATA RETENTION

R/W CYCLES



PROCESSING

INTEGRATION

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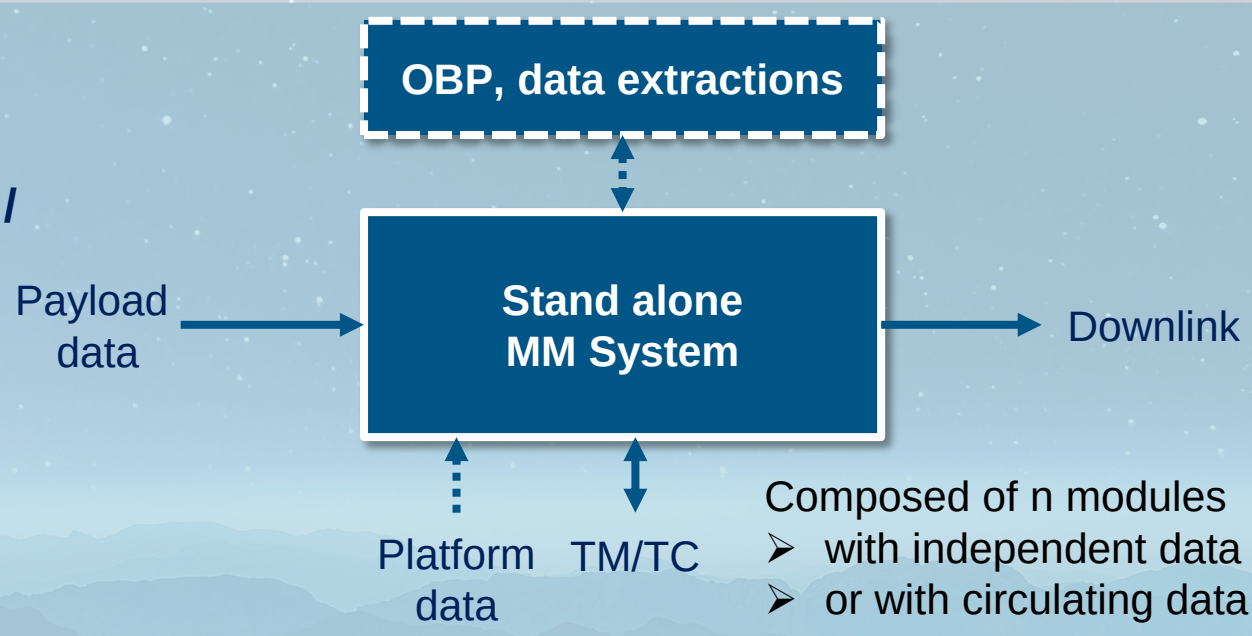
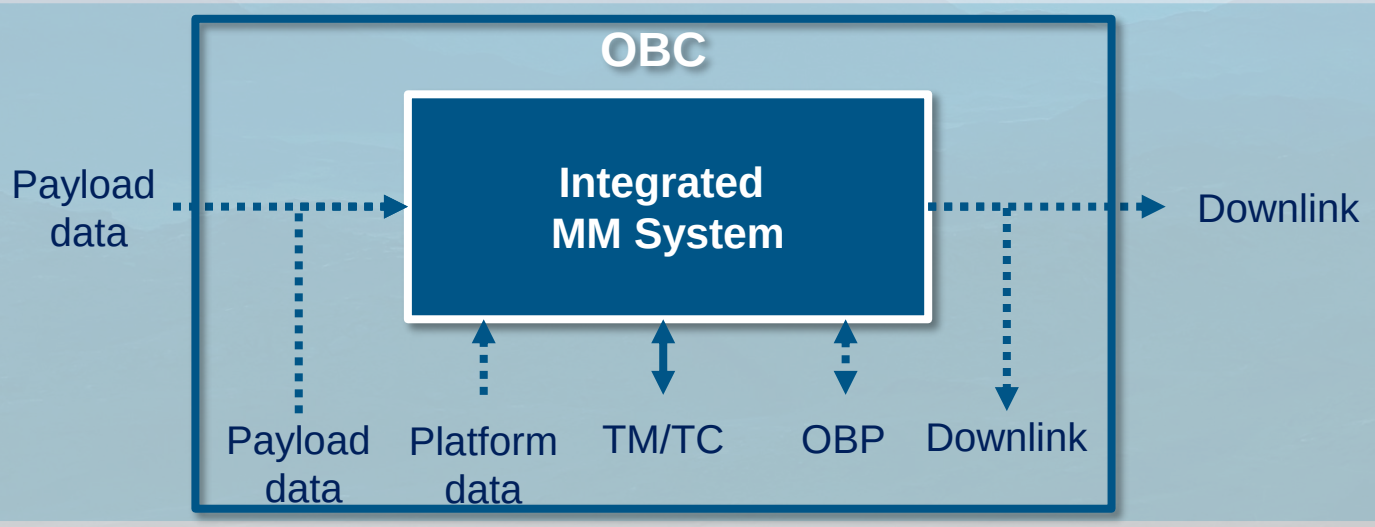
Next generation Mass Memory – a versatile architecture

Payload data storage / replay + File server for OBP



Various Use Cases In integrated OBC configuration



- **Various use cases**
- **Single hardware module**

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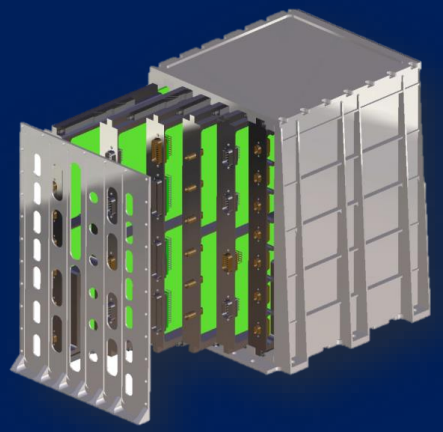
Next generation Mass Memory – a versatile architecture

- **Toward a standard modular form factor**
  - Common standard and form factor at least covering the next generations of
    - Mass Memory Units
    - On board computers
- **Additional versatility needed for maximizing the links adaptation**
  - Covering the main competitive markets
- **Common part selection and design addressing the different demands of quality-classes**



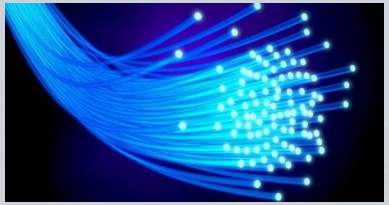
Next generation Mass Memory – performance enablers

❖ RAM memory

- ➢ SDRAM was used in the first generation (CORECI-1)
- ➢ DDR2 is flying in the current generation (CORECI-2)
- ➢ **DDR4 is required for the 3rd generation**
  Necessary for high speed data buffering

❖ High speed interfaces

- ➢ The current generation is based on copper links
- ➢ **The 3rd generation will need to introduce optical links capabilities (at the Inputs and Outputs)** : optical transceivers & connectors will be introduced



- ➢ SpFi has interesting resilience mechanisms to make it suitable for interfacing high speed rate data in and out of the Mass Memory Systems (in a point to point mode or as demonstrated in the Hi-Side H2020 project in a payload networking concept).

Next generation Mass Memory – performance enablers

New FLASH component

- Not just a drop-in replacement with a newly qualified part !
- Under the hood, each technological step increases complexity
- IO dynamic impedance calibration
- IO dynamic timing adaptation
- Data randomization
- Multi-pass programming
- Parametric control depending on temperature
- Higher BER : higher ECC requirements

	CORECI 1	CORECI2	3rd GEN
Capacity	10’s Gb/chip	100’s Gb/chip	x Tb/chip
Datasheet	70 pages	170 pages	> 300 pages
Commands	~20	~30	> 50
ECC required (BER)	2×10^{-4}	2×10^{-3}	10^{-2}

Evolution from SLC to Pseudo SLC / TLC

Requires the right investigations to mastering for usage in space

Mitigation technics to be setup accordingly

Next generation Mass Memory – performance enablers

❖ Processing capabilities (both HW and SW) are required for :

- ➢ Inputs / outputs protocol management
- ➢ The FLASH controllers
- ➢ The file systems management
- ➢ The file server management
- ➢ The file transfer management
- ➢ The storage computing (compression, data extraction,…)
- ➢ The security management (cyphering,..)
- ➢ …

❖ Processing selection

➢ The actual flying generation is based on a couple of components :
the RTG4 (~150k FF @ ~100 MHz) + the SCOC3 (LEON3 @ 80MHz)

➢ **The next generation will be based on a unique NG-ULTRA SoC, selected :**

- **For its performance** (~500k FF @ ~150 MHz + 4xARM Cortex R52 @ 600MHz)
- **For its intrinsic hardening (Rad-Hard by design)**
- **For its unicity in addressing the European independence necessities**

- **A SoC combining a high performance FPGA and SW capabilities is necessary**
- **Europe shall dispose of suitable chip and technologies**

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Next generation Mass Memory – performance enablers

❖ Other technologies enablers

- ➢ PCB material suitable for high frequency signals routing
- ➢ High Speed signal routing technics and processes
- ➢ Secondary power distribution based on GaN-FET for power performance and capacity
- ➢ Standard Rack and PCB connectors (pressfit) for the board modularity standard

- **The new generation is linked with a package of technologies transitions**
- **Coherent with next generation of OBCs**

Airbus Space Electronics Mass Memories Roadmap

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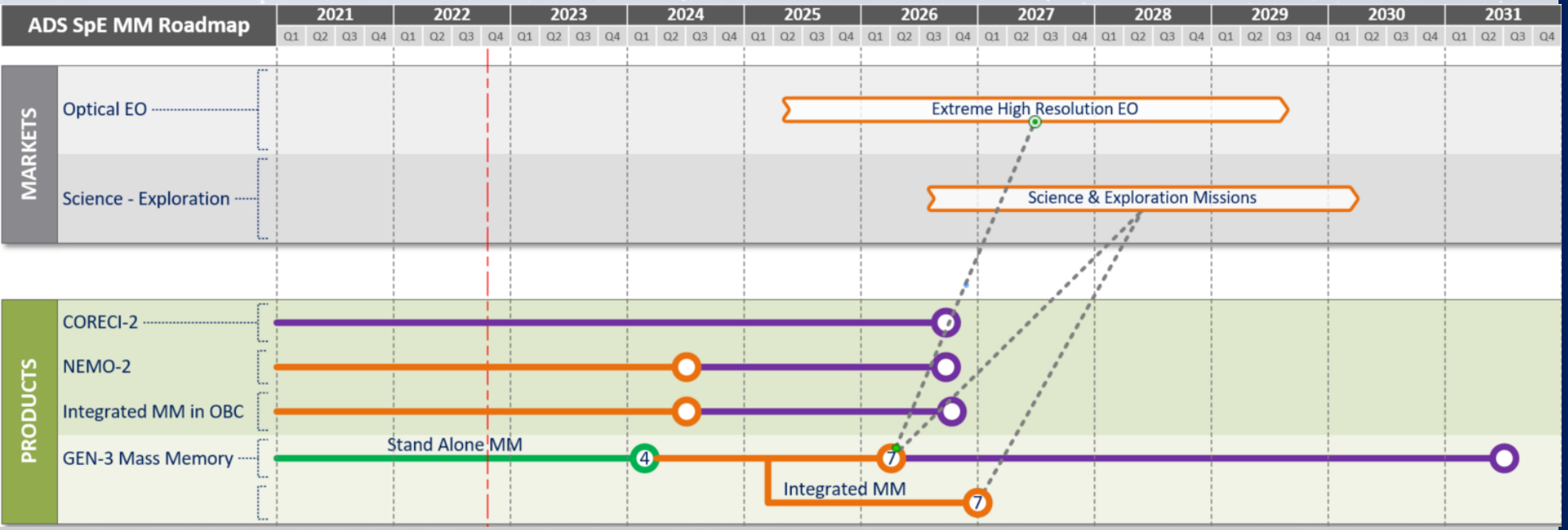
Airbus Space Electronics MM Roadmap

- ❖ **Generation 2 of Flash MM will cover short term market needs**
- ❖ **Generation 3 memories under preparation**



- **Technology development coherent with other product lines development**
- **New modularity applied**
- **Key components :**
  - **NG-Ultra**
  - **NG Flash (TLC)**
  - **DDR4**

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Thank you

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