Innovations in electrical interfaces for visible imaging sensors to support future big data and high-speed missions.

ADCSS – ESTEC in Noordwijk, Netherlands Oct. 25th – 27th, 2022

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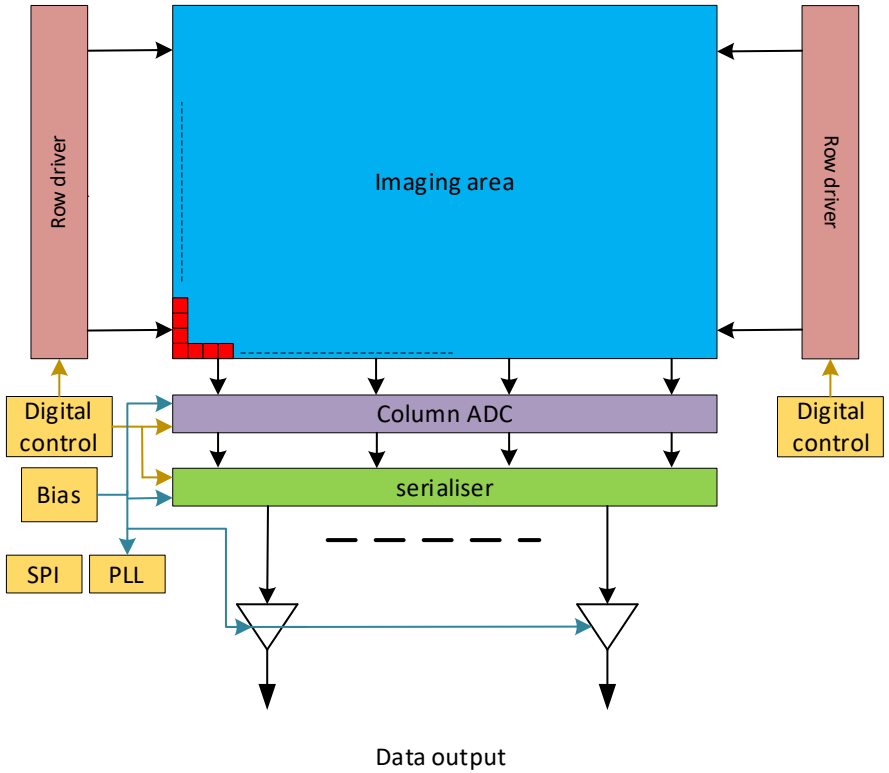
Motivation

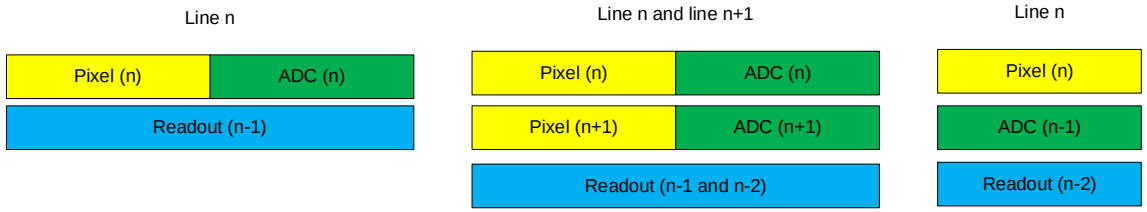
CMOS detector electrical interface becomes more and more important:

- As the electrical-optical performance becomes more mature the focus can move to other improvements
- Higher frame rates
- Higher quantities of data to be output by larger pixel areas and new features
- Improve ease of integration at system level

Context

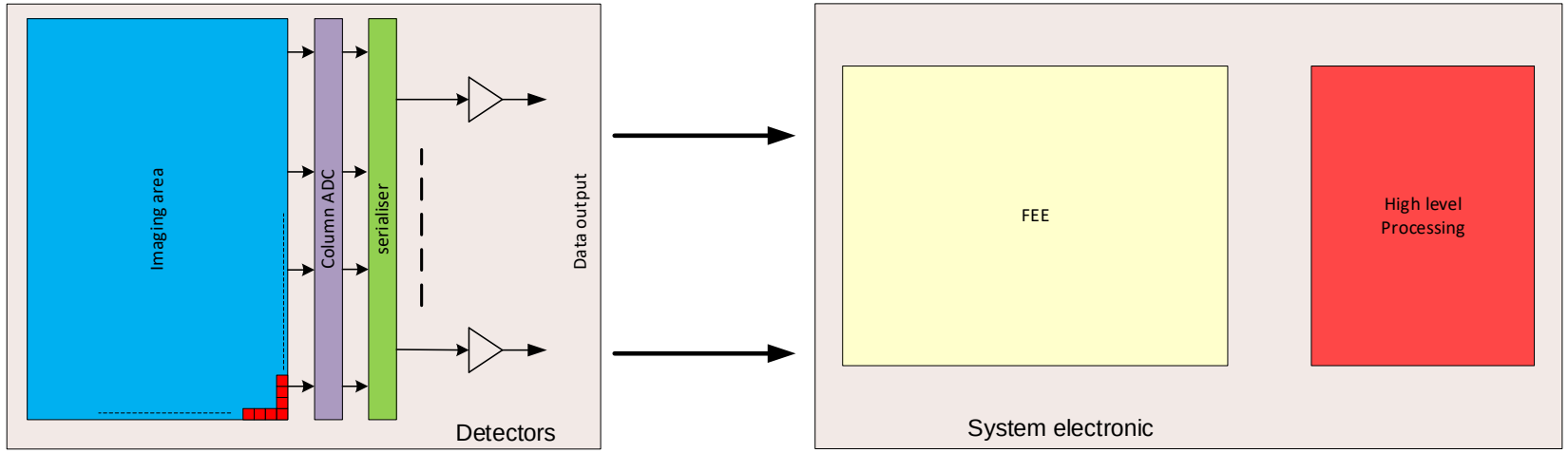


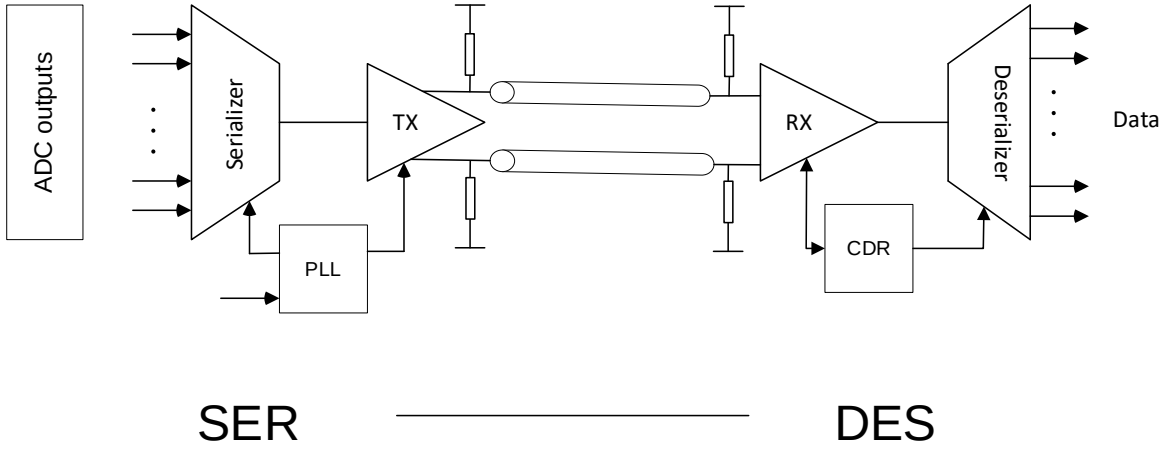
Simplified readout timing



- Frame rate and amount of data have drastically increased.
- Effort was put on Pixel, ADC and readout timings
- As an example some devices have a rate of 80 Gb/s
- Then electrical interface took huge importance to improve:
  - Speed
  - Power consumption
  - System integration
  - Silicon area

SERDES solution

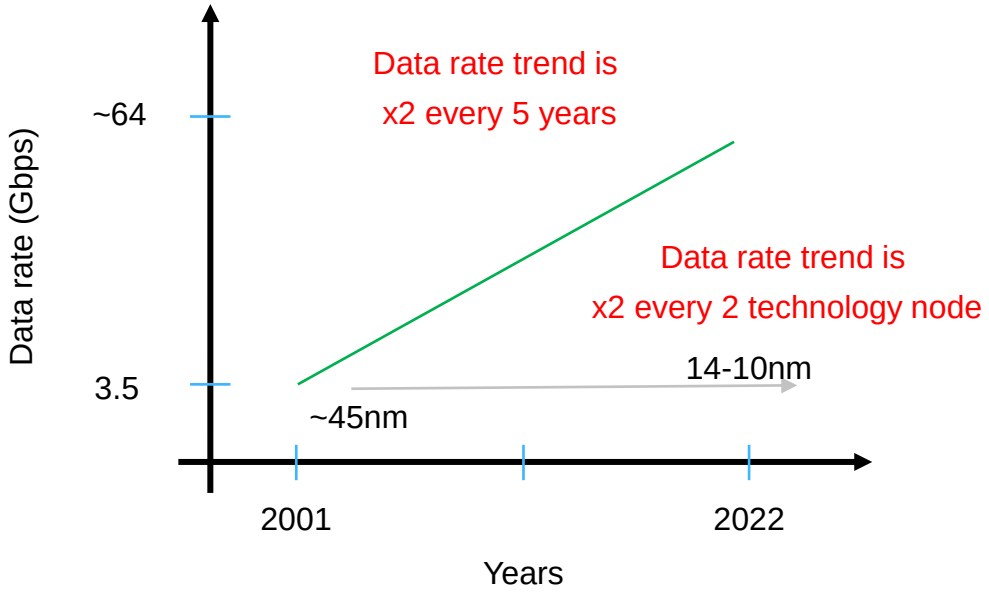




Serialize from all columns to few outputs to trade:

- Bandwidth
- Number of outputs drivers
- Power consumption
- Silicon area

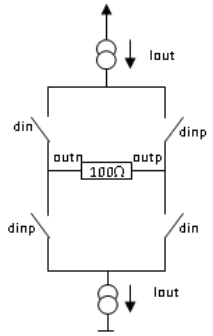
Data rate trend



- Today the maximum data rate per output is 64 Gbps
- This needs to go small technology nodes not always compatible with pixel performance and price point
- However, today using a 180 nm node more compatible with pixel performance requirements we can still have data rates up to 4 Gb/s
- To address cases such as 80 Gb/s we will implement multi TX outputs.

Driver choices

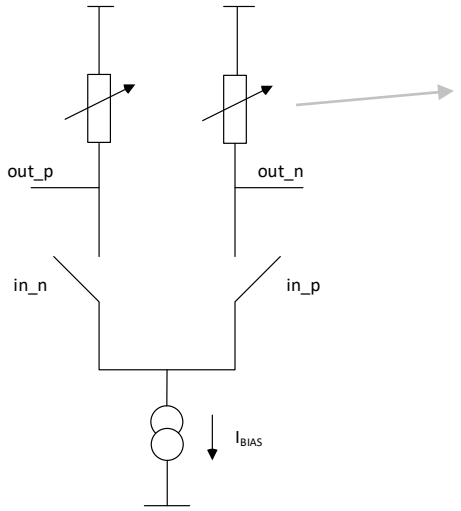
Low frequency < 500 Mhz



Two standards (there are more):

- Common Mode ~1.25 (LVDS)
- Common Mode ~0.9 (sub-LVDS)
- Limited to 1Ghz

High frequency > 500 Mhz and up to 4Gb/s

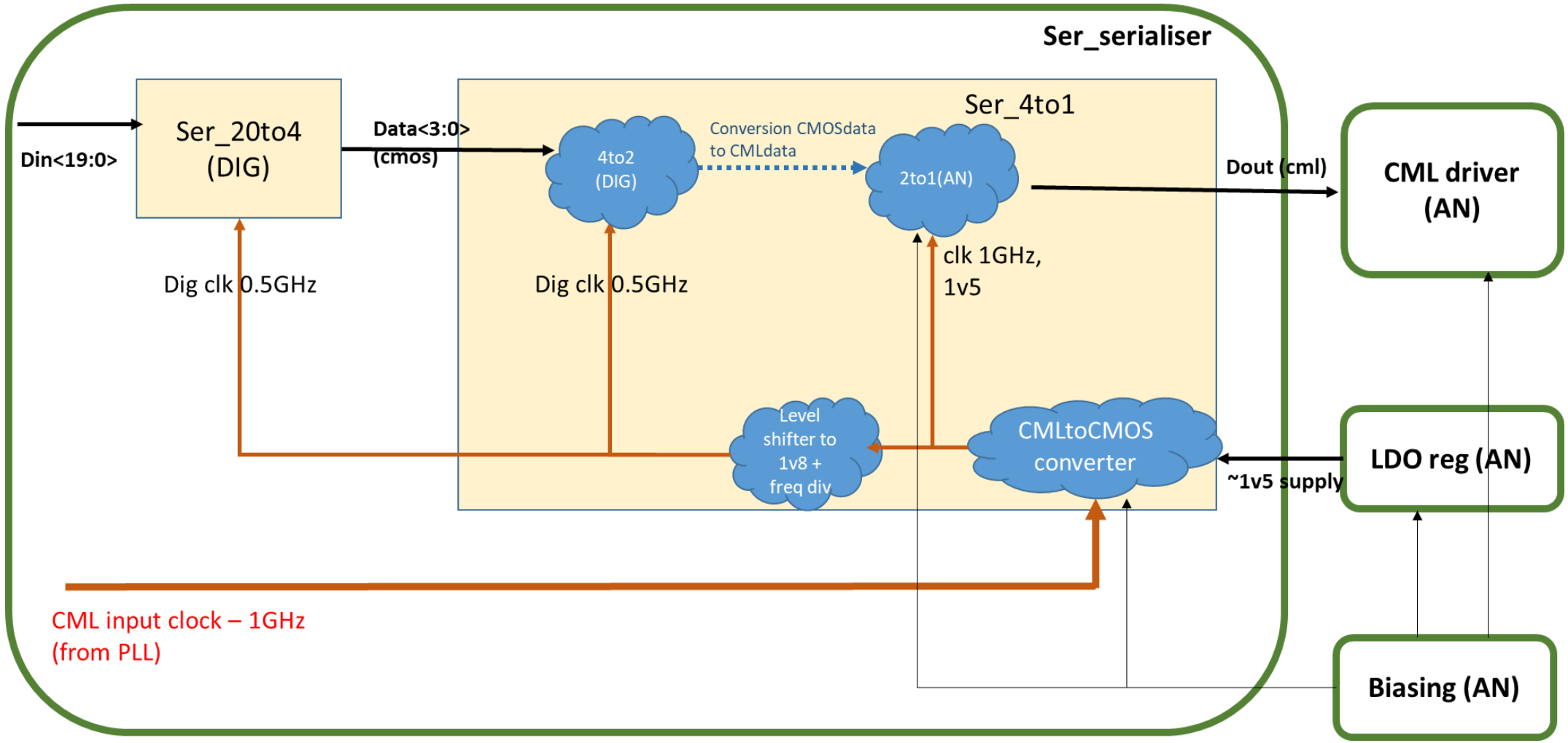


Adjustable Common mode and voltage swing.

At high frequency CML drivers enables

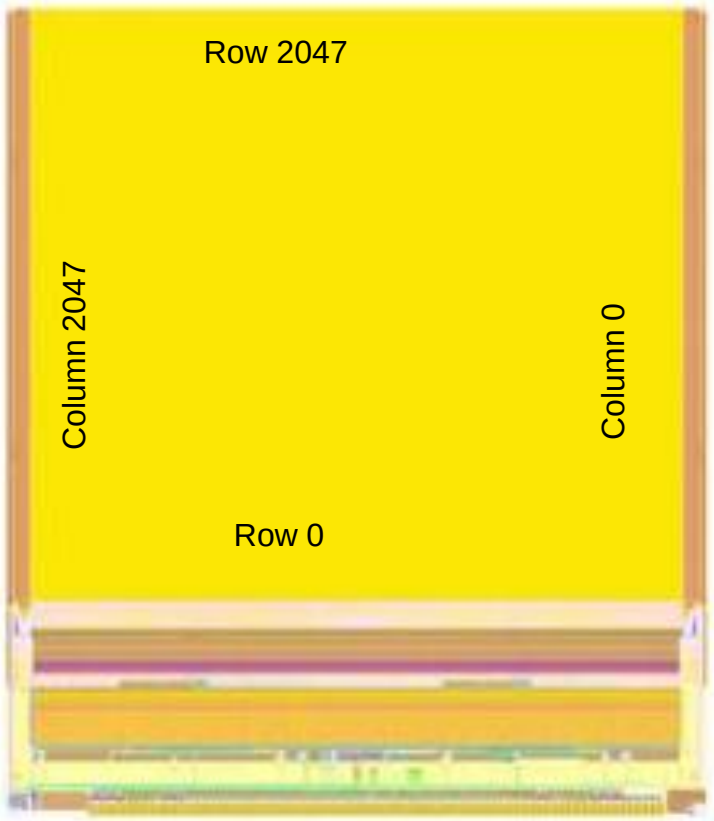
- Lower number of drivers
- Lower pin count
- Lower power
- Lower silicon foot print

Block diagram using CML drivers



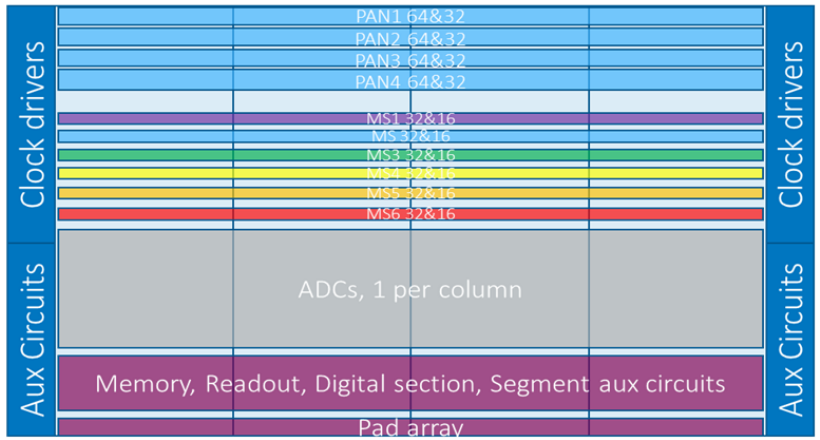
CIS120

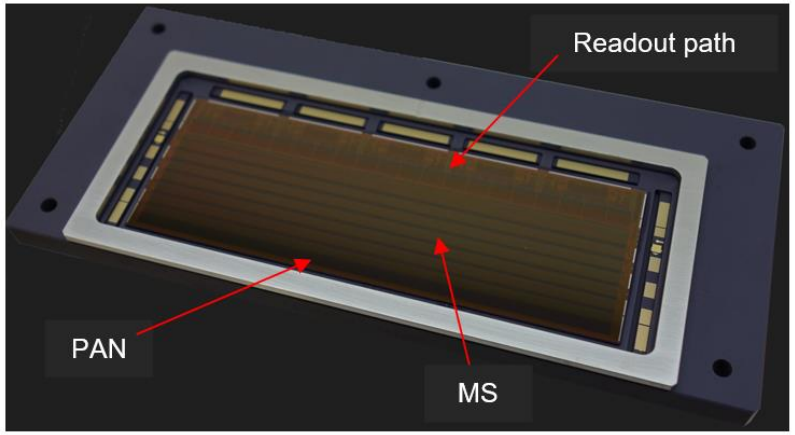
Format	2048 x 2048
Pixel pitch	10 µm
Die size (width x height)	22.2 x 28.35 mm
Outputs, LVDS or sub-LVDS	4 data + 2 sync
Output data rate	260 Mbps/channel
Setup and control bus	SPI
Power supplies	3.3V and 1.8V
Clocks	4 MHz and 130 MHz
ADC resolution	8, 10, 12 or 14 bit
Operating mode	Rolling shutter, Global shutter & global shutter with DDS
Version	Back Illuminated



CIS125 CCDonCMOS

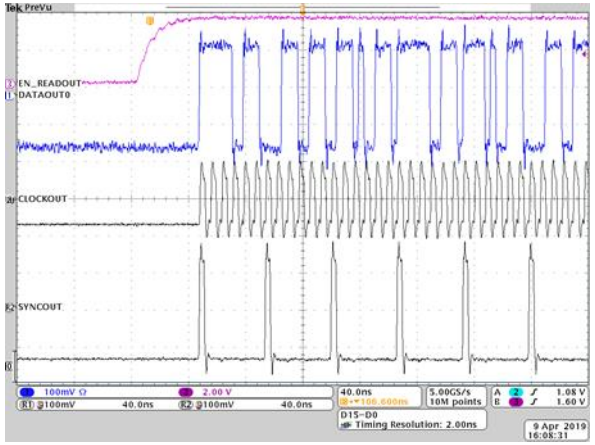
TDI charge domain





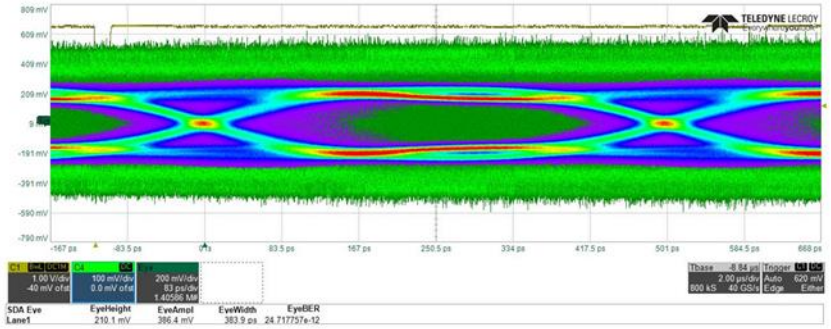
Pan Channels	4 pan – each made up of 2 sub TDI pan: 64 lines and 32 lines
MS Channels	6 MS – each made up of 2 sub TDI MS: A & B 32 lines and 16 lines
Pixel pitch µm	5µm Pan, 10µm MS
Number of pixels	Pan: 16k columns MS: 8k columns
Full Well Capacity (per pair)	Pan: 60ke$^-$ MS: 240ke$^-$
Max. Line Rate	Up to 30 klines/s depending on configuration (55 klines/s with customisation)
Read-out speed at max. line rate	2.0 Gbit/s
Other features	Antiblooming Radiation Tolerant

LVDS and CML



CIS120 – LVDS SERDES at 260Mb/s

Data and clock generation

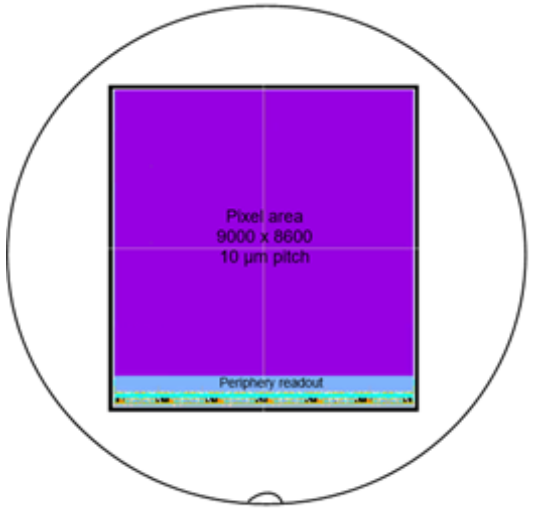


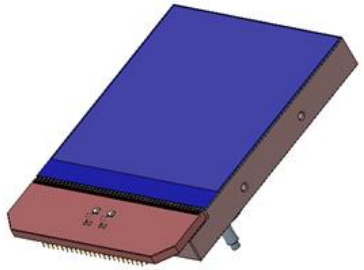
CIS125 – CML SERDES at 2Gb/s

The data stream format includes per line:

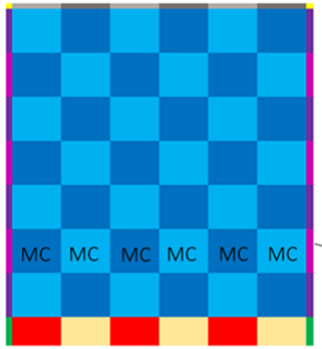
- A word to indicate the start of line (SOL)
- A word to indicate the line readout and other relevant information
- The image data
- A CRC word
- A word to indicate the end of line (EOL)

CIS300 – Large area detector family

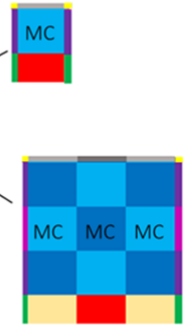




CIS301 & CIS302

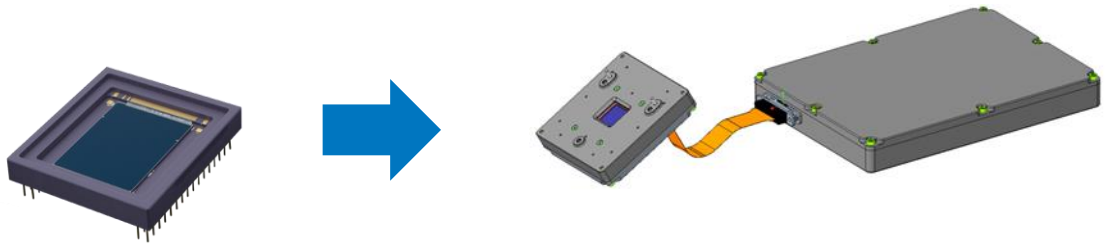


10µm pixel pitch			
MC segments	Number columns	Number rows	Frame rate (fps)
1:1 unit	1500	1500	51
2:2 units	3000	2920	26
3:3 units	4500	4340	18
4:4 units	6000	5760	13
5:5 units	7500	7180	11
6:6 units	9000	8600	9
6:7 units	9000	10020	8
7:7 units	10500	10020	8
7:8 units	10500	11440	7



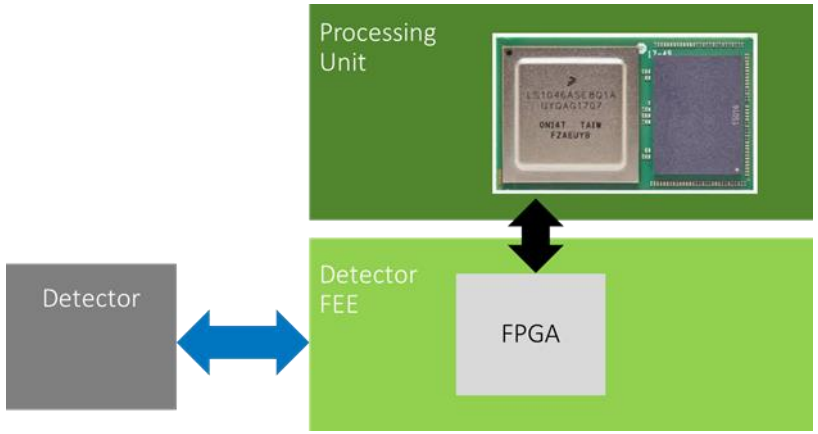
Parameters	CIS301 and CIS302
Pixel pitch	10 µm
Array size	9000 columns x 8,600 rows
Pixel type	Pinned Photodiode, Switchable dual gain
Operating Modes include	Rolling Shutter HDR (High Dynamic Range) Global Shutter Staircase (multiple non-destructive reads)
ADC bits	Selectable 12 or 14 bits
Frame rate	8 fps @12 bits (Rolling shutter) 8 fps max @ 12 bits (Simple Global shutter) 4 fps max @ (Global Shutter with Digital Double Sampling (DDS))
Region of Interest	Capable of selecting region of interest in row and column directions - freedom to select any or all combinations of adjacent odd and even rows - can select from the 12 outputs to use to select different groups of columns
Multiple Gain settings	Any combination of pixel and pre-amplifier gain: Pixel gain: x1, x10 Pre-Amplifier gain: x1, x3, x7, x15, x31
Full Well Capacity	> 140 ke$^-$ (lowest pixel gain setting) > 15 ke- (highest pixel gain setting)
Noise	< 2 e$^-$ (high gain rolling shutter) < 5 e$^-$ (high gain global shutter) < 30 e$^-$ (low gain rolling shutter)
Dynamic Range with HDR operation	95dB typical
QE @550nm	95% (dependent on anti-reflection coating)
Dark Current	0.01e-/s @-50°C Dark current halves for every reduction of 5-6°C
Interface	12 CML outputs 50 MHz Master Clock SPI
Package/chip format	Three side buttable, silicon carbide package
Power Dissipation	6 W (at full frame rate) Low power mode exists (down to < 2W).

FEE and system in package



CIS120 – Processing level 0:

- FEE based FPGA platform
- Low level processing (DS offset; GS DDS, Gain and offset …)
- Spacewire/Spicefibre



CIS125/CIS300 – Processing level 1:

- Advance data processing platform
- FEE based FPGA included
- Edge computing
- Spacewire/Spicefibre

Summary

Detector electrical interface becomes more and more important:

- Higher frame rate
- Higher quantity of data

Teledyne e2v has silicon proven SERDES based LVDS and CML up to 2 Gb/s per video channel.

SERDES approach (including data stream) enables high data rate easy to integrate at FEE level.

Next step is further integration:

- Front End Electronic
- Processing capability

Acknowledgement

- The author gracefully acknowledges the support of the Teledyne e2v team

THANK YOU