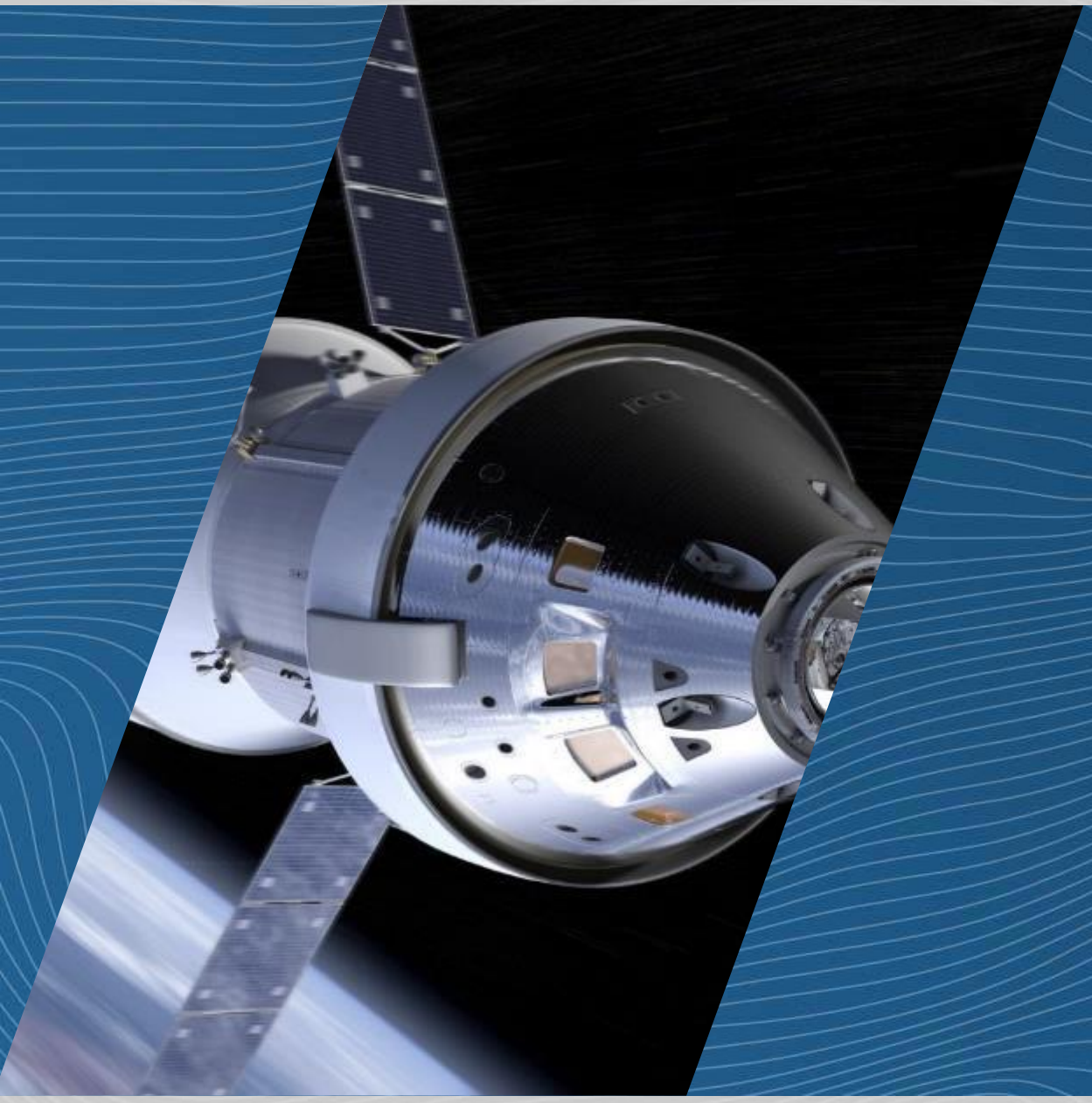


CAES PIONEERING ADVANCED ELECTRONICS

GR740, GR765 and GR7xV: SPARC and RISC-V for On-Board Computing

2022-Oct-27

CAES PIONEERING ADVANCED ELECTRONICS

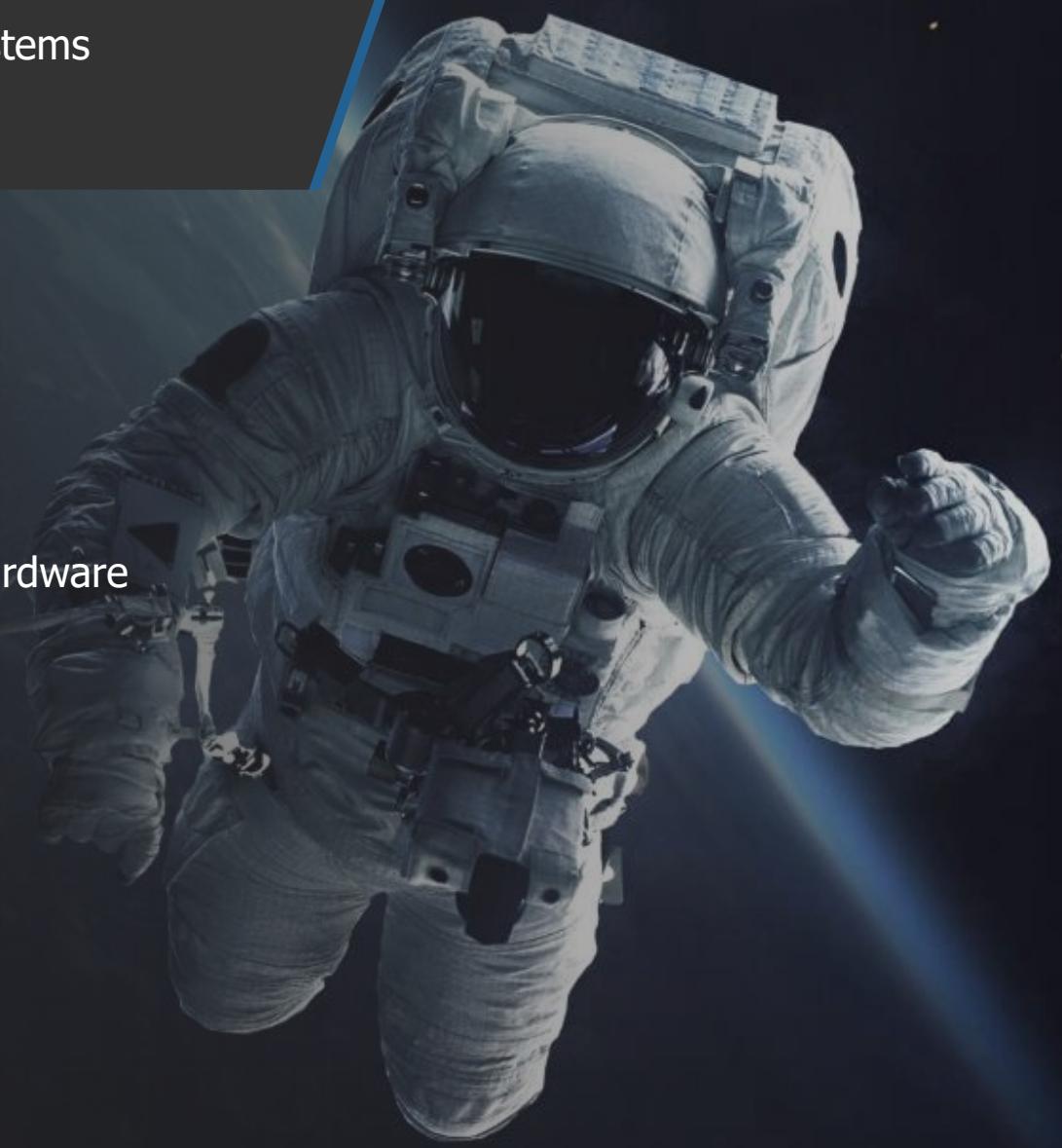
A world leader in embedded computer systems for harsh environments

Experts in fault-tolerant computing

We provide a full ecosystem to support hardware and software design for:

- Standard components
- Semi-custom FPGA
- Full custom ASIC

Based on SPARC and RISC-V architectures



Computing Roadmap – 2022, September

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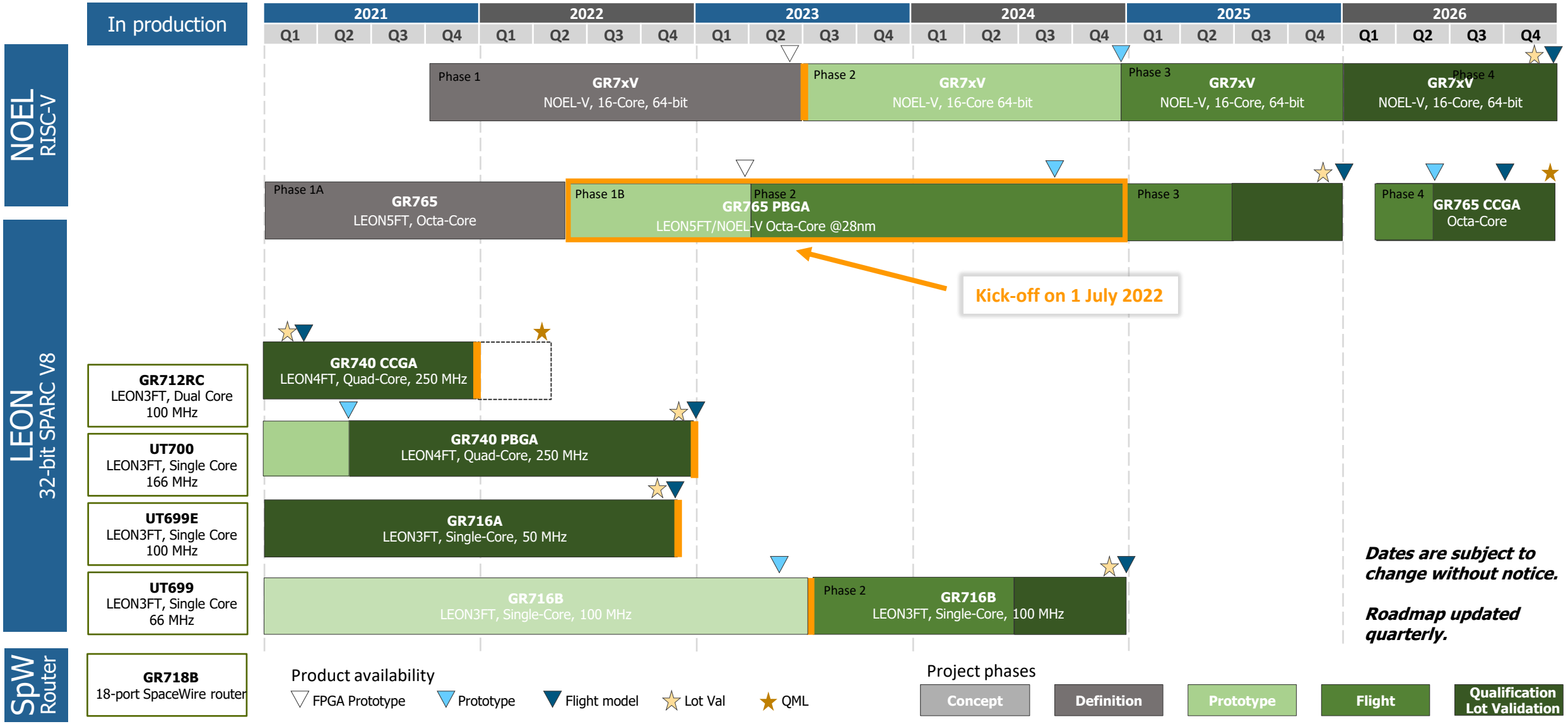

Computing Roadmap – 2022, September

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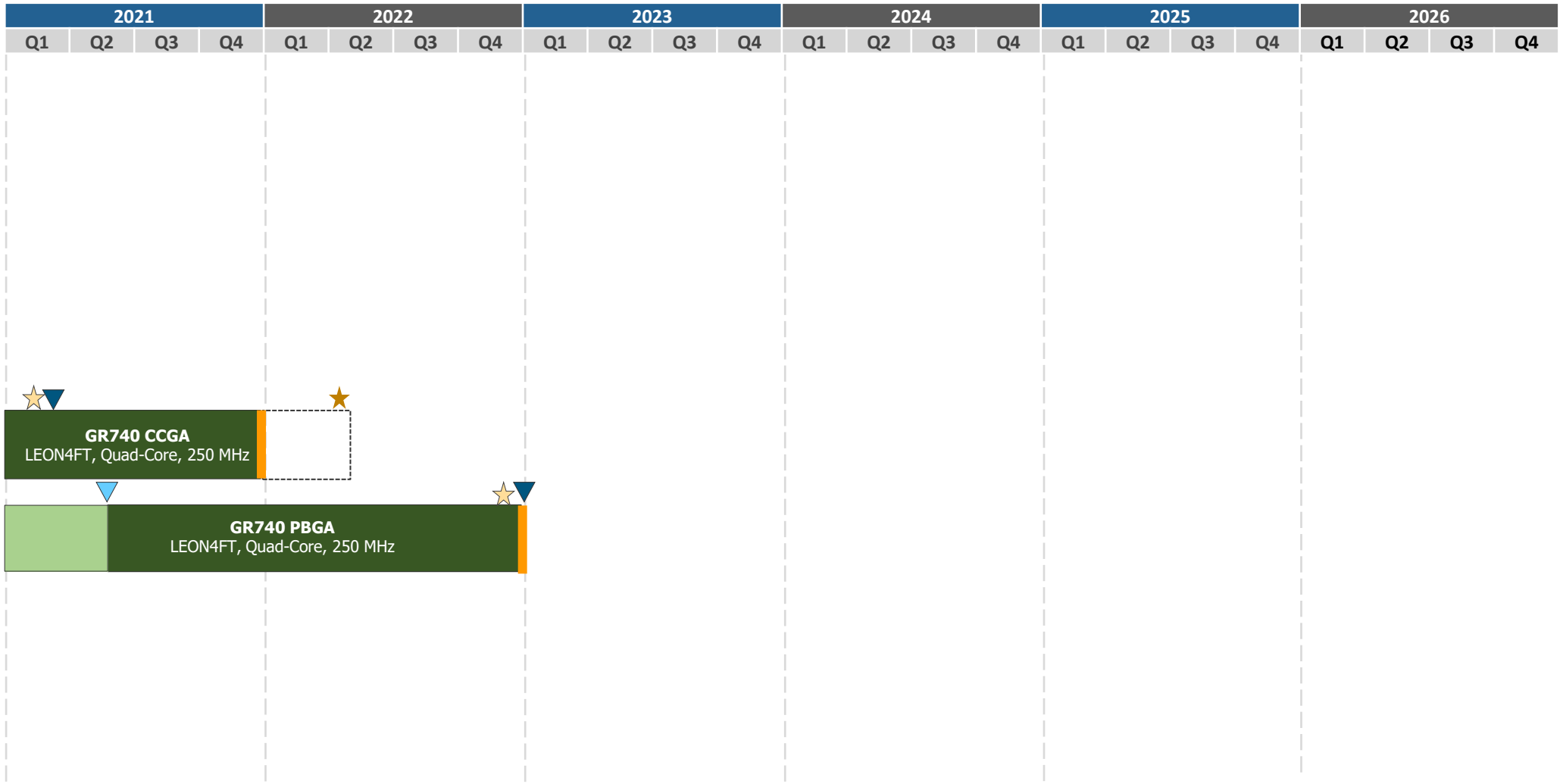
In production

NOEL RISC-V

LEON 32-bit SPARC V8

SpW Router

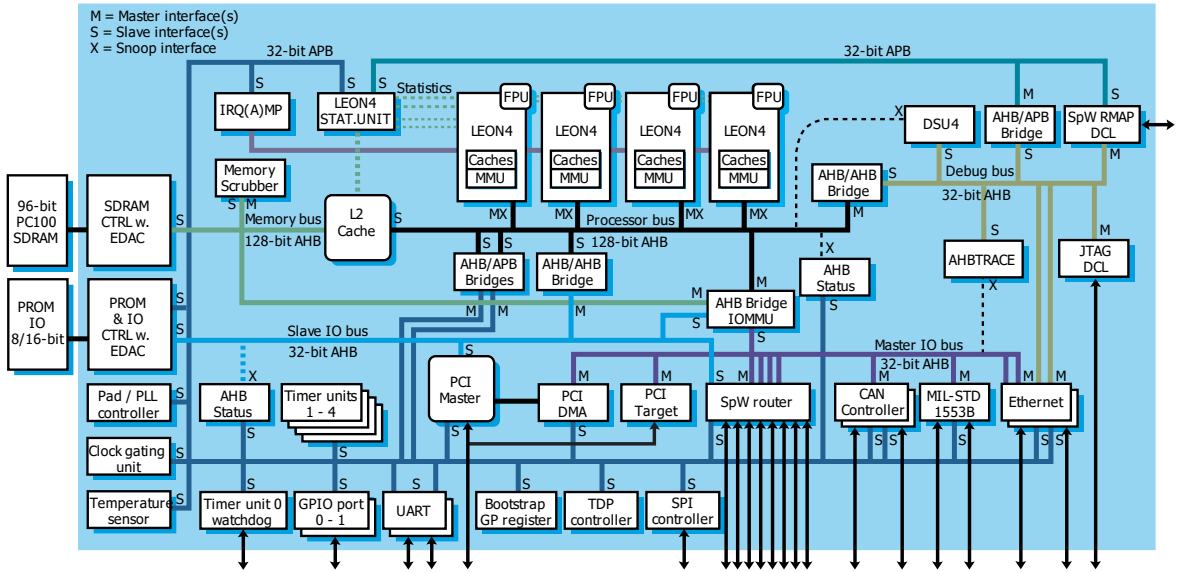


GR740 - Quad-Core LEON4FT Processor

CAES PIONEERING ADVANCED ELECTRONICS

Fault-Tolerant Quad-processor SPARC V8

- High performance, wide range of interfaces
- SPARC V8 compliant, Radiation-hard and Fault Tolerant
- Designed as ESA's Next Generation Microprocessor, NGMP
- LEON Technology – re-use of Development and Software ecosystem
- Low risk, off-the-shelf product
- Excellent performance/watt ratio
  - Very low power, < 3 W (core typical)
  - Performance 1700 DMIPS (1000 MIPS)



STANDARD MICROCIRCUIT DRAWING	PREPARED BY: Phu H. Nguyen	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime	
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE	CHECKED BY: Phu H. Nguyen		
	APPROVED BY: Muhammad A. Akbar	MICROCIRCUIT, PROCESSOR, DIGITAL, CMOS, RADIATION HARDENED, QUAD CORE LEON4 SPARC V8 PROCESSOR, MONOLITHIC SILICON	
AMSC N/A	DRAWING APPROVAL DATE: 22-04-18		
	REVISION LEVEL	SIZE: A	CAGE CODE: 67268 — 5962-21204
		SHEET: 1 OF 51	

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esa LEON SPARC Compliant SCD V8

Computing Roadmap – 2022, September

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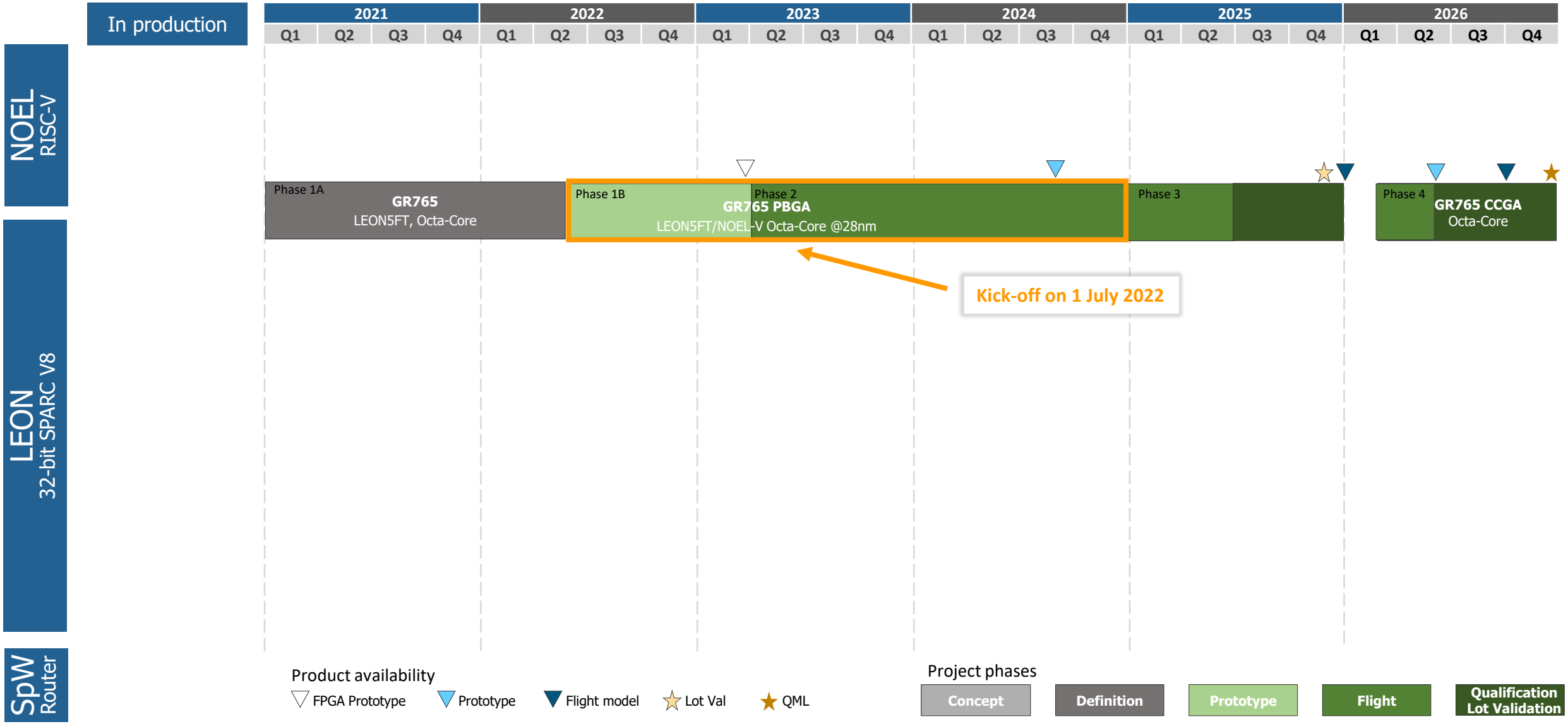


GR765 – Overview

- **Phase 1A (funded): DARE65 Demonstrator** – Downsized implementation of GR765 architecture. Availability TBD for eval board with plastic parts in 2023.
- **Phase 1B/2A/B (funded): GR765-XX** – GR765 implementation. Goal is 2024 component availability. Projects started.
- **Phase 3A/B: GR765-CP/MP/MS** – GR765 product (same design as GR765-XX) with Qualification & production flows/temperature ranges available as per other CAES standard products. Availability (flight models) is TBD.
- **Phase C: GR765-*-C(C/L)GA** – Ceramic package development
- **Complemented by:** ESA Fifth Generation Space Microprocessor development

GR765 is a new component development based on an extended GR740 SoC design

The development of the demonstrator and the updates of the SoC design to form the GR765 are undertaken in ESA GSTP, ARTES Competitiveness & Growth, and NAVISP EL2 activities with funding from the Swedish National Space Agency and CAES.

Disclaimers:

GR765 Effort is on-going & subject to change without notice. Currently there is no guarantee of a product launch.

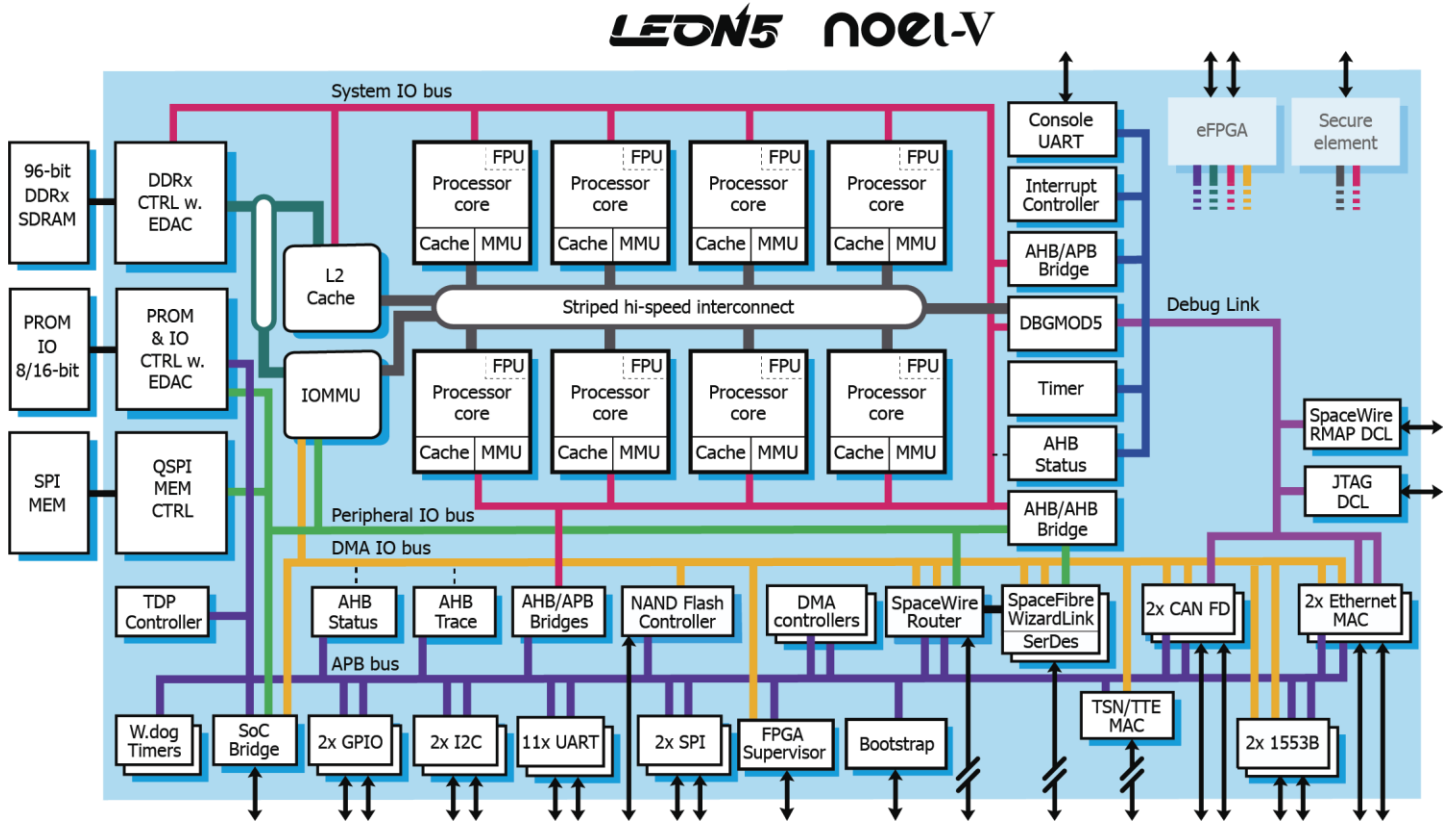
Contact Gaisler to receive the latest available information.

GR765 – Octa-Core Processor

In development
No guarantee of product launch

Baseline Features

- Fault-tolerant **octa-core** architecture
  - **LEON5FT SPARC V8 or NOEL-V RV64GCH**
  - Dedicated FPU and MMU, 64 KiB per core L1 cache, connected via multi-port interconnect
- **1 GHz processor frequency - 26k DMIPS**
- 2+ MiB L2 cache, **512-bit** cache line, 4-ways
- **DMA controllers**
- **DDR2/3 interface with dual x8 device correction capability**
- 8/16-bit PROM/IO interface
- **(Q)SPI and NAND memory controller interfaces**
- **Secure Element, providing Secure (authenticated) boot (TBD)**
- **eFPGA ~30k LUT (TBD)**
- **High-pin count – LGA1752 package allows reduction of pin sharing**
- **Target technology: STM 28nm FDSOI**



SPARC RISC-V®

Instruction Set Architectures

CAES PIONEERING ADVANCED ELECTRONICS

Why RISC-V?

- Enabling new technologies by standardization
  - Hypervisor support
  - Vector extension, …
- Growing base of 3rd party ecosystem:
  - Toolsets
  - Libraries, engines etc.
- Attractive to talent entering the space domain
- Influx of know-how by talent entering the space domain
- Hardware and software potential for future space applications: A new class of processors requires a modern architecture

RISC-V®

Why SPARC?

- Existing base of space proven HW and SW designs
- Mature ecosystem for today's space applications, e.g. qualified OS
- Accumulated development know-how in the industry
- Software backward compatible with existing LEON devices

SPARC

GR765 provides RISC-V and SPARC

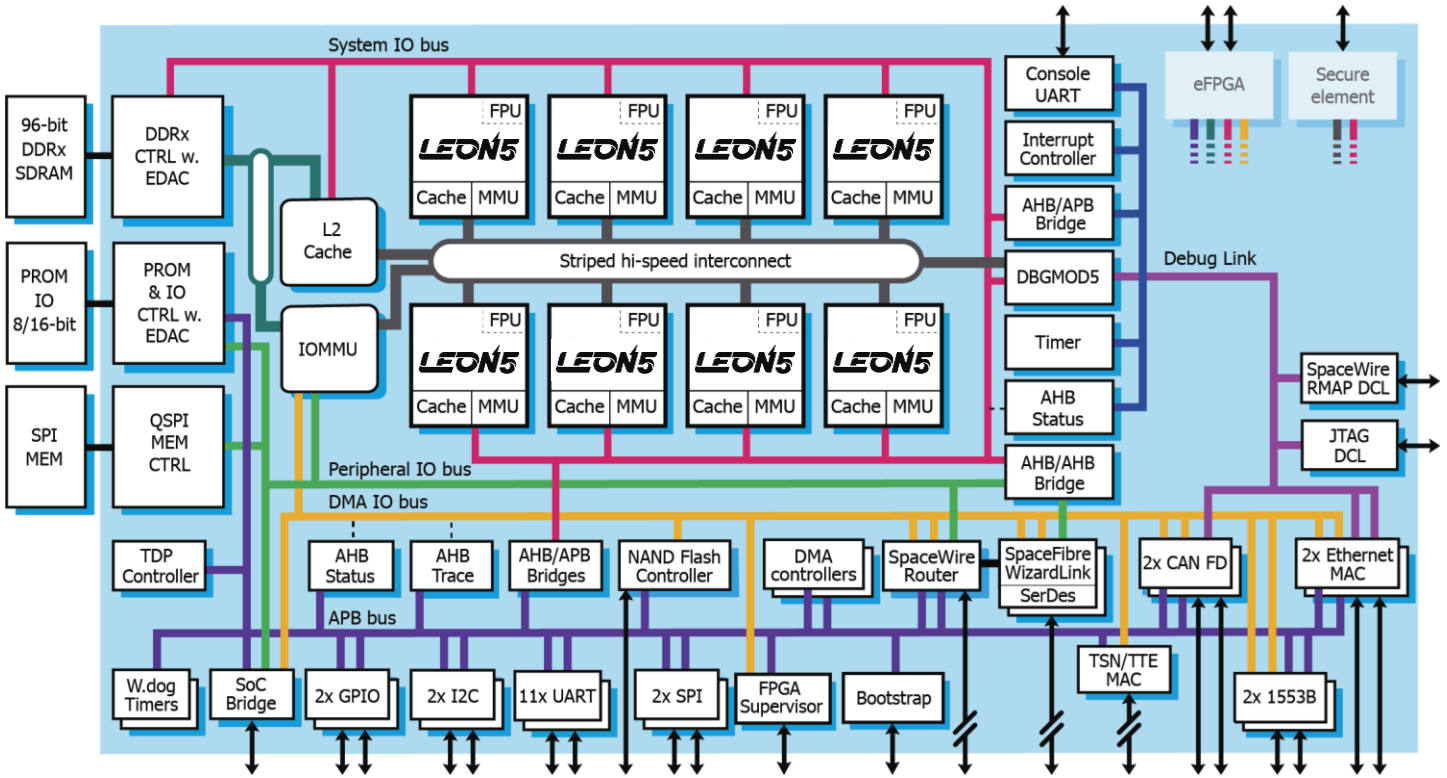
- Both architectures are needed by the industry
- Faster time-to-market for RISC-V while continuing SPARC - single component development investment and qualification effort
- Minimal silicon overhead - sharing of resources on chip. User selects CPU (LEON5FT or NOEL-VFT), device cannot operate with both at the same time.
- De-risking early stages of new application development
  - The architectural choice can be evaluated easily

GR765 – SPARC Mode

In development
No guarantee of product launch

GR765 in SPARC mode

- LEON5FT provides backward compatibility with LEON4FT/GR740 and earlier LEON implementations
- LEON5FT 8-stage integer pipeline with dual lanes, allowing up to two instructions per clock cycle.
- Improved branch prediction capabilities, choice between two-level adaptive predictor with history buffer and static prediction.
- Late ALUs allow masking latencies and enables higher throughput in processor pipeline.
- Store buffer improvements to reduce stalls introduced by store operations (improved cache controller with back-to-back stores and 4-entry store buffer).
- Improved version of the high-performance GRFPU: GRFPU5 can handle the full IEEE-754 standard including denormalized numbers as inputs and outputs.
- New FT features: L1 cache SECDED ECC allows error correction on the fly. Optional hardware scrubber for L1 and register file.

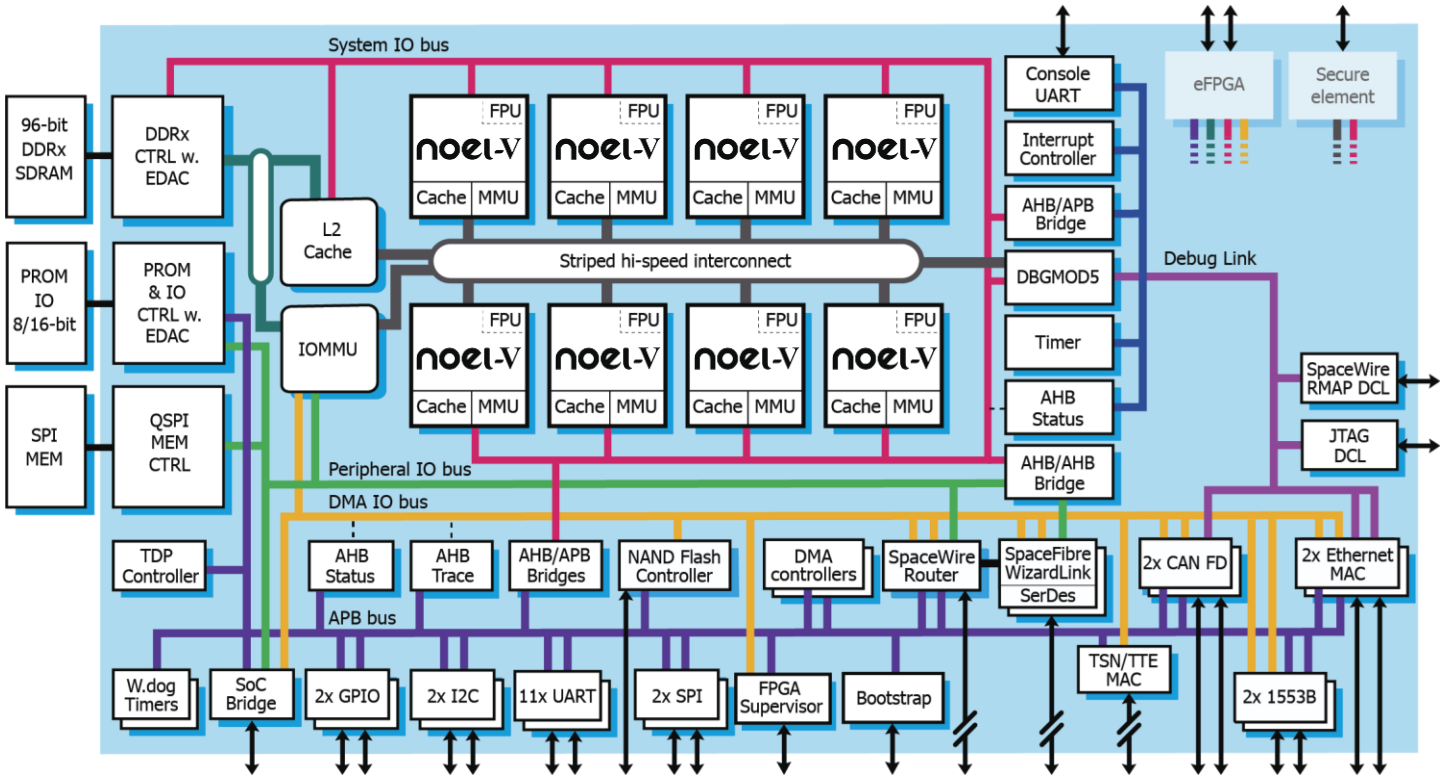


GR765 – RISC-V Mode

In development
No guarantee of product launch

GR765 in RISC-V mode

- NOEL-V processor core provides the same microarchitectural improvements as the LEON5FT
- NOELV/GR765 provides RISC-V compatibility through conformance to the OS A (Embedded) RISC-V Platform Specification
- RV64GCH – 64-bit processor
  - 64 Base integer instructions (I)
  - MUL/DIV (M)
  - Atomics (A)
  - Half/Single/Double Precision Float (Zfhmin, FD)
  - Compressed instructions (C)
  - Hypervisor (H)
  - Bit manipulation (subset of) (B)
  - Physical Memory Protection (PMP)
  - MMU - 39 bit virtual addressing, separate I and D, fully associative, TLB
- Cache control extensions
  - Cacheline invalidate, zero, etc (Zicbom, Zicbop, Zicboz)
  - Cachability in page tables (Svpbmt)
- RISC-V Advanced Interrupt Architecture (AIA)

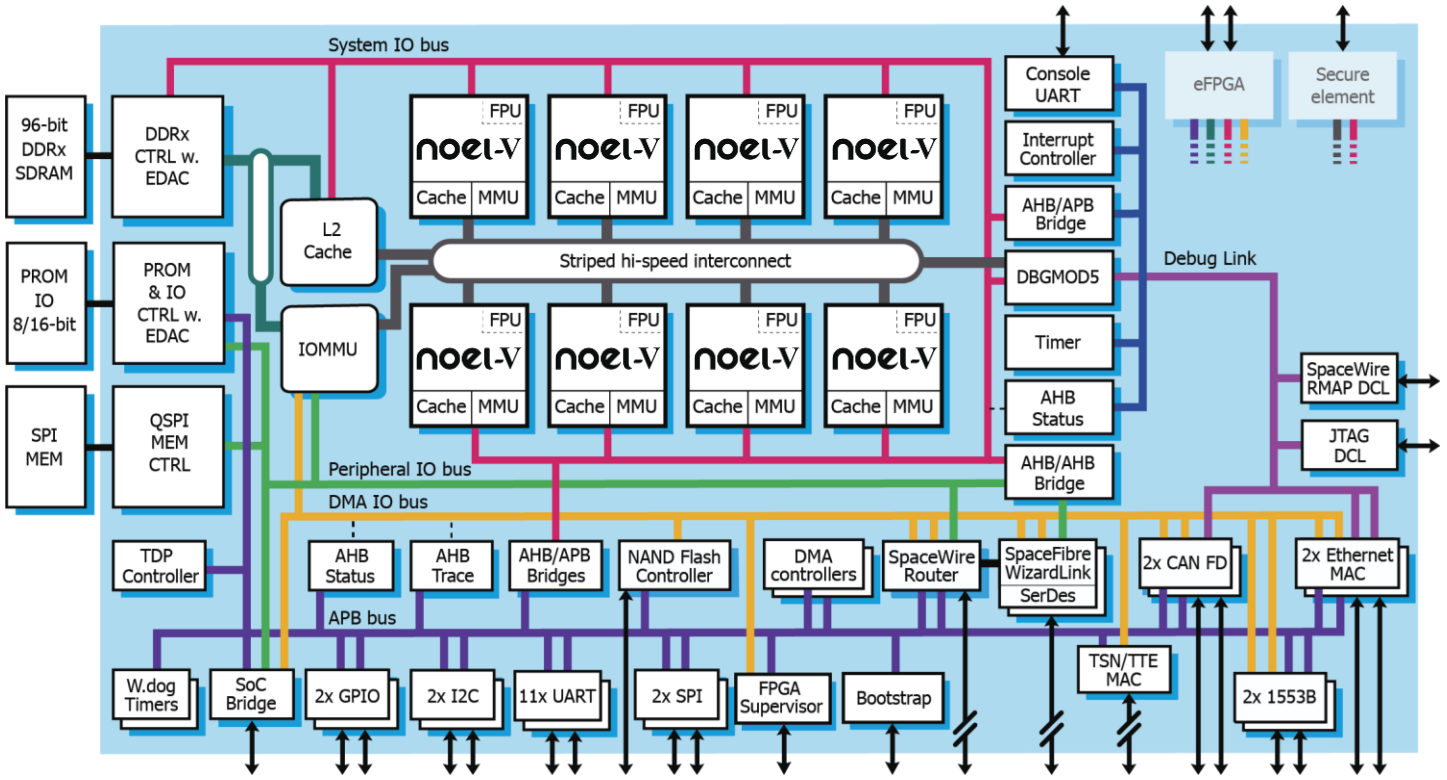


GR765 – RISC-V Mode

GR765 in RISC-V mode, continued..

- Control flow integrity (standardization ongoing)
  - Shadow stack - stack overwrites must not cause return to the wrong place
  - Landing pad - memory overwrites must not cause jumps/calls to the wrong place
- Enhanced security
  - Smepmp - enhance security by limiting what machine mode has access to
  - Smstateen - hide state that an OS/hypervisor does not know about
- RISC-V Debug Module (DM)
  - Compatible with the RISC-V debug specification
  - JTAG Debug Module Interface
  - Hart Run Control
  - GPR and CSR register access
  - Program buffer
  - Triggers
- Extended monitoring
  - Improved visibility of hardware behaviour

In development
No guarantee of product launch



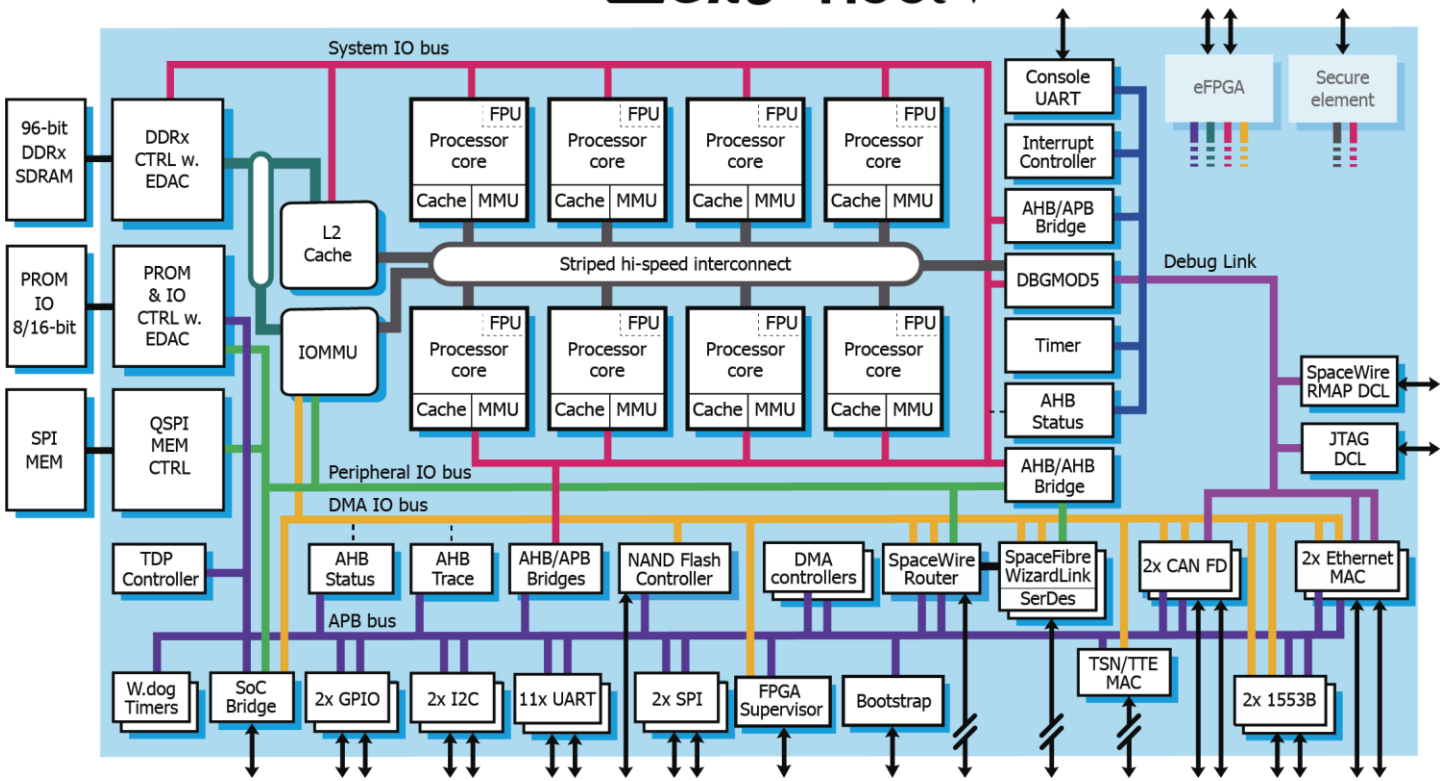
GR765 – Interfaces

Interfaces – SPARC and RISC-V mode

- **SpaceFibre x8 lanes 6.25 Gbit/s, simpler protocols**
- **12-port** SpaceWire router with +4 internal ports
- 2x 10/100/1000 Mbit Ethernet
- **2x or 3x (TBD) TT / TSN Ethernet support**
- **2x** MIL-STD-1553B,
- **2x CAN FD**
- **2x I2C interface**
- **12** x UART
- **2x** SPI controllers
- **SoC Bridge interface**
- **FPGA Supervisor interface**
- Timers & Watchdog, GPIO ports
- Debug links:
  - Dedicated: JTAG and SpaceWire
  - CAN, SpFi, Ethernet

In development
No guarantee of product launch

LEON5 noel-V

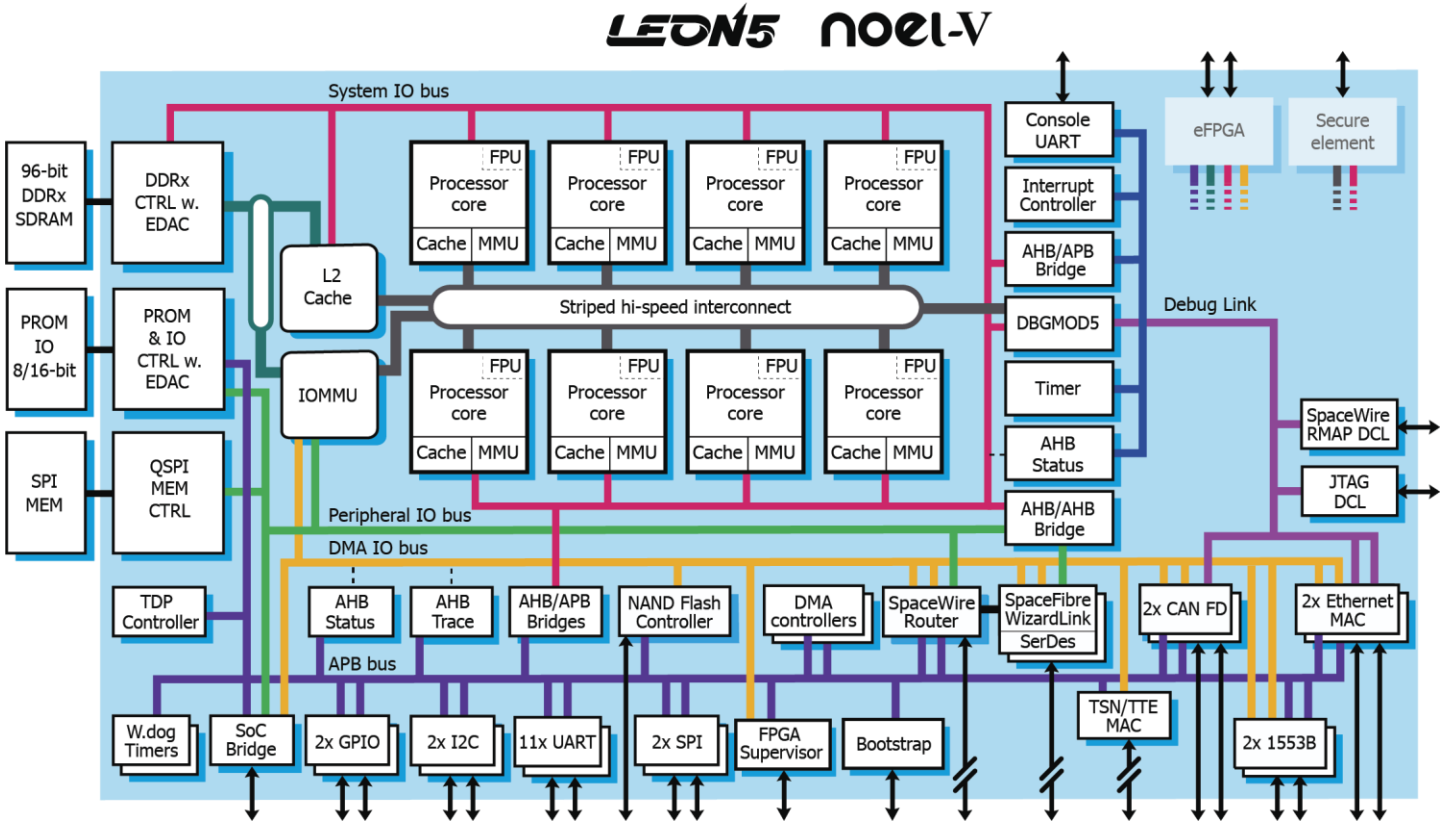


SPARC RISC-V®

GR765 – SoC improvements

Improvements

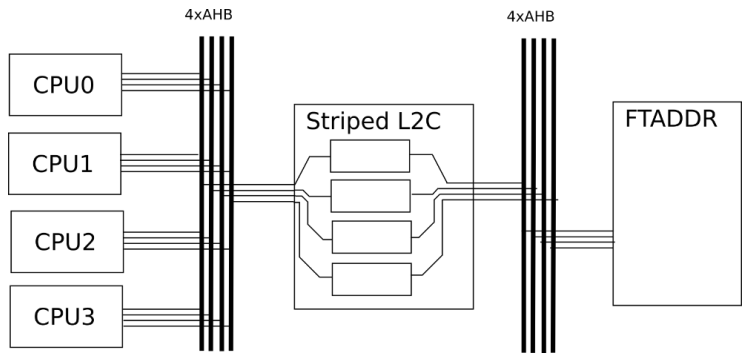
- Higher computational capacity and improved power consumption
- Processor subsystem utilizes multi-port connection (striped bus) between CPU cores and Level-2 cache, providing higher performance in the general case
- Improved timing isolation features (multi-core separation) where processors can use a subset of the multiple connections to Level-2 cache and memory controller.
- Additional I/O interfaces



SPARC RISC-V®

GR765 – Improved interconnect

- Striped interconnect contains 2/4 AHB 2.0 buses
  - All cores connected to all stripes
  - Built in support for larger physical address space, up to 48-bits
- Encoding to stripe based on (configurable) bits in physical address
  - Isolation is achieved by changing the most significant stripe selection bit to a higher logical address bit. Thus, it is possible to separate stripe 0-1 from 2-3.
- Encoding to stripe address space in L1 cache backend
  - Consistent addressing from L1 backend to DDR controller
- Fully isolated L2 cache pipelines dedicated to each stripe.
  - Controlled through a common AHB interface



GR765 – SpaceFibre interfaces

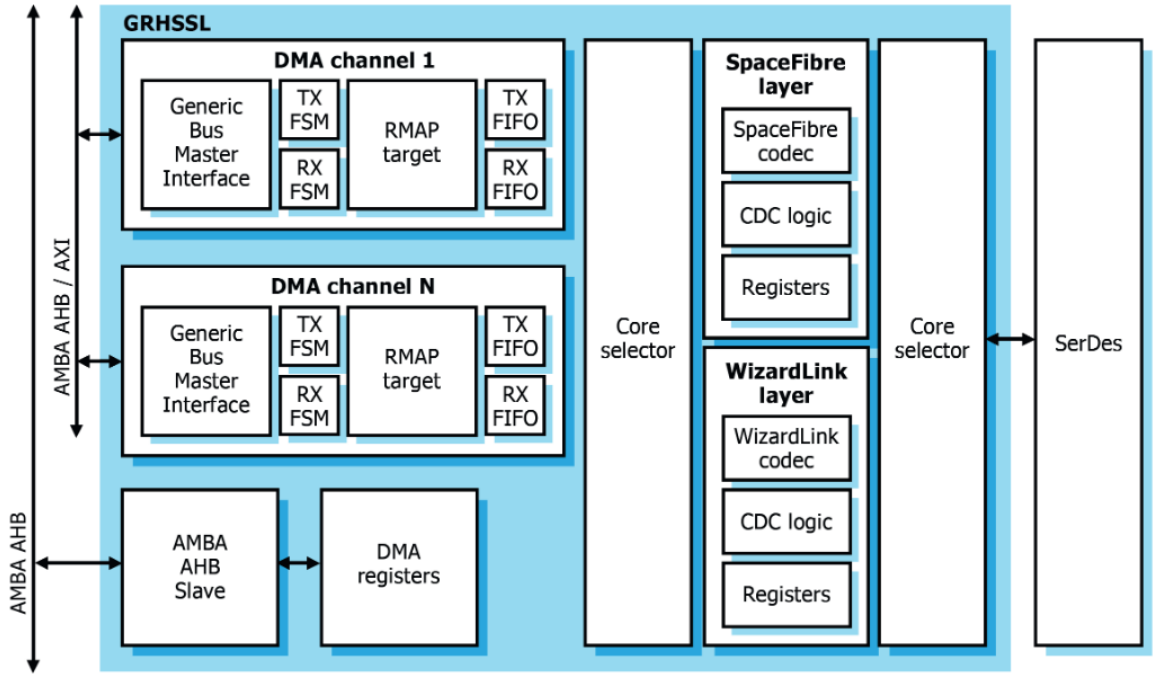
- SpaceFibre codec designed according to the ECSS-E-ST-50-11C standard
- Flexible DMA engine with multiple DMA channels: DMA channels operate in parallel and are assigned a subset of Virtual Channels and/or the Broadcast Channel
- Dedicated RMAP target per DMA channel: Make use of the dedicated AHB master interface of every channel
- RMAP can be separately enabled/disabled and configured in run time for each virtual channel: Each VC has a dedicated node address and destination key register
- Standalone RMAP CRC-8, CCSDS CCITT CRC-16 and 16-bit Checksum (J.G. Fletcher, ISO 8473-1:1998) logic for generic packets

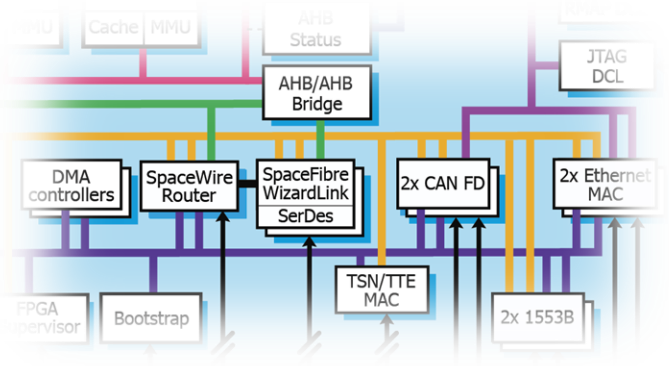
Integration of SpaceFibre with the SpaceWire router

- Bridge between SpaceWire and SpaceFibre traffic. Virtual channels route to SpaceWire router

WizardLink extension

- Companion WizardLink controller designed to interoperate the TLK2711 transceiver. Enable the communication with legacy equipment using custom protocols over WizardLink
- Minimal hardcoded functionality, high degree of configurability
- Only one controller (SpaceFibre or WizardLink) can be active at a time, selectable at run-time via AHB registers





GR765 – Under evaluation

Under evaluation

- IOMMU extensions – Replace GR740 IOMMU with implementation of RISC-V IOMMU (for both SPARC and RISC-V modes)
- eFPGA fabric vendor selection
- Secure element vendor selection

- Real-time trace support (RISC-V E-Trace encoder implemented, evaluating Nexus)
- DDR4 support
- PCIe (low probability)

Computing Roadmap – 2022, September

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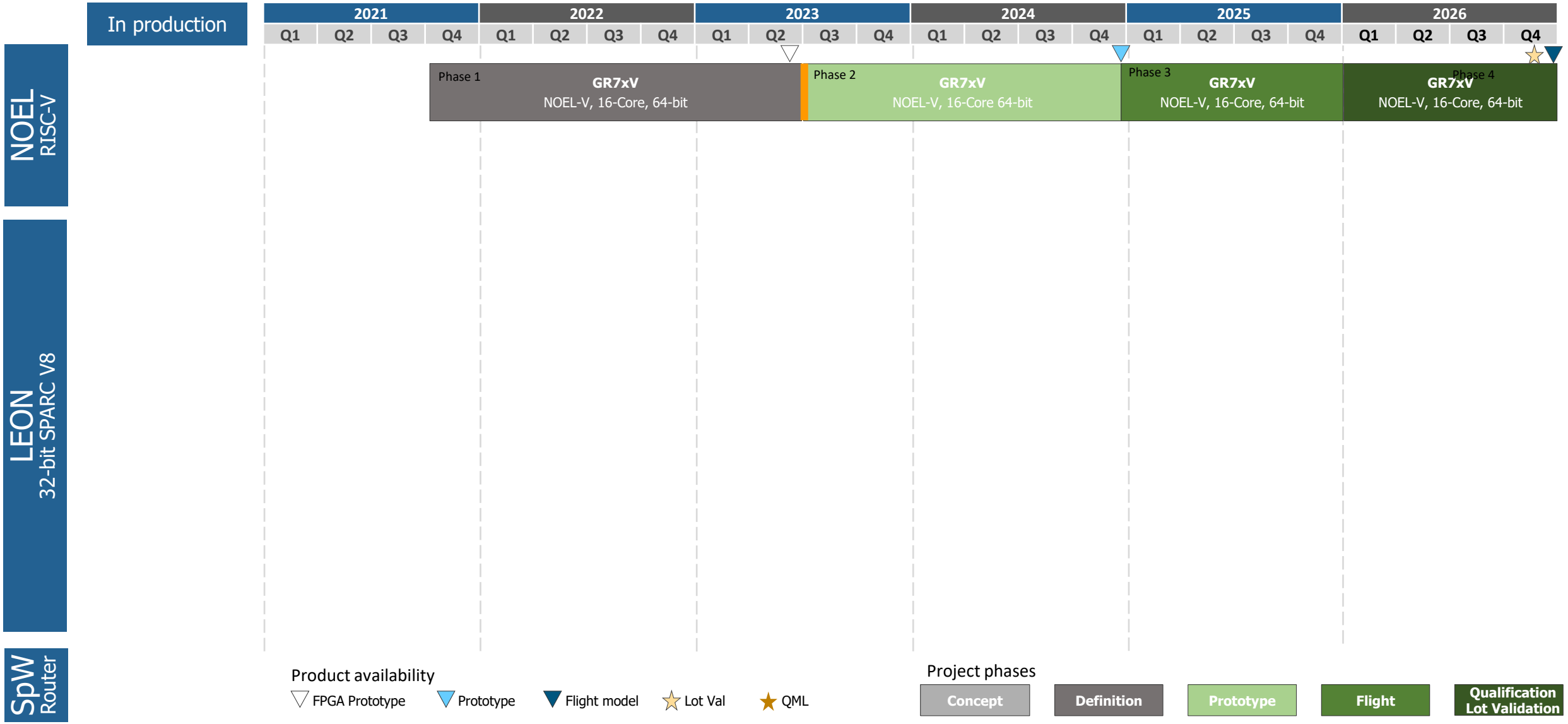


GR7xV – Overview

- The GR7xV is the working name for a future RISC-V based radiation-hardened fault-tolerant microprocessor
- Current specification, architectural and preliminary design work is carried out in a SNSA co-funded activity within the ESA ARTES Competitiveness & Growth programme.

GR7xV – 16-core NOEL-V Processor

In development
No guarantee of product launch

Baseline Features

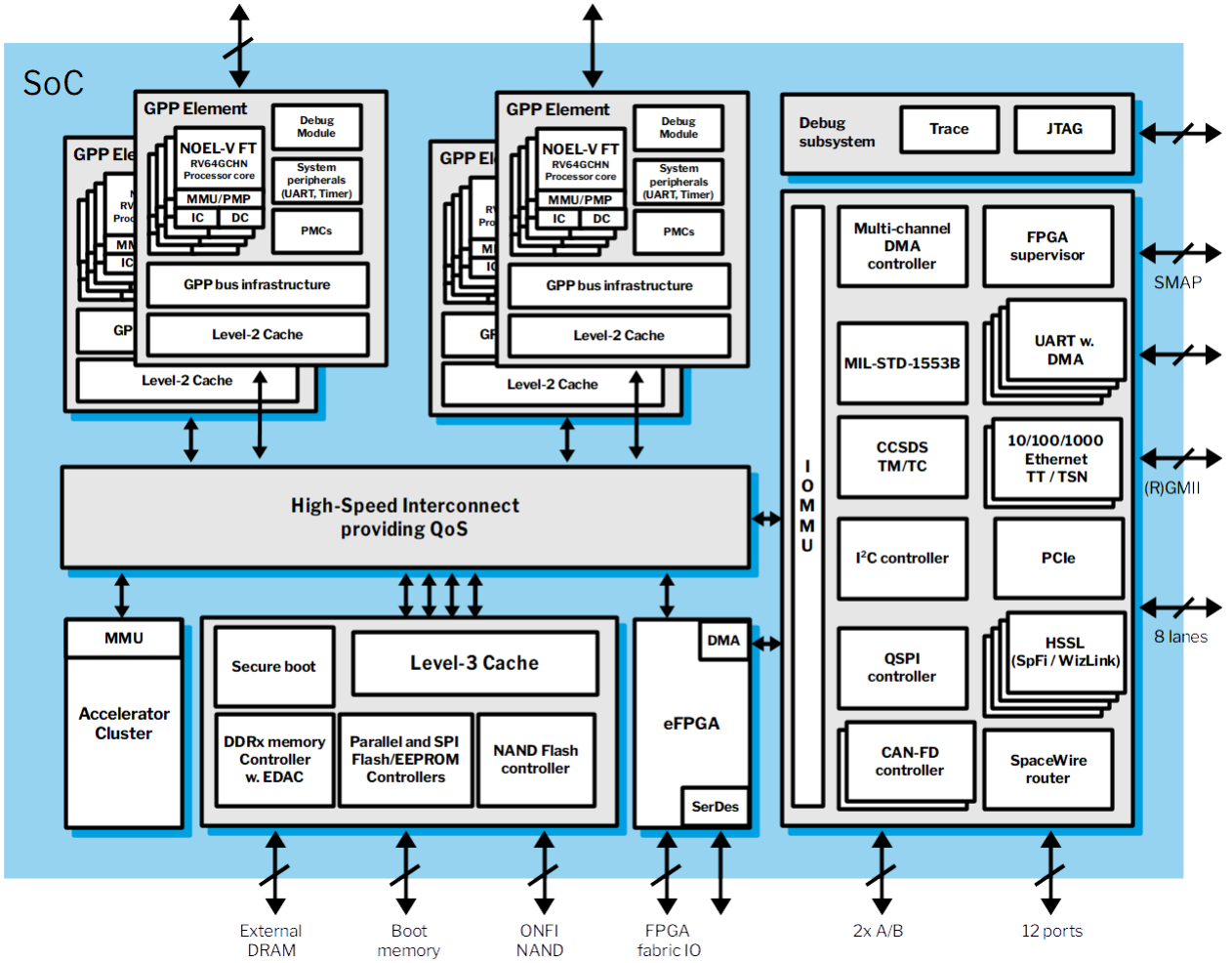
- Fault Tolerant 64-bit RISC-V Hexadeca-core with islands (GPP elements) of four general-purpose processors each with dedicated L2 caches
- HW assisted cache coherency between GPP elements and IO (accelerator TBD)

Accelerator

- Accelerators are being evaluated within the currently running activity
- Applications: Signal processing, ML, computer vision.
- Intent is to use accelerator for computations where the GPPs are inefficient.
- Software libraries to be provided by commercial vendor.

eFPGA

- Approach is to provide eFPGA for glue logic



Software

- Complete ecosystem
- A combination of Gaisler and 3rd party software

Tool chains, Operating systems and compilers

- Bare-C
- Linux
- RTEMS
- VxWorks
- Zephyr

Hypervisors

- XtratuM/XNG (FentISS)
- PikeOS (SYSGO)
- Xvisor

Boot loaders

- MKPROM2
- GRBOOT Flight bootloader

Tools

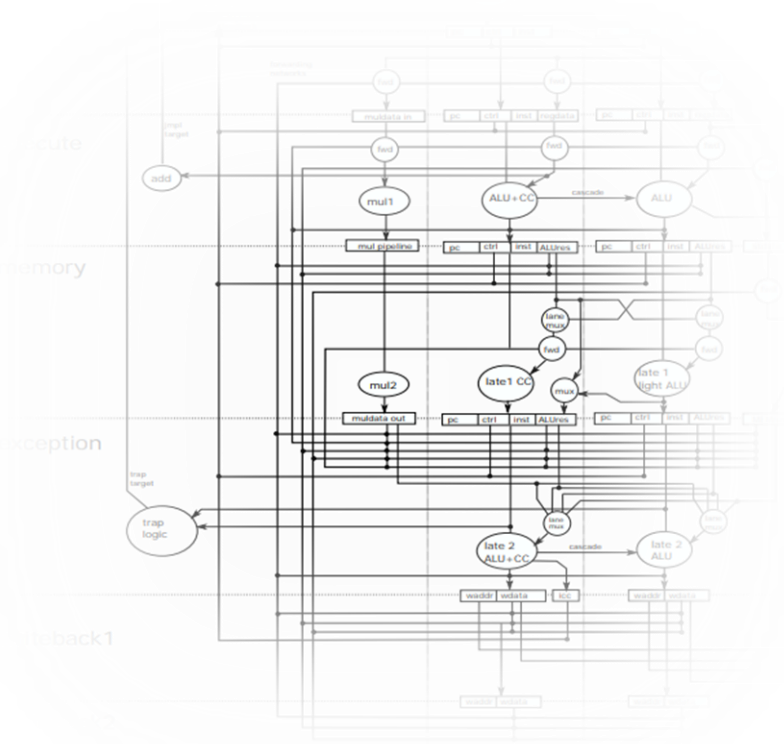
- GRMON3
- TSIM3

GR765 and GR740 SW Compatibility

- LEON5FT maintains backward compatibility with LEON4FT.
- Software running on top of environments such as RTEMS, VxWorks, Linux, ... should not require any changes if moving from GR740 to GR765 (updated OS will be provided by CG).
- Example: unmodified LEON3 Linux image will boot on LEON5.
- Redefinition of some internal processor configuration registers, may affect operating system, bootloaders, ….
- Set of communication interfaces is kept and expanded – but PCI is removed
- Changes will be addressed in a **Software Porting Guide**.
  - Versions of communication controller IP may be updated, may require updated software drivers.
  - Memory controllers and pin-mux control are updated.
  - Requires updates to bootloader.
- Significant differences in timing (different processor microarchitecture, memory controller, bus structure, etc).
- Work ongoing to enable same level of software support for NOEL-V as for, and extending beyond, the LEON processors.

Final words

- GR740 is available today in ceramic and plastic packages
- The GR765:
  - Includes an **octa-core** LEON5FT. Bootstrap option allows to enable NOEL-VFT RISC-V 64-bit processor cores instead of the LEON5FT cores.
  - Supports DDR3 SDRAM, high-speed serial link controllers and several other extensions.
  - GR765-XX (prototype) components are to be available in 2024.
  - FPGA bitstreams to be made available within the coming months
- GR7xV is Gaisler's future architecture, significantly changing the SoC architecture
- LEON5 and NOEL-V are available as part of the GRLIB IP library
  - Dual licensed IP library: Free open-source variant available at gaisler.com/getgrlib
  - The library includes infrastructure for project file generation for most popular EDA tools and SoC template designs
- FPGA bitstreams for Xilinx and Microchip FPGA evaluation boards are available for download
- Debug monitor and software toolchains (Bare-C, RTEMS, Linux, …) are also available

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