NG-Ultra

The European rad-hard SoC + FPGA
suitable for future space applications

ADCSS 2022

DEFENCE AND SPACE

Jean-Luc POUPAT, October 2022
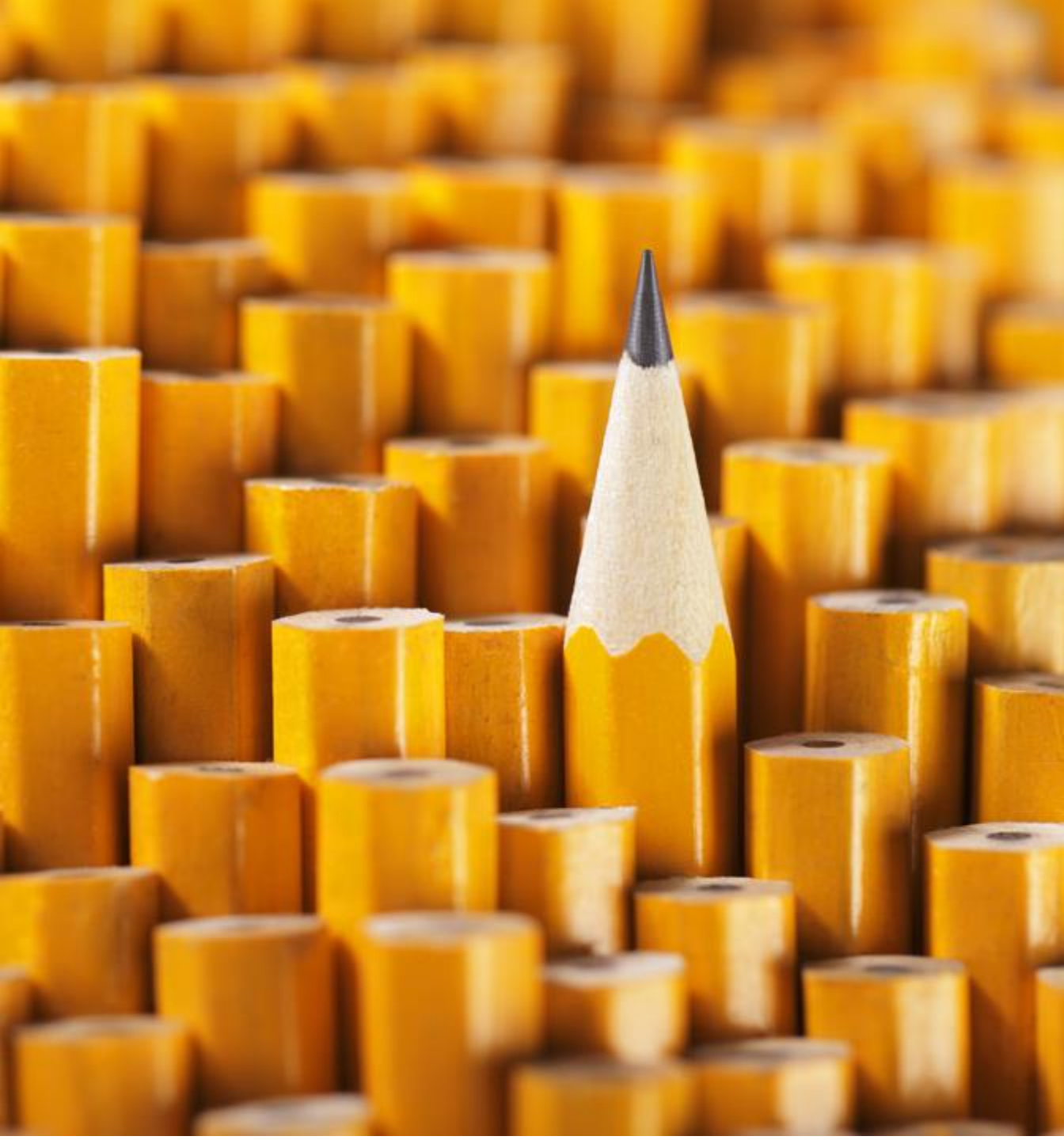
AIRBUS

AGENDA

Introduction

Performances Status

Ecosystem Status

Suitability for Upcoming Missions

Conclusion

AIRBUS

Why NG-Ultra is unique in the landscape of available Rad Hard components?

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Initiated by **CNES**, collaboration between **Airbus** and **TAS** to develop a **European chip** with 4 main objectives :

- a large improvement of **performances** to cope with evolutions of needs in the mid/long term

- a dynamic **ecosystem** closer to ground applications in order to enhance possible synergies

- a competitive **solution** allowing much more integration and **suitable** for upcoming missions

- a space technology for **European strategic non-dependence**
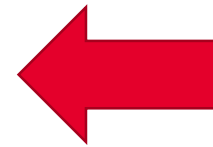
NG-Ultra = SoC + FPGA

NanoXplore is the company owning and commercialising the NG-Ultra manufactured by **STMicro**

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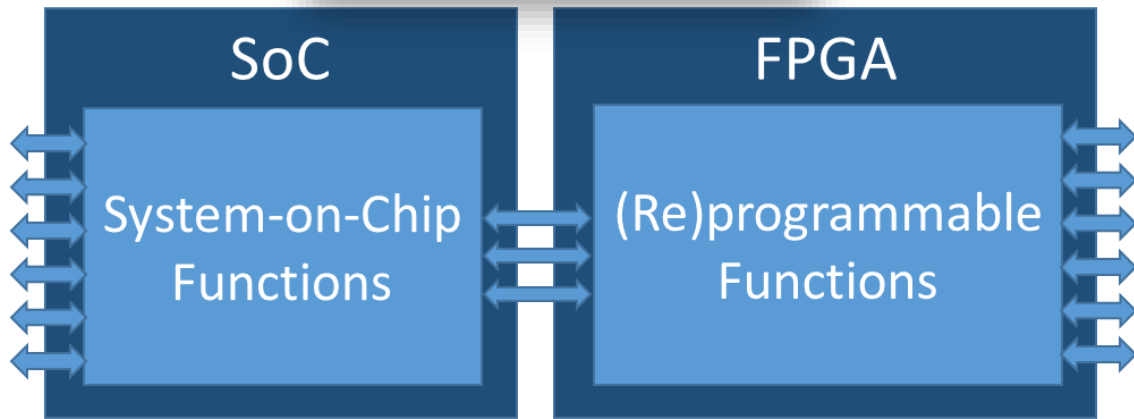
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Current generation

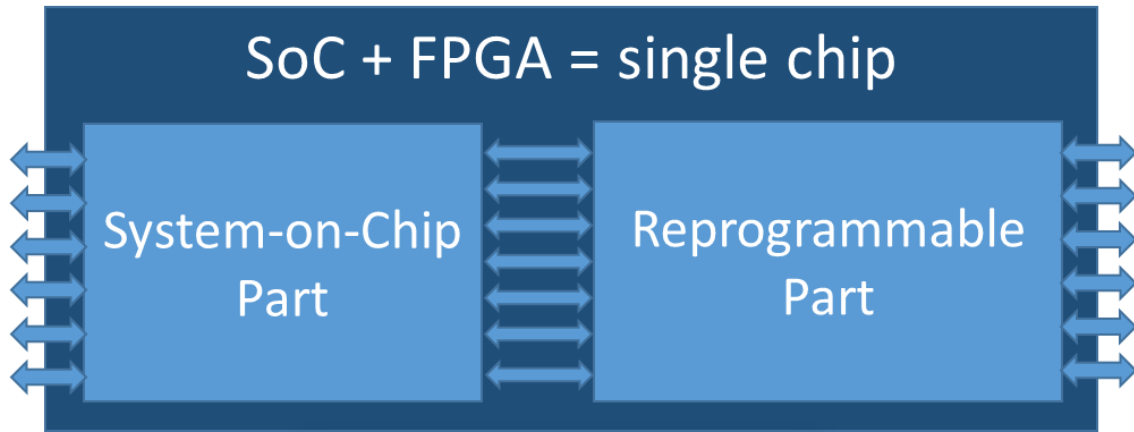SoC — System-on-Chip Functions

FPGA — (Re)programmable Functions

Example : SCOC3 + RTAX2000

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Current generation

SoC

System-on-Chip Functions

FPGA

(Re)programmable Functions

SoC + FPGA = single chip

System-on-Chip Part

Reprogrammable Part

Next generation

Example : SCOC3 + RTAX2000

Example : NG-Ultra

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American industry

European industry

Rad Hard

Intel® Agilex™ FPGA Series

F-SERIES	I-SERIES	M-SERIES
For wide range of applications	For high-performance processor interface and bandwidth-intensive applications	For compute-intensive applications
Up to 58G transceivers	Up to 112G transceivers	Up to 112G transceivers
PCIe* Gen4	PCIe Gen5	PCIe Gen5
DDR4 SDRAM	DDR4 SDRAM	DDR5 and Intel Optane™ DC persistent memory support
Quad-core Arm* Cortex*-A53 SoC option	Quad-core Arm Cortex-A53 SoC	Quad-core Arm Cortex-A53 SoC
	Compute Express Link (CXL) to Intel* Xeon* Scalable processor option	Compute Express Link (CXL) to Intel Xeon Scalable processor option
		High Bandwidth Memory option

Integrated SoC+FPGA

- Consistent with the design of processing boards

- Optimized interfaces SOC ←→ FPGA

- Key enabler for more integrated designs & cost reduction

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How I see my design

How the others see it

What are the breakthroughs [*] of NG-Ultra architecture and detailed performances ?

(*) for a rad-hard component

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On chip Memory
- eRAM
- eROM

ARM-based quad-core CPU

Debug & Trace

| Cortex-R52 | Cortex-R52 | Cortex-R52 | Cortex-R52 |

External Memory
- DDR
- FLASH

Enhanced AXI Interconnect Cross-Bar

Embedded FPGA

16 channels DMA

SoC Services
- Clock & Reset
- V&T Monitor
- Error Mgmt
- Boot SpW
- Security
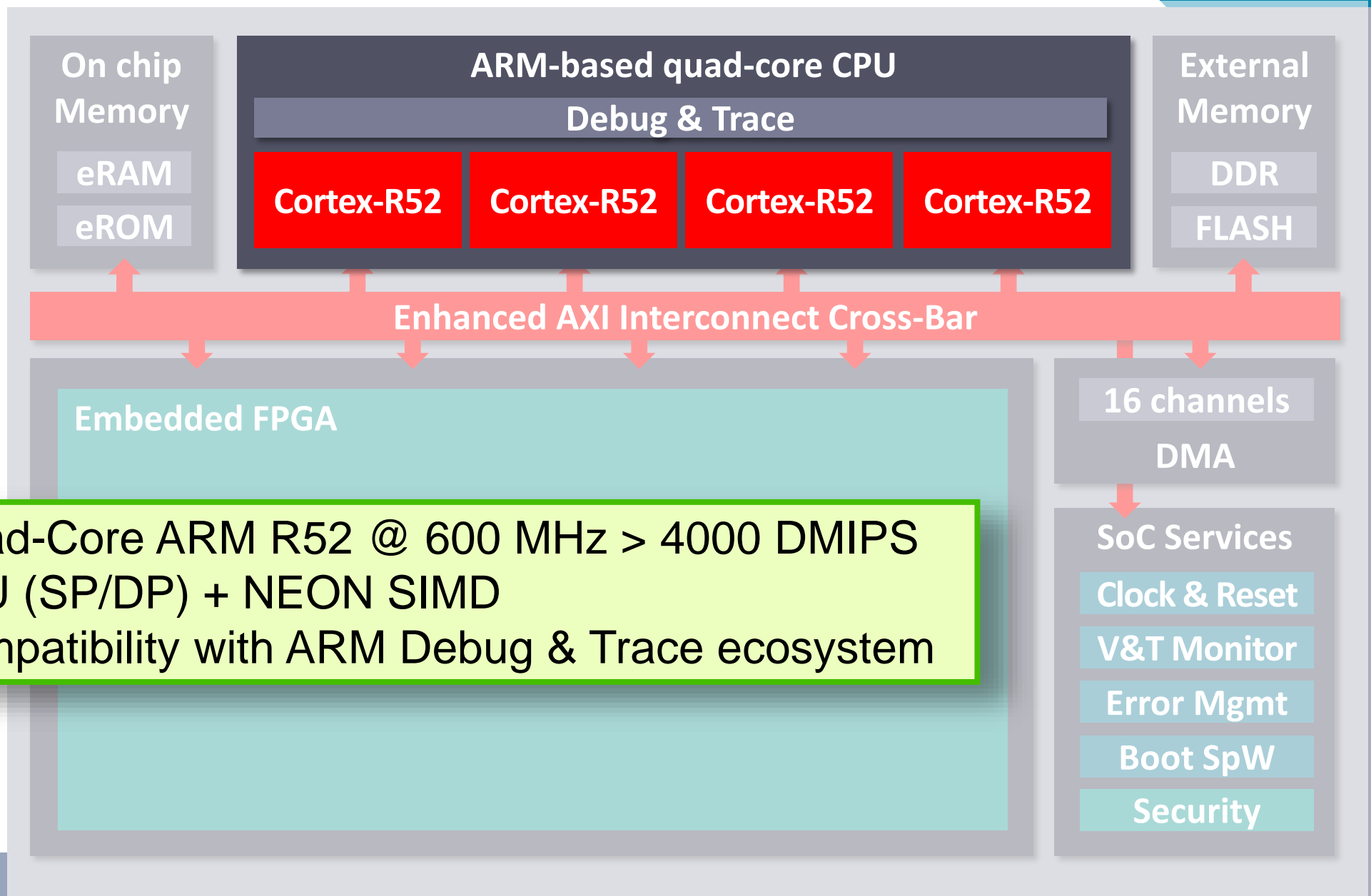
→ Quad-Core ARM R52 @ 600 MHz > 4000 DMIPS
→ FPU (SP/DP) + NEON SIMD
→ Compatibility with ARM Debug & Trace ecosystem

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FPU : Floating Point Unit / SP/DP : Single/Double Precision / SIMD : Single Instruction Multiple Data Co-processing

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- eROM

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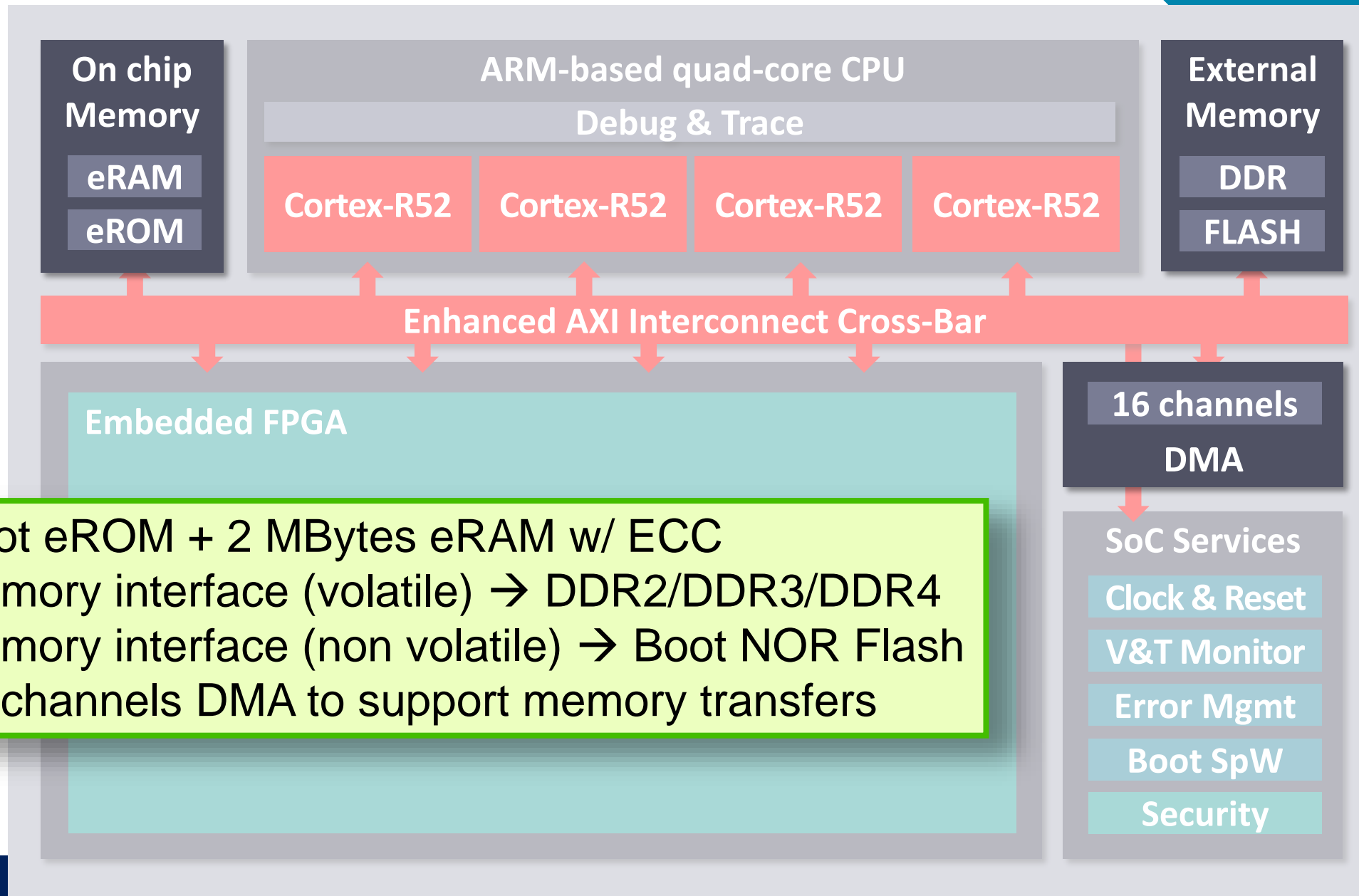
➔ Boot eROM + 2 MBytes eRAM w/ ECC
➔ Memory interface (volatile) ➔ DDR2/DDR3/DDR4
➔ Memory interface (non volatile) ➔ Boot NOR Flash
➔ 16 channels DMA to support memory transfers

ECC : Error Correcting Code- / DMA : Direct Memory Access

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On chip Memory
- eRAM
- eROM

ARM-based quad-core CPU

Debug & Trace

Cortex-R52 | Cortex-R52 | Cortex-R52 | Cortex-R52

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Embedded FPGA

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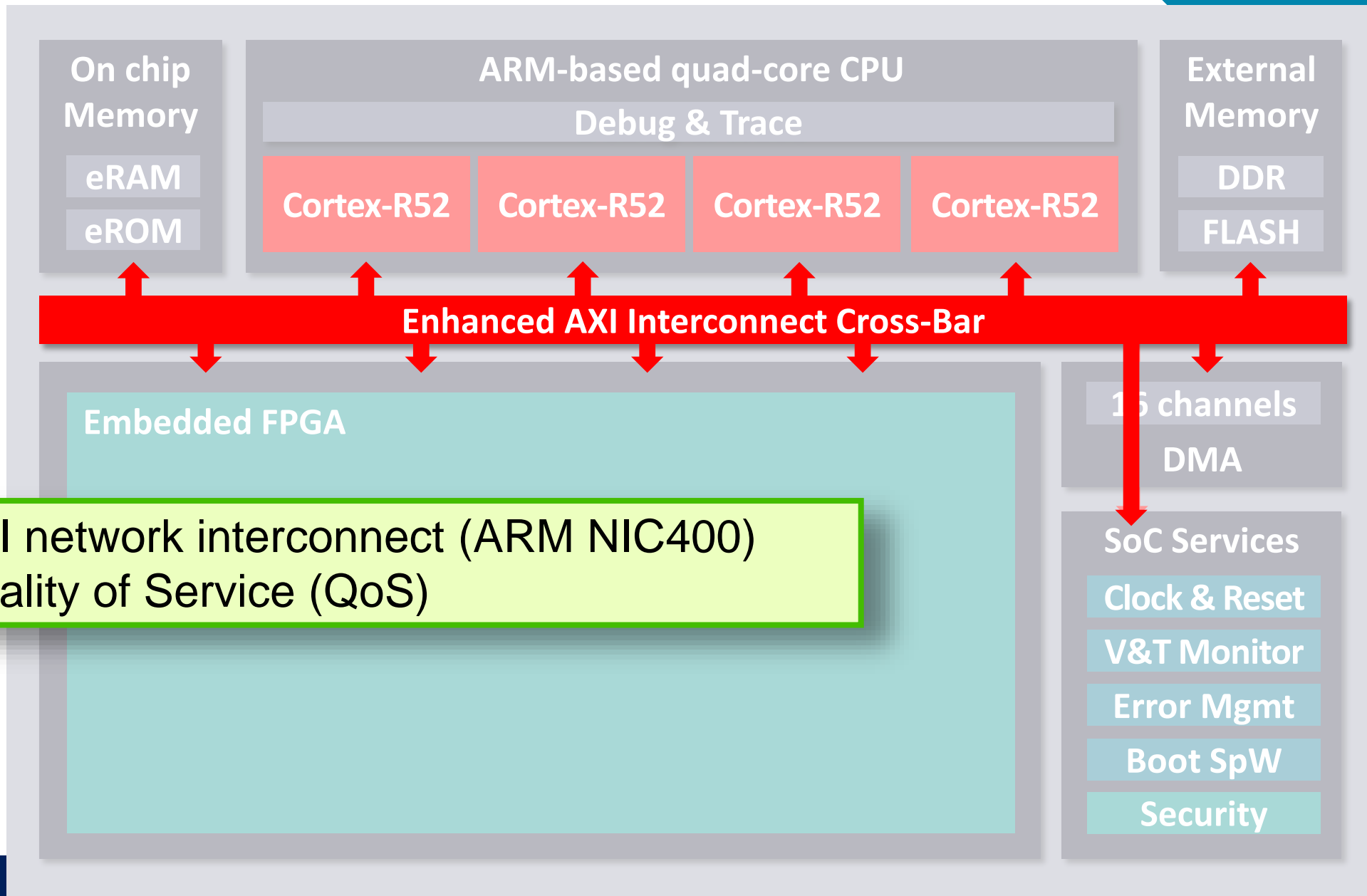
→ AXI network interconnect (ARM NIC400)
→ Quality of Service (QoS)

SoC Services
- Clock & Reset
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On chip Memory
- eRAM
- eROM

ARM-based quad-core CPU
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External Memory
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Embedded FPGA

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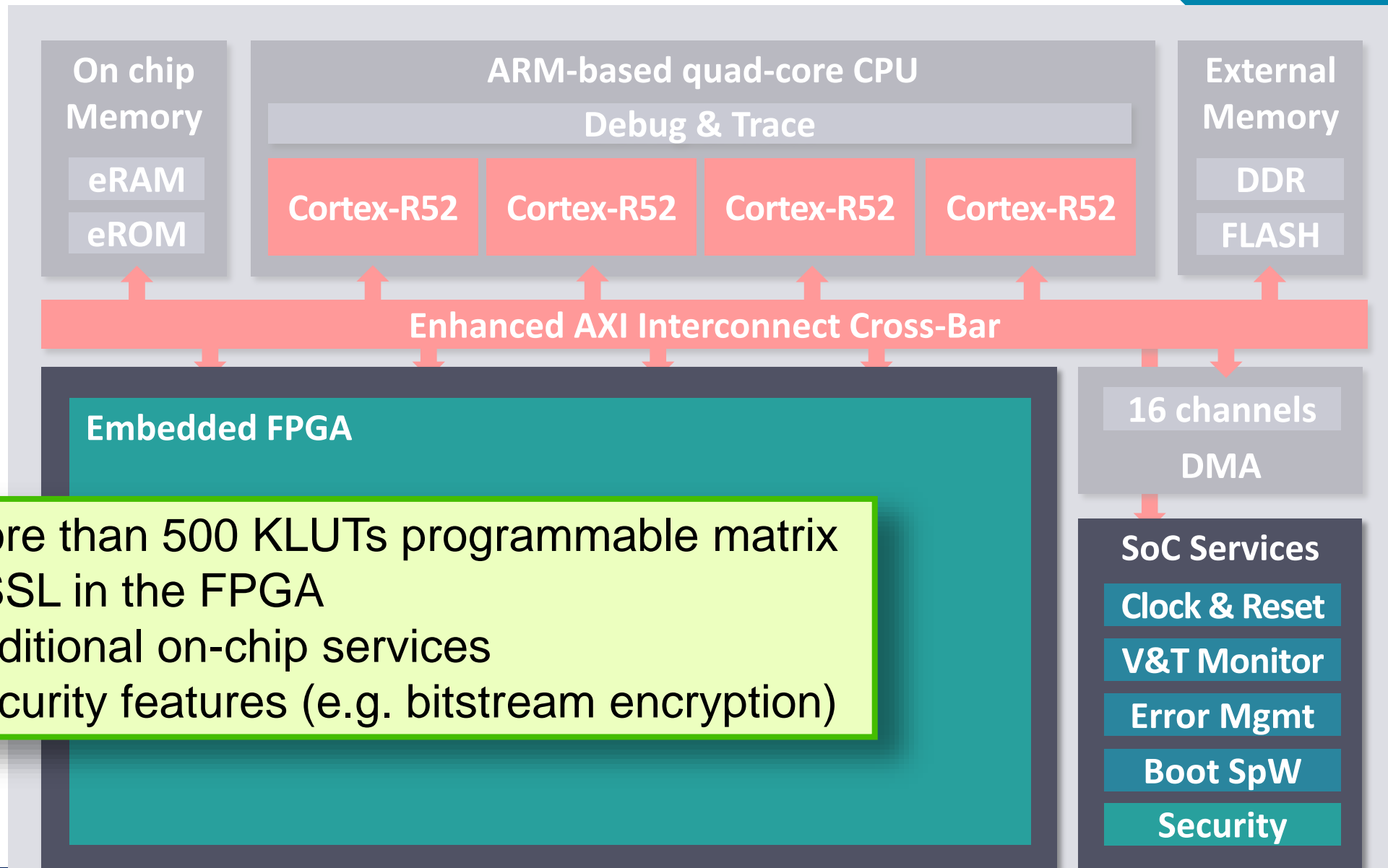
→ More than 500 KLUTs programmable matrix
→ HSSL in the FPGA
→ Additional on-chip services
→ Security features (e.g. bitstream encryption)

SoC Services
- Clock & Reset
- V&T Monitor
- Error Mgmt
- Boot SpW
- Security

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LUT : Look Up Table / HSSL : High Speed Serial Link

On chip Memory	ARM-based quad-core CPU				External Memory
	Debug & Trace				
eRAM	**Cortex-R52**	**Cortex-R52**	**Cortex-R52**	**Cortex-R52**	**DDR**
eROM					**FLASH**

Enhanced AXI Interconnect Cross-Bar

Embedded FPGA

16 channels

DMA
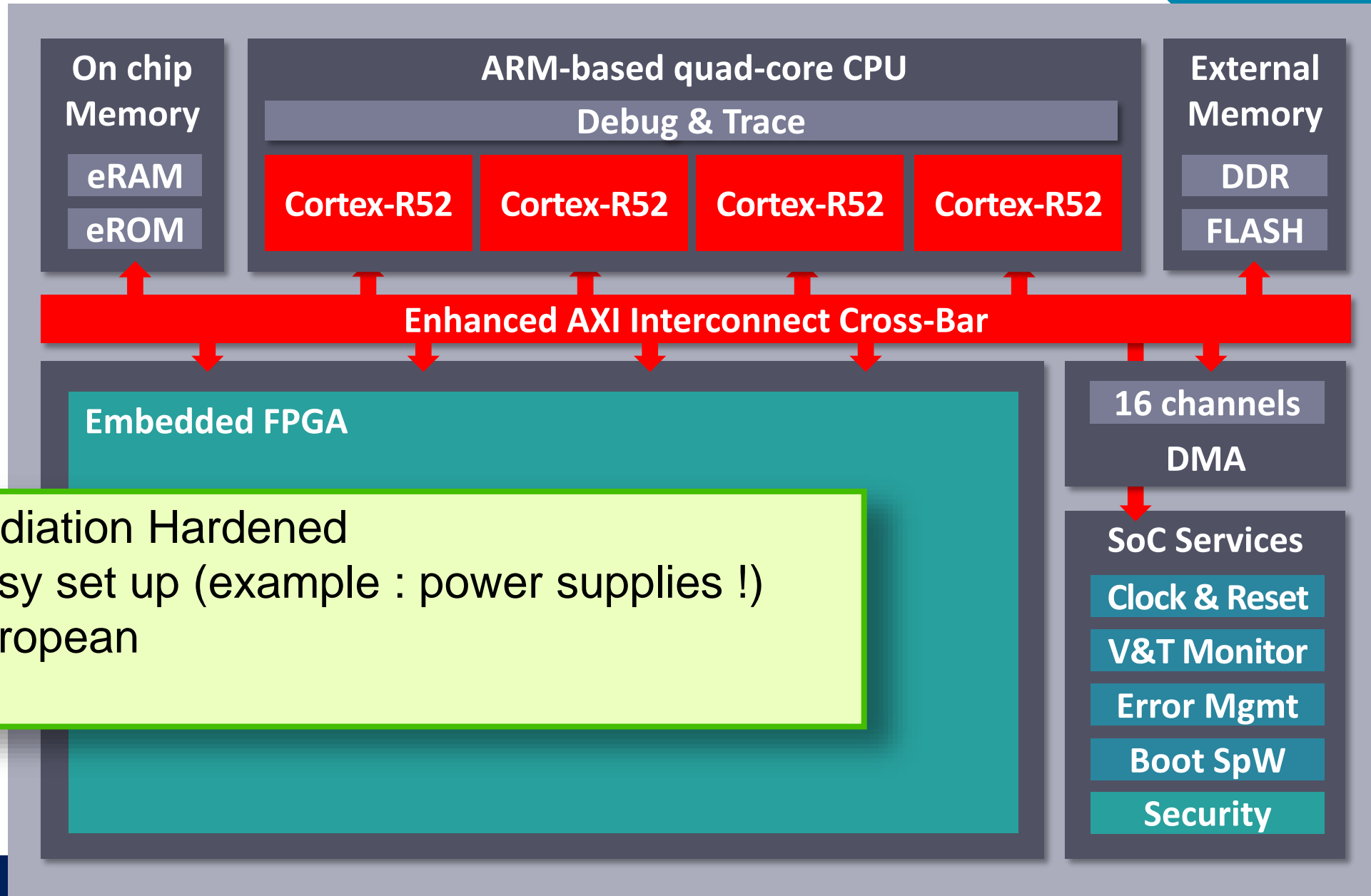
→ Radiation Hardened
→ Easy set up (example : power supplies !)
→ European
→ …

SoC Services

Clock & Reset

V&T Monitor

Error Mgmt

Boot SpW
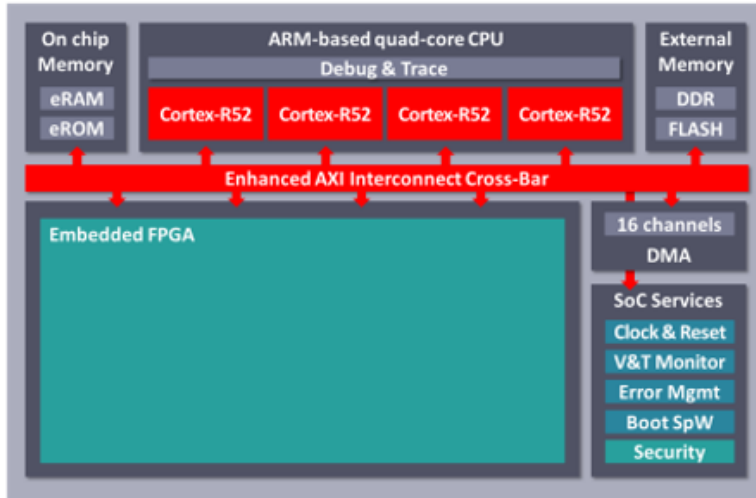
Security

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PS = Processing System

PL = Programmable Logic

NG-ULTRA

PS part
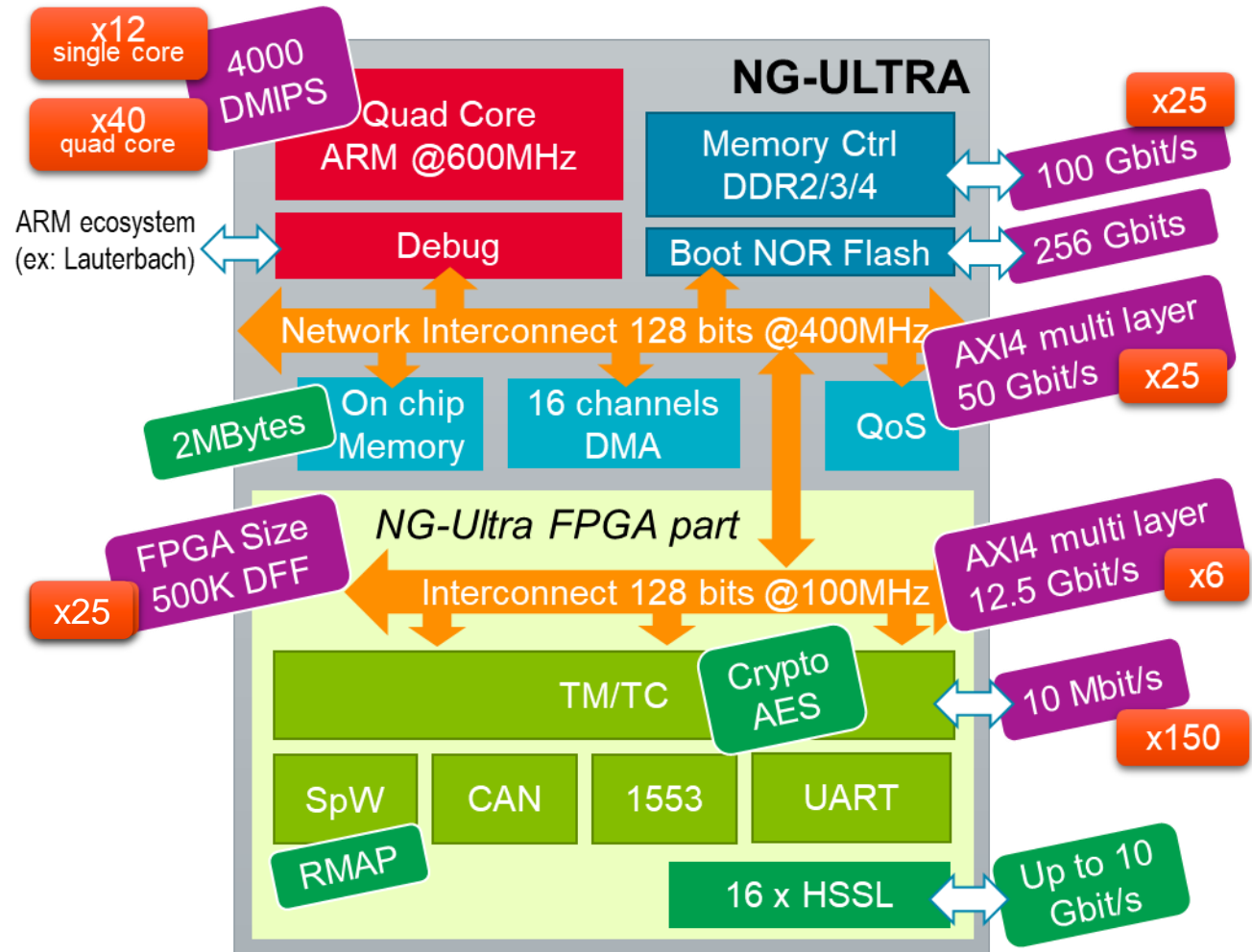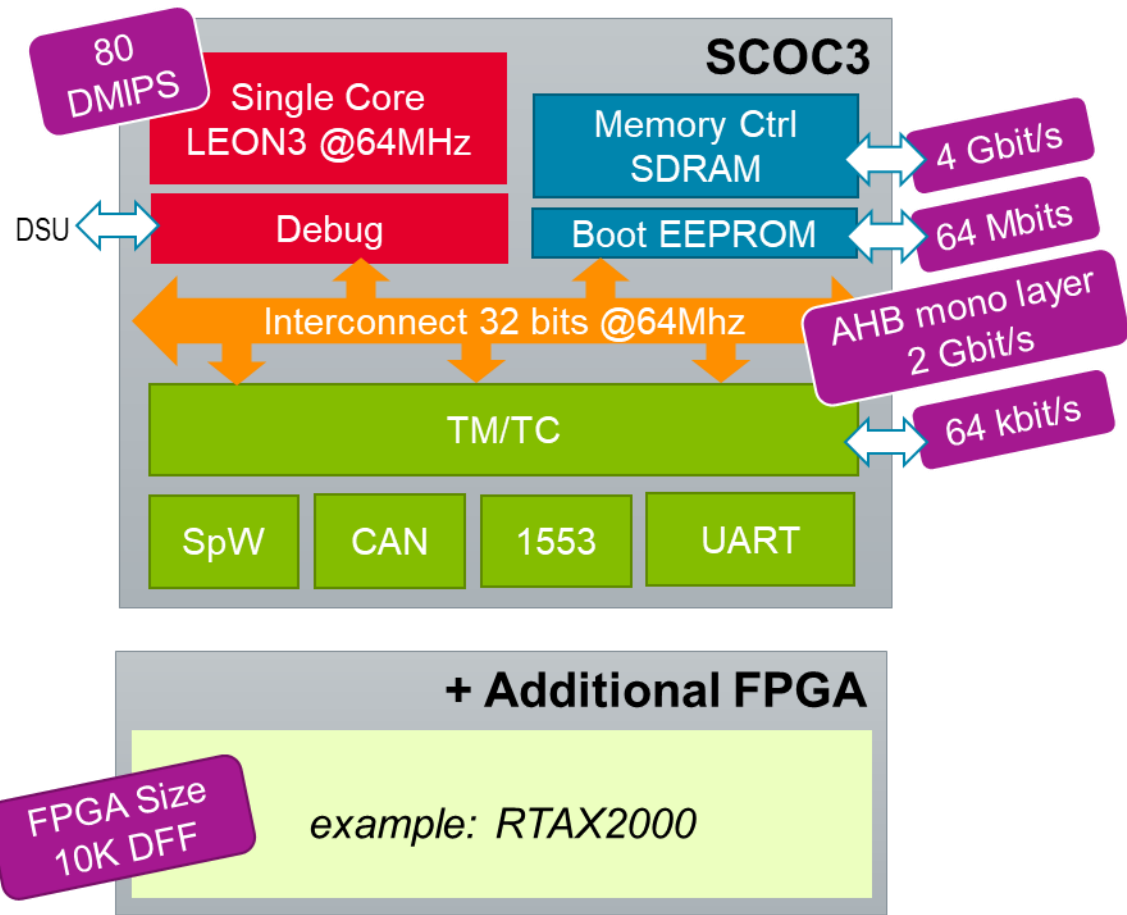

PL part
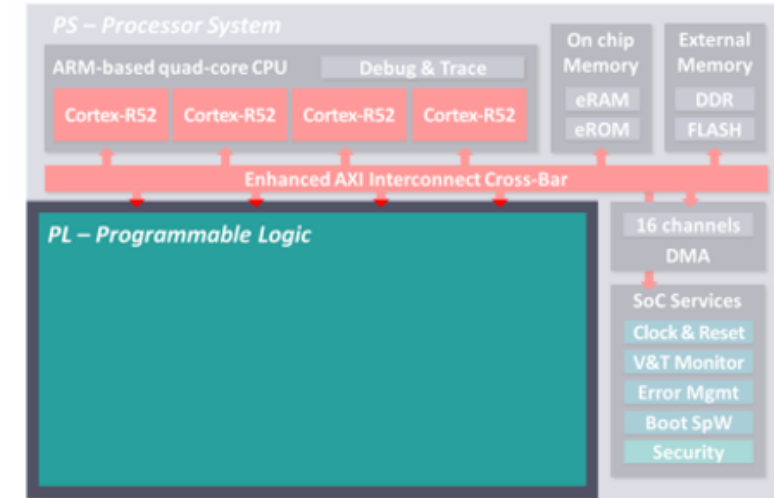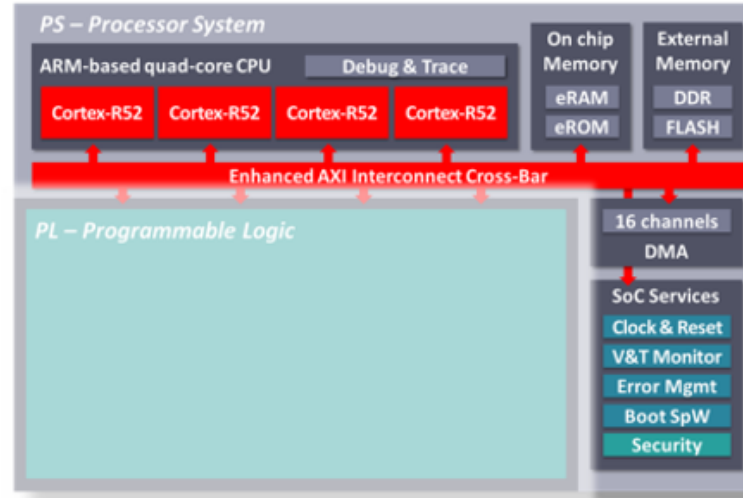
SoC + FPGA

SoC only

FPGA only

CPU Performance
→ 40 x SCOC3
→ 2 x GR740

FPGA Capacity
→ 2 x RTG4 (*)
→ 25 x RTAX2000 (*)

(*)   estimation of realistically useable FPGA size at ADCSS 2022 date, twice more to be expected considering theoretical LUTs resources and the strong momentum deployed on tools

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SCOC3

- 80 DMIPS
- Single Core LEON3 @64MHz
- Debug
- DSU
- Memory Ctrl SDRAM — 4 Gbit/s
- Boot EEPROM — 64 Mbits
- Interconnect 32 bits @64Mhz
- AHB mono layer 2 Gbit/s
- TM/TC — 64 kbit/s
- SpW
- CAN
- 1553
- UART

+ Additional FPGA

- FPGA Size 10K DFF
- example: RTAX2000

NG-ULTRA

- x12 single core
- x40 quad core
- 4000 DMIPS
- Quad Core ARM @600MHz
- ARM ecosystem (ex: Lauterbach)
- Debug
- Memory Ctrl DDR2/3/4 — x25 — 100 Gbit/s
- Boot NOR Flash — 256 Gbits
- Network Interconnect 128 bits @400MHz
- AXI4 multi layer 50 Gbit/s — x25
- 2MBytes
- On chip Memory
- 16 channels DMA
- QoS
- *NG-Ultra FPGA part*
- FPGA Size 500K DFF — x25
- AXI4 multi layer 12.5 Gbit/s — x6
- Interconnect 128 bits @100MHz
- TM/TC
- Crypto AES
- 10 Mbit/s — x150
- SpW
- CAN
- 1553
- UART
- RMAP
- 16 x HSSL — Up to 10 Gbit/s

Comparing performances is important but not enough. Many other criteria shall be considered such as package, radiation hardening, cost, hardware setup (memories, power supply…), easiness to use, hardware and software ecosystem, risk mitigation of export control limitation, support to a European solution…

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Demonstrated NG-Ultra SoC Benchmarks

First tests performed on NG-Ultra prototypes at 600MHz on one ARM Cortex-R52 core (**single core**)

CoreMark	Freq (MHz)	CoreMark (Iterations/sec)	CoreMark/MHz
LEON2 (MDPA)	81 MHz	125 CoreMark	1.54
LEON4 (GR740)	250 MHz	511 CoreMark	2.04
Bring-Up Eval board (NG-Ultra)	**600 MHz**	**1 818 CoreMark**	**3.03**

Dhrystone	Freq (MHz)	DMIPS per core	DMIPS/MHz
LEON4 (GR740)	250 MHz	425 DMIPS	1.7
Brin-Up Eval board (NG-Ultra)	**600 MHz**	**1 250 DMIPS**	**2.08**

ARM performances (from ARM datasheet)
- ARM Coremark maximum performance : 4,3 CoreMark/MHz, without interconnect, without robustness features
- ARM Dhrystone maximum performance : 2,09 DMIPS/MHz

Performance on quad-core expected to be close to 4x the single core performance thanks to AXI architecture

→ NG-Ultra SoC performance breakthrough demonstrated @600 MHz !

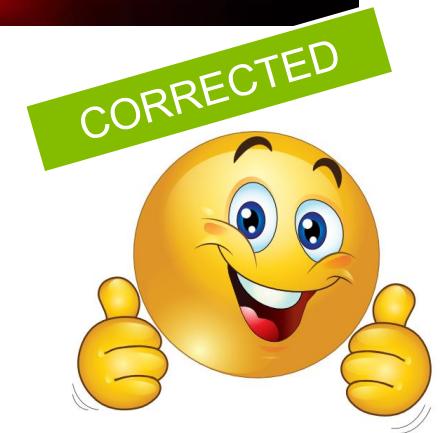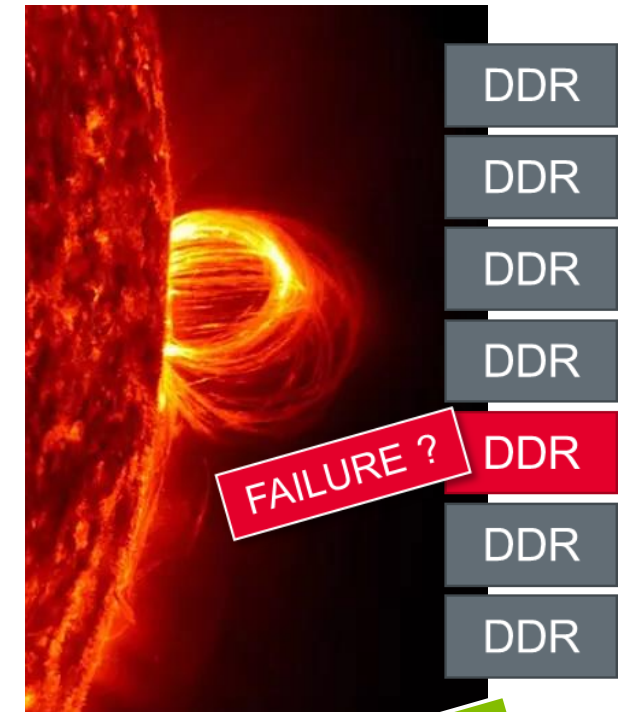**AIRBUS**

High performances DDR interface

- Supporting DDR2, DDR3 and DDR4
- Memory protection optimized for 8-bit & 16-bit devices
- Data bus width 64 bits + Reed-Solomon (RS) checkbits
  - DDR2 @ 200 MHz / 400 MT/s → 25 Gbps bandwidth
  - DDR4 @ 800 MHz / 1600 MT/s → 100 Gbps bandwidth
  - (to be compared to 3,2 Gbps for GR740)
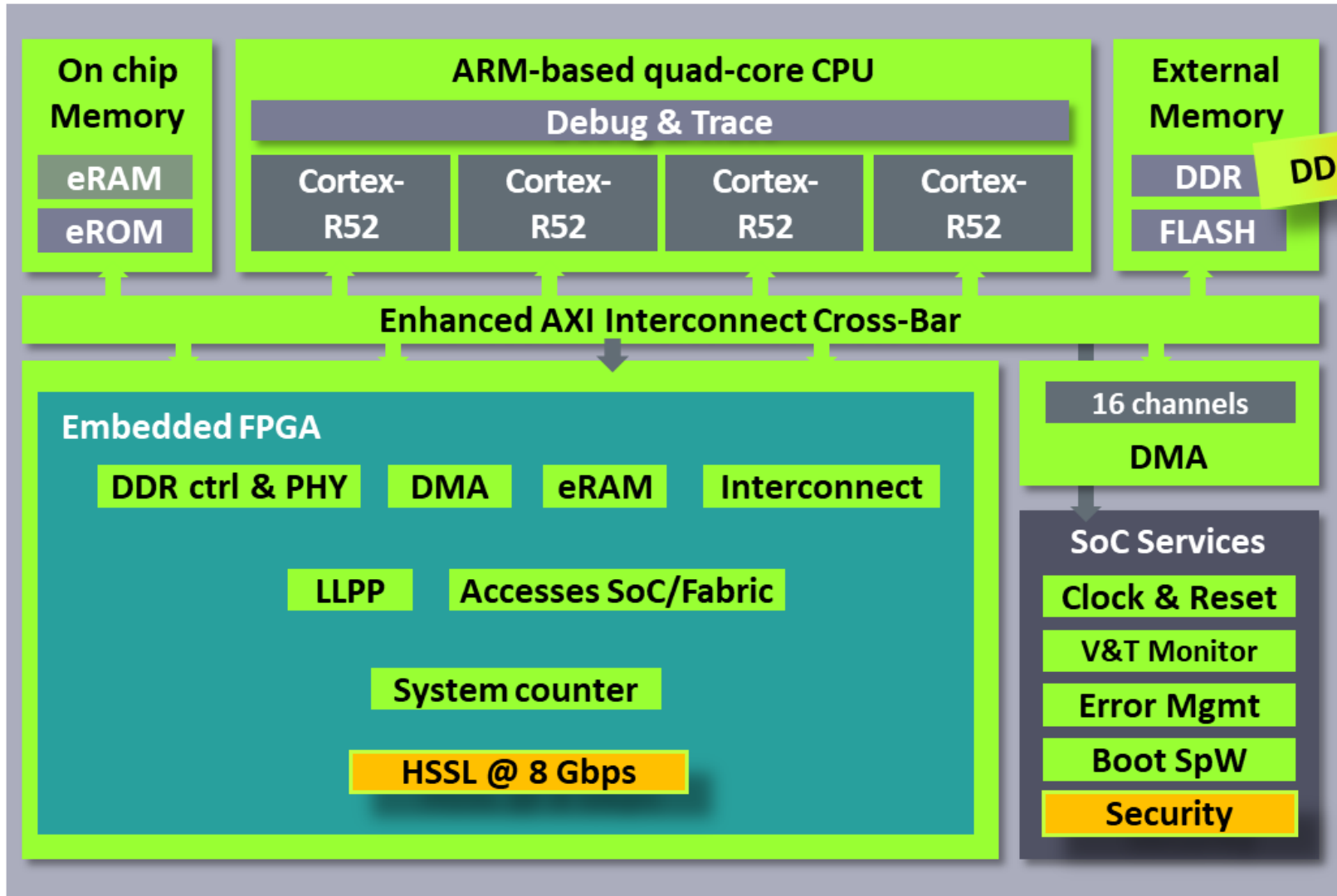- 4 memory channels to maximize bandwidth availability with integrated QoS

Very high level of protection against failures

- Error detection and correction **against SEU**
- **Robustness against SEFI** up to the loss of two 16-bits devices
- Software warned as soon as one device is in error

User-oriented features

- Integrated zero-padding
- Integrated autotest

DDR
DDR
DDR
DDR
FAILURE ? DDR
DDR
DDR

CORRECTED

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On chip Memory
- eRAM
- eROM

ARM-based quad-core CPU
- Debug & Trace
  - Cortex-R52
  - Cortex-R52
  - Cortex-R52
  - Cortex-R52

External Memory
- DDR — DDR4
- FLASH

Enhanced AXI Interconnect Cross-Bar

Embedded FPGA
- DDR ctrl & PHY
- DMA
- eRAM
- Interconnect
- LLPP
- Accesses SoC/Fabric
- System counter
- HSSL @ 8 Gbps

16 channels
DMA

SoC Services
- Clock & Reset
- V&T Monitor
- Error Mgmt
- Boot SpW
- Security

Functions

Functions demonstrated on first samples v1

Functions

Functions not demonstrated on v1, test to be performed on v2

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NG-Ultra tested for heavy ions during 2 radiation campaigns → **no SEFI**

- FPGA Configuration memory → no error detected (**no SEU, no SEFI**) up to 68 MeV/g/cm3
- DFF/registers → no error detected (**no SEU**) up to 68 MeV/g/cm3
- SoC → **no SEFI**
- PLL → **no SEFI, few SET,** good radiation performance,

Robustness of NG-Ultra v1 confirmed (**no SEU, no SEFI**), no redesign needed for v2 due to radiation

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What is the ecosystem status for developing hardware and software with NG-Ultra ?

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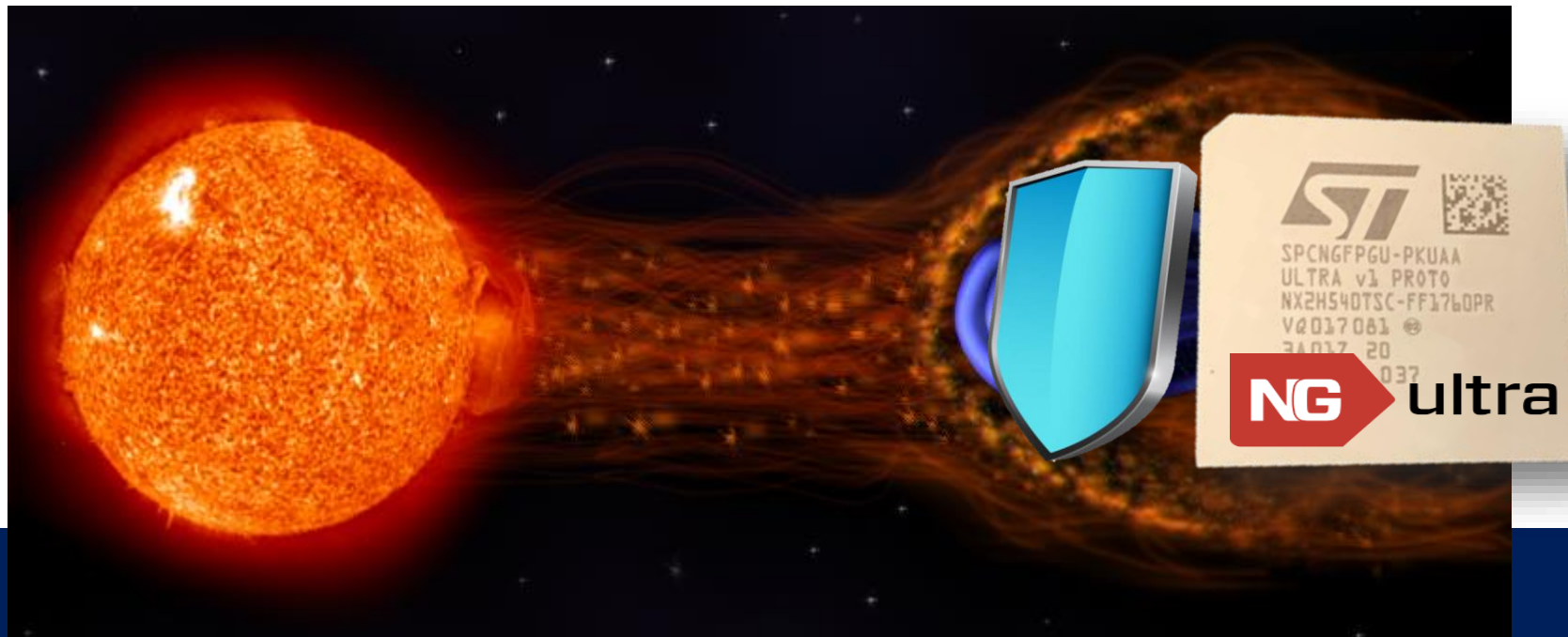
For **hardware** development

Synthesis, Place & Route → NXMap

- Synthesis step → can be considered as mature thanks to an agreement with Mentor Precision RTL which has helped a lot to get round of difficulties with NX synthesis tool.
- Place & Route step → target to have automatic optimization done by the tool is not yet reached, can be get round with manual place & route tasks with NX support, noticeable improvements of the tools after each release

Bitstream loading → NXBase2

- Available & Mature

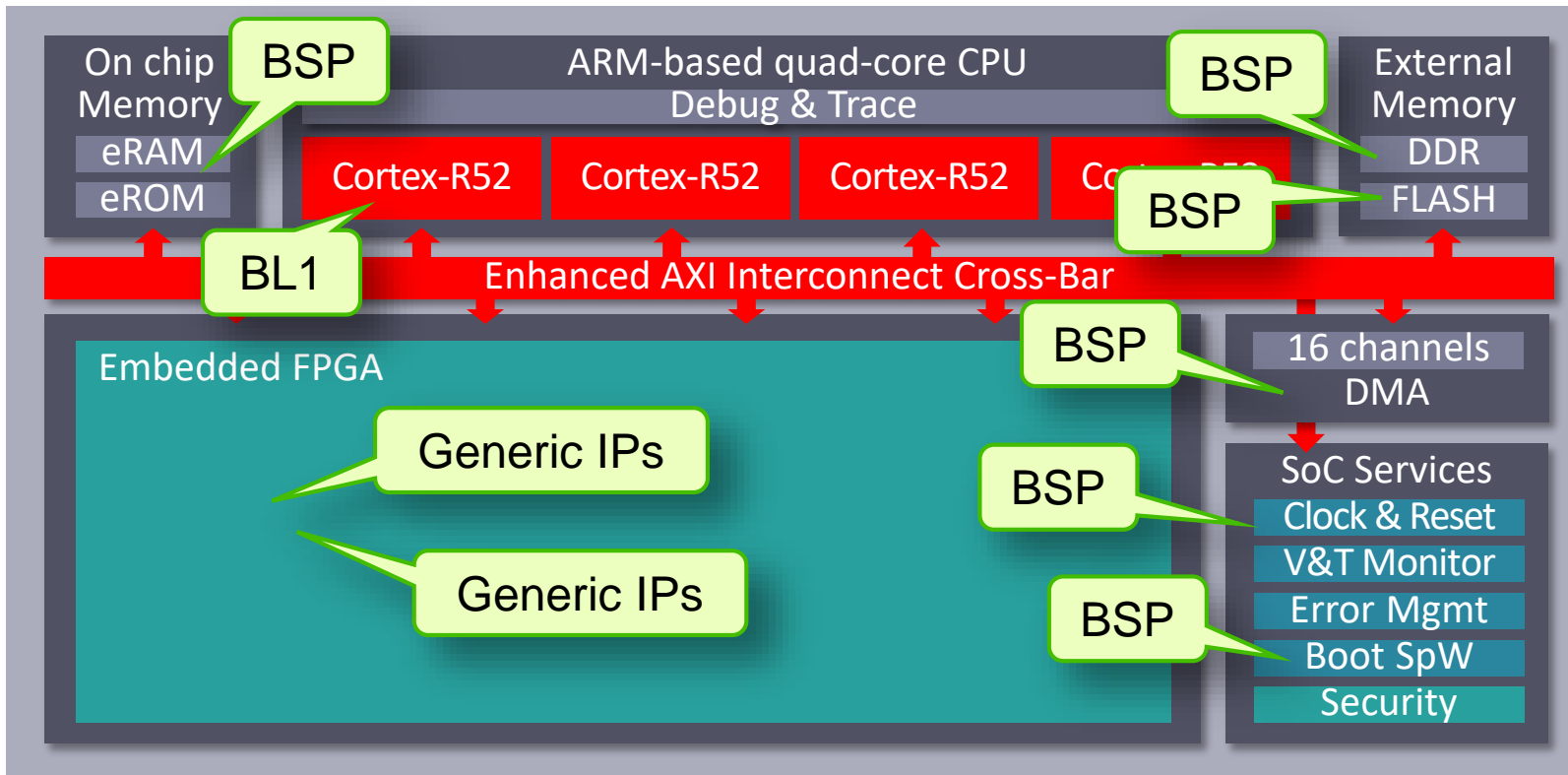## For **software** development

Debug and trace → ARM ecosystem

- Supported as predefined chip in Lauterbach toolsuite
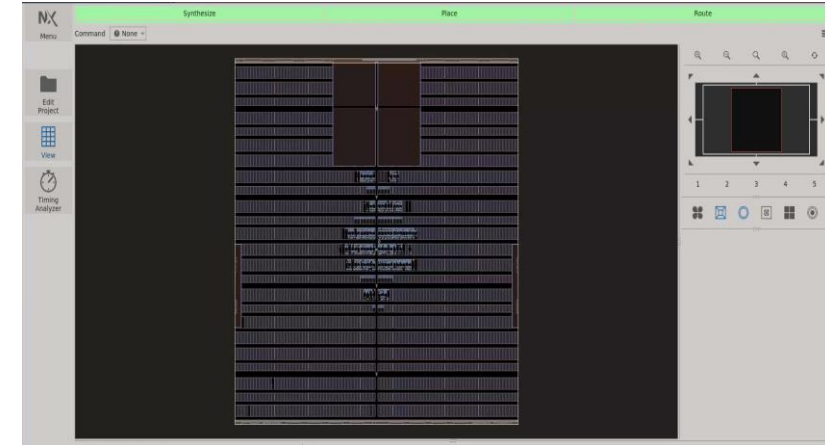
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Software Design Kit (SDK) available

- BSPs (drivers) for SoC functions available
- Generic Boot Loader 1 (BL1) to complement Boot Loader 0 (in the ROM) available

Hardware

- Generic IPs embedded in NXMap for the FPGA

HW and SW developments to maximise reuse of building blocks

Developed by the DAHLIA consortium and completed by Airbus internal R&D

Enabler for non recurring cost reduction for future projects

The more users we are, the more the ecosystem can keep growing !

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Hardware Developments

- Elementary modules usable for all NG-Ultra-based projects
- Common platform for all NG-Ultra-based projects in Airbus DS

Software Developments

- RTOS selected & adapted to NG-Ultra
- Hypervisor selected & adapted to NG-Ultra
- Common Platform BSPs

Common framework for all NG-Ultra projects

- Reducing non-recurring costs
- Reducing time-to-market

➡ Fully in line with ADHA objectives

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Why NG-Ultra answers to a large number of future needs and space missions ?

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NG-Ultra already implemented on an Airbus processing board

Perfect demonstration for a future NG-Ultra-based OBC

- NAND Flash + **DDR4 Memory**
- High Speed Serial Links
- Enhanced Security features (SDLS extended)
- High performances multicore processing
- Bitstream encryption included
- ADHA-compatible format

Very integrated OBC

- **500 kLUT** compared to ~20kLUT for previous generation with RTAX2000
- More embedded functionalities
- **Very compact product**

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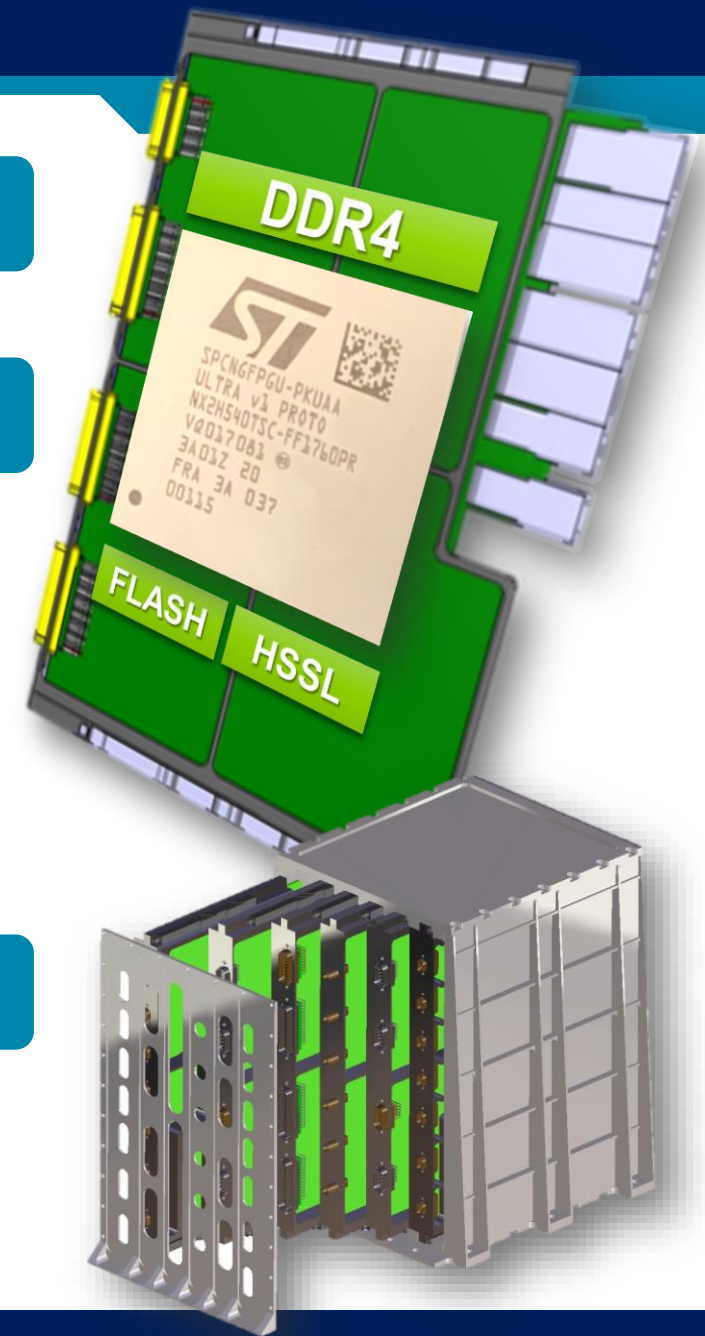
Payload Missions
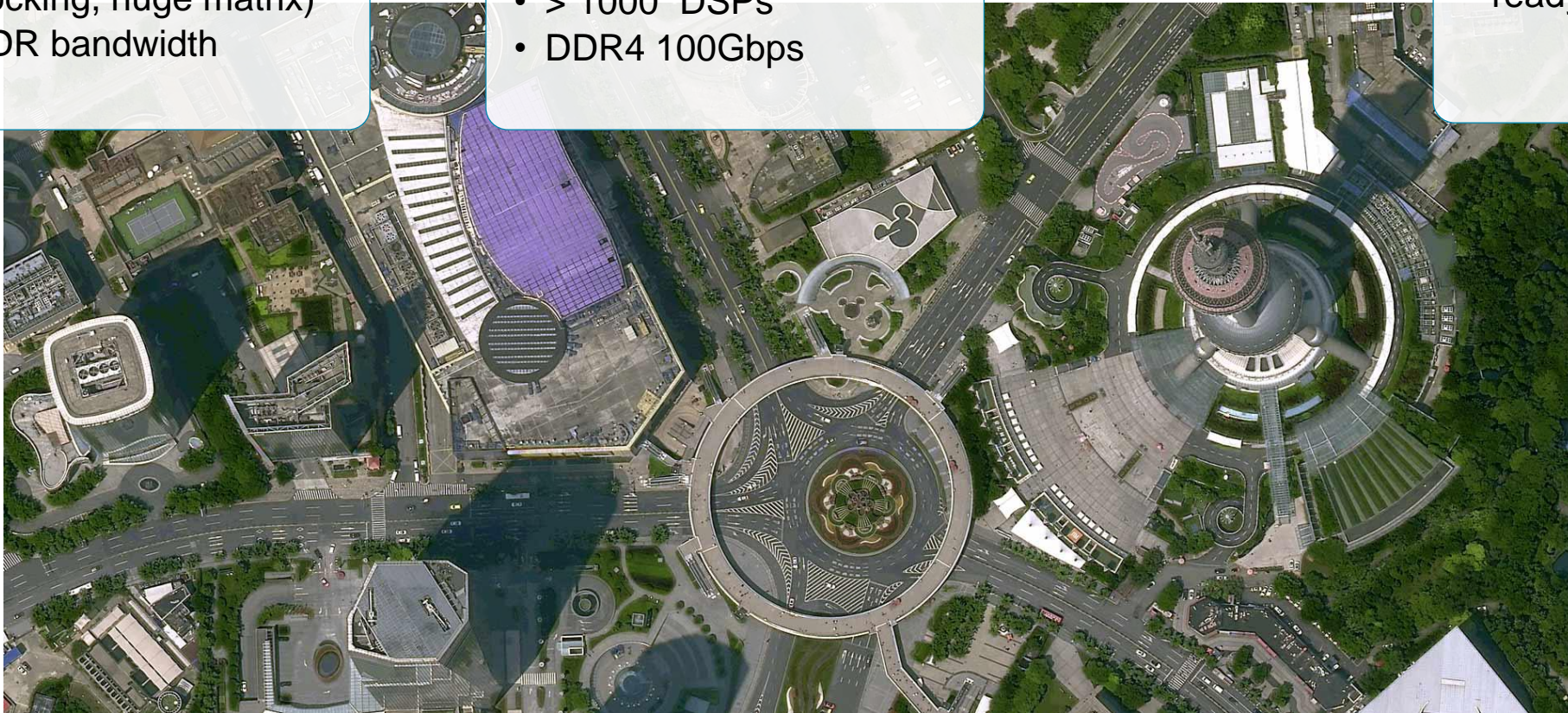
Payload missions requirements analysis
- Very performant FPGA (fast clocking, huge matrix)
- High DDR bandwidth

NG-Ultra suitability ? Confirmed !
- Huge 500k LUT matrix
- > 1000 DSPs
- DDR4 100Gbps

NG-Ultra board for payload processing under development at Airbus
- Ground demonstrator ready for Q4 2023

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How I see my design

How the others see it

What can be concluded considering the overall picture and status on NG-Ultra ?

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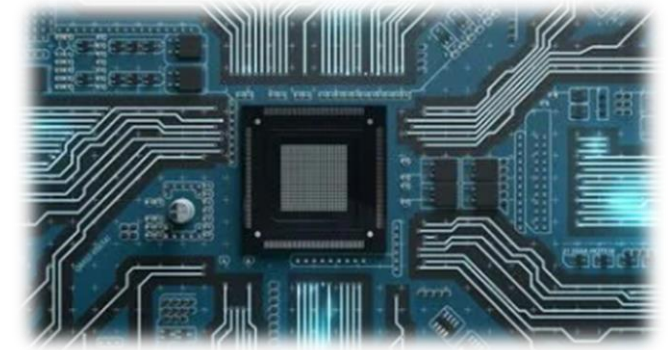
A global trend towards SoC+FPGA

- Initiated by American manufacturers (Zynq, Versal, Intel Agilex…)
- Suiting integration trend of smartphone and automotive industries

European Non-dependence

- **The only Rad Hard European SoC+FPGA**
- High performances breakthrough compared to available European solutions

Airbus, a key player on NG-Ultra chip

- Involved since the beginning
- SoC architecture WP leader
- IP designer (e.g. DDR Ctlr)
- Several boards already under development at Airbus

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Key features

- Huge FPGA matrix + High performance Quad-Core Processing ARM R52 **in a single chip**
  - Processing performances demonstrated @600 MHz on first samples, easy power supply setup, v2 already available
- DDR2/3/4 memory interface with high bandwidth and **very high level of protection**
  - Robust to the loss (SEFI) of one memory device with memory protection still active
- **European component**
  - Key for European non-dependence, ITAR-free
- **Rad Hard**
  - Very promising results from radiation campaign + 28 FDSOI technology intrinsically latch-up immune

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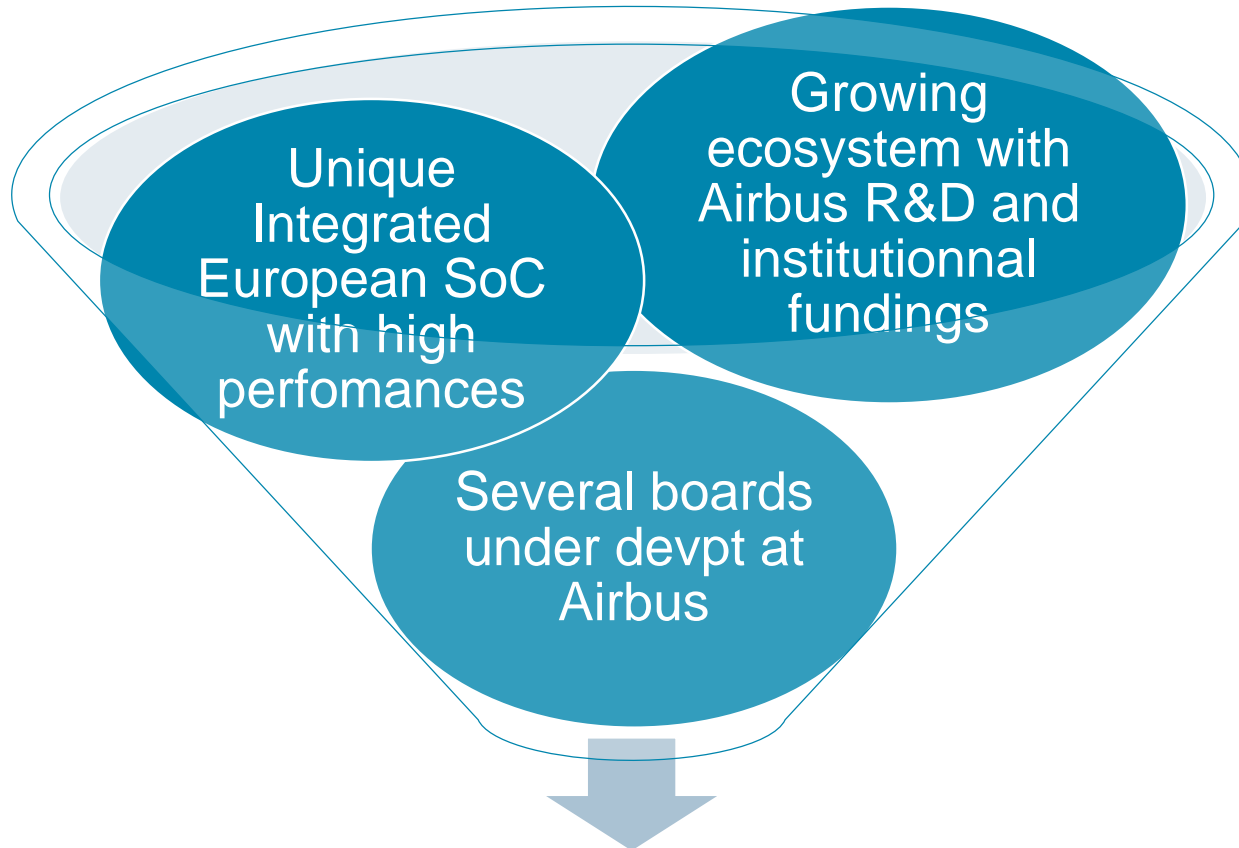
NG-Ultra in a nutshell

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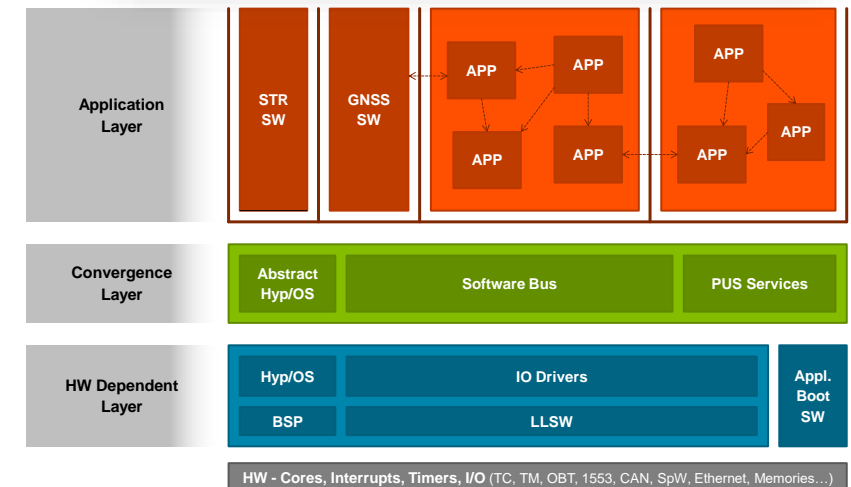
Key points

- Qualification in 2022 (organic) & 2023 (ceramic)
- Official release of **NXmap** in March 2022
  - Very close and fruitful collaboration with NanoXplore
  - Continuous improvement, confidence in tools capacity to meet performance needs for complex designs use cases
- **SW ecosystem** / BSP & BL1 developments
  - Enabler for non recurring cost reduction for future projects
- Several **NG-Ultra boards** now in development within Airbus DS
  - Such as the processing board for the future Airbus NG-Ultra based OBC
  - Allowing Airbus DS to master hardware and software around NG-Ultra (Power Supply, Flash boot, DDR, software devpt…)

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Unique Integrated European SoC with high perfomances

Growing ecosystem with Airbus R&D and institutionnal fundings

Several boards under devpt at Airbus

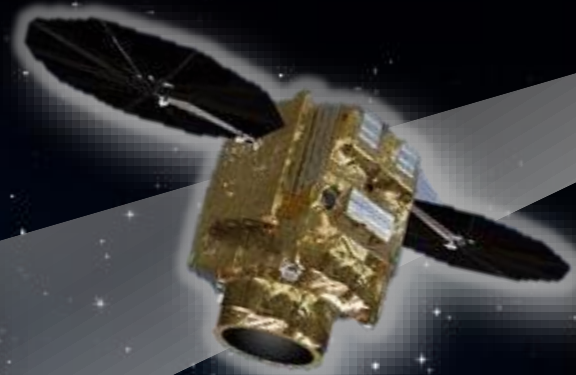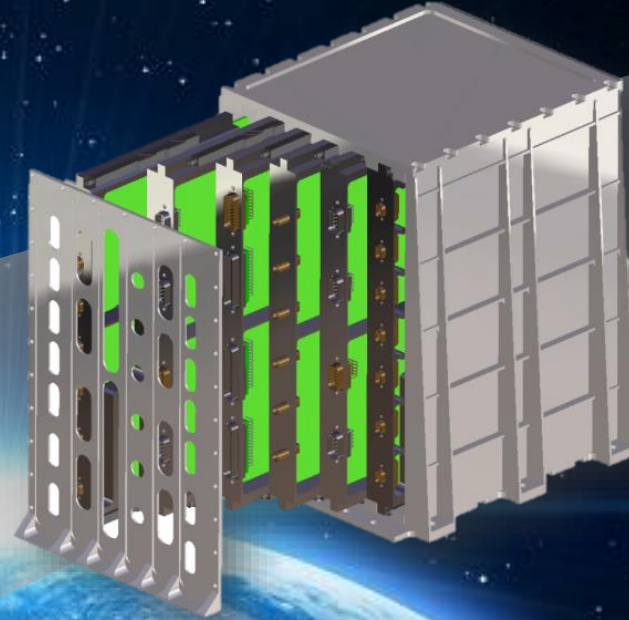NG-Ultra offers key benefits and breakthroughs
It is **suitable** for most of upcoming missions

The rest of the story… is a matter of choice !

Application Layer	STR SW	GNSS SW	APP APP / APP APP	APP APP / APP APP
Convergence Layer	Abstract Hyp/OS	Software Bus		PUS Services
HW Dependent Layer	Hyp/OS	IO Drivers		Appl. Boot SW
	BSP	LLSW		

HW - Cores, Interrupts, Timers, I/O (TC, TM, OBT, 1553, CAN, SpW, Ethernet, Memories…)

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At the leading edge of hardware and software skills, Airbus teams offer unique end to end competences and solutions for Space, such as all activities currently in progress around NG-Ultra

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Thank you

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