TAS - HW/SW EXPERIENCE WITH INTEGRATED OBC FEATURING MULTICORE SOC

ADCSS 2022 – ESA-ESTEC – 27th Oct. 2022

Ivan Cappelluti – Paolo Serri

Date: 27/10/2022
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INTRODUCTION AND HW DEVELOPMENTS

COMPETENCE CENTER HARDWARE ENGINEERING ITALY

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INTRODUCTION – GR740 in the TAS-I OBC Roadmap

/// Thales Alenia Space in Italy decided to adopt the NGMP as core of the Platform OBC Product since 2013

/// This was considered as the “natural” evolution in the Platform OBC roadmap based on ESA supported processors

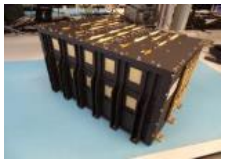
2000

LEONARDO

SPARC-V7 ERC32 TSC-695F 20DMIPS

62 satellites in orbit

ESA programs: CryoSat-2, GOCE, SWARM, Sentinel-1A&B



2010

LEONARDO-3G

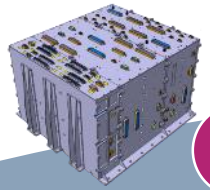
SPARC-V8 LEON3FT

EPICA-NEXT SoC 80DMIPS

84 satellites in orbit

SBNEO Platform

ESA programs: Sentinel-1C&D



2018

IPAC

SPARC-V8 Quad-Core LEON4FT

GR740 SoC 1700 DMIPS

Including GNSS RX

ESA programs: Copernicus, G2SB1, Space Rider

2020

Extension GR740 as common Processor for all Computer Products, including **Mass Memories** and **Payload/Instrument Computer**

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CRONOLOGY 1/3

/// In **2010** TAS-in-Italy started the **definition of a new generation of avionics computer** based on **Multi-Core Processor** in the frame of Italian National programs and internal R&D, in order to **integrate several processing tasks** previously distributed among many computers around the satellite (e.g. Star Tracker processing, GNSS Navigation processing, AOCS Data Fusion) with **benefit in term of avionics platform competitiveness**

/// In **2013** the **ESA NGMP (Next Generation Microprocessor)** has been selected by TAS-in-I as major building block for the new computer generation family

/// May 2013: preliminary draft datasheet of LEON4-NGMP available

/// A trade off was activated in order to compare a solution based on the GR740 SoC from Cobham-Gaisler or on a custom FPGA solution based on use of NGMP IP Core. The final **solution based on GR740 was in the end selected mid-2016**, and detailed board design started.

/// Adopted board name is **Multi-Core Processor Module (MCPM)**

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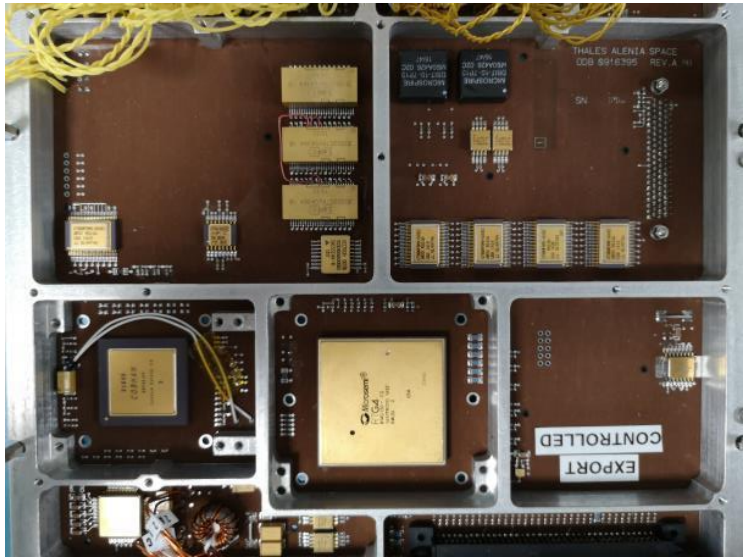
CRONOLOGY 2/3

/// First MCPM based on GR740 has been designed by TAS-in-Italy Competence Center Electronics in **2016** targeted to Platform On-Board Computer with HIREL EEE components

/// TAS-in-Italy GR740 HI-REL board assembled and tested **mid 2017**



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CRONOLOGY 3/3

/// A **new version “COTS” of the board has been developed in 2017/18**, targeted to low cost missions

/// TAS-in-Italy GR740 COTS board assembled and tested **early 2018**

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MCPM BOARD CHARACTERISTICS

/// MCPM is targeted to Platform Avionics Computer functions. According to some limitations imposed by GR740 (not all the SoC functions can be used due to Pin Multiplexing), it has been necessary to help the SoC with an additional companion reprogrammable FPGA (allowing flexibility and configurability).

/// GR740 provided interfaces:

- 8 SPW links (from GR740 router to external users)
- 1 PCI (bridge to COMPANION FPGA)
- 1 MIL-STD-1553B Bus
- 2 CAN Bus
- 2 UART
- JTAG, DSU SPW

/// COMPANION FPGA provided Interfaces:

- Interface to non-volatile large memory (NOR FLASH)
- Clocks generation & Timings management
- GR740 reset and additional Interrupt Controller
- 4 SpW links (for high rate TM/TC/RM internal connection)
- 5 serial link (for low rate TM/TC/RM internal connection)
- Interface to GNSS RF and GNSS Receiver correlators
- Second MIL-STD-1553B Bus

/// MCPM memory budget:

- 64 kB Non-Volatile Boot Memory (maximum allowed due to GR740 Pin Multiplexing limitation)
- 32 MB Non-Volatile Memory (supported by Companion FPGA)
- 512 MB Volatile SDRAM (256 MB in COTS version)

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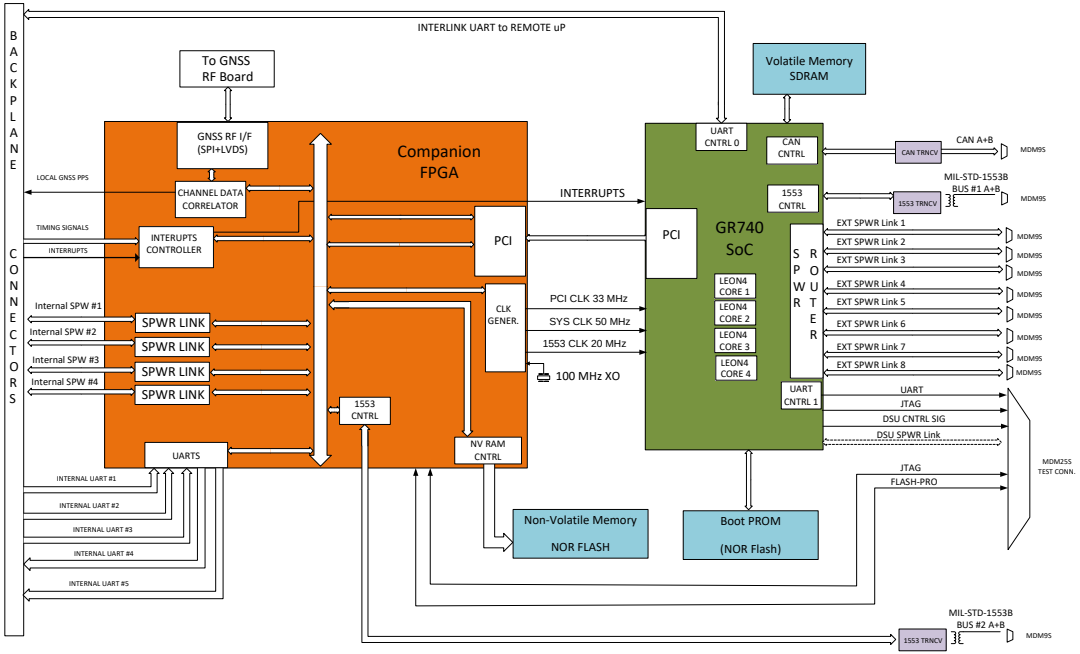
MCPM BOARD



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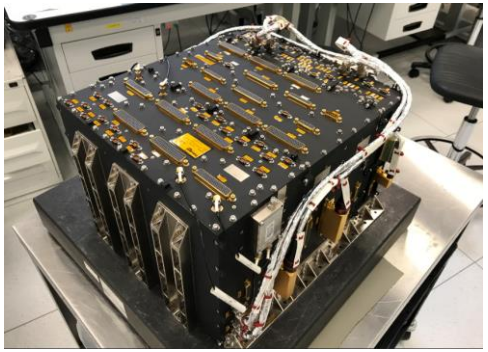
THE IPAC PRODUCT

/// MCPM Board is part of the TAS in Italy state-of-the-art On Board Computer, called **IPAC**

/// IPAC Product development started in **2017**, in the frame of PLATiNO Italian Program, with the goal to improve Platform Management functions:

- Integration and miniaturization
  - **Physically** : significant reduction of volumes and masses, merging several functions in one equipment: Core Computer, Input/Output Terminal, GNSS, Payload Mass Memory.
  - **Processing** : quad-core GR740 allows to execute several tasks formely distributed on different devices: Avionics-Data Handling, AOCS, GNSS, Payload Data Storage
- Modularity and Flexibility
  - Modular and configurable Building Blocks, according to mission requirements (CORE, I/O, PLMM)
  - Re-programmable FPGAs
- Competitiveness
  - Extensive use of **COTS**



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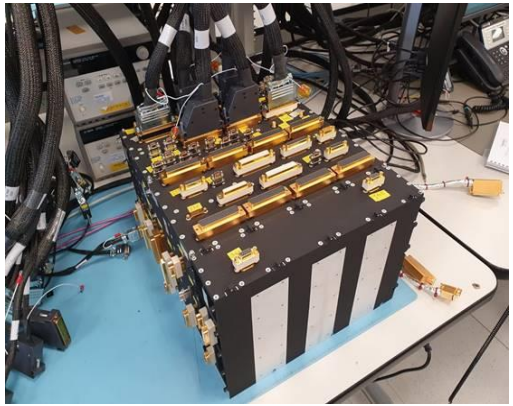
FROM IPAC COTS TO IPAC HI-REL

/// Success of IPAC COTS led to the development of the IPAC HI-REL, based on the same architecture with the following modifications :

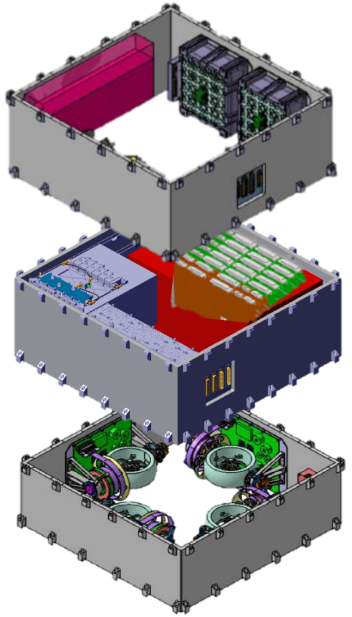
- **FPGA migration** to RTG4 (HiRel) and integration of TM, TC, RM functions in a single device
- Replacement of COTS EEE-Parts with **HIREL EEE-Parts**
- **Radiation hardness** improvement so to make the Product compatible with missions like G2G MEO e Sic3 GEO. This has been done both introducing RadHard parts in the design and modifying mechanics thicknesses
- Introduction of the **Security Function** on a dedicated mezzanine board, so to allow customization of the function according to specific customer requirements.



IPAC FOR NIMBUS

/// Miniaturization and Competitiveness improvement

- Further Mass Reduction
  - Additive manufacturing
  - OBC, I/O, PLMM, GNSS and ICU
- Massive use of PED and COTS
  - GR740 Plastic Package
  - More than 95% of EEE-Parts are PED/COTS
- Inter-Satellite Link Option
  - Interface with Optical ISL
  - Dedicated PLMM
- Co-Processor Option (HPC)
  - Compatibility with different solutions
  - MM shared with ISL Function



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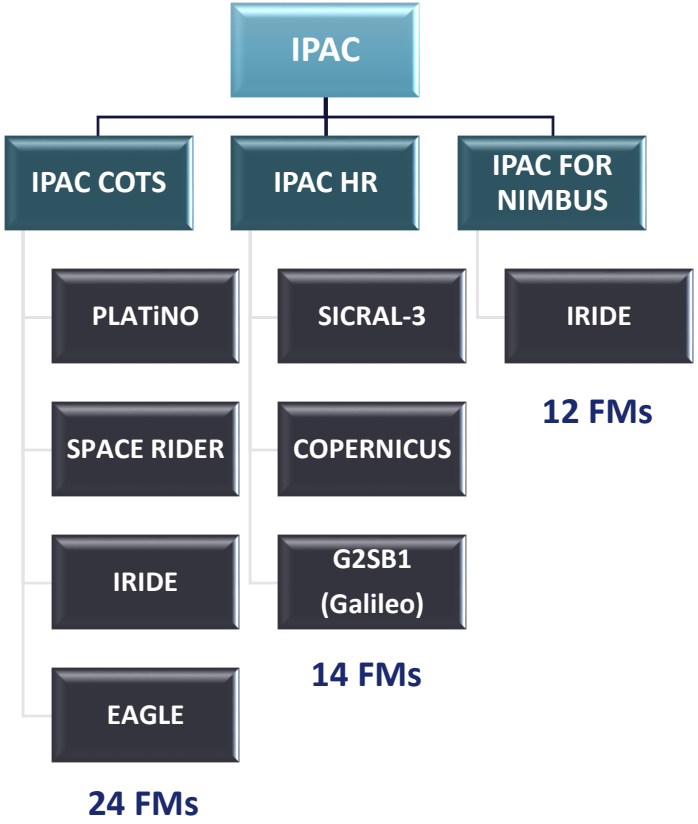
IPAC PRODUCT CONFIGURATIONS



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SW DEVELOPMENTS

COMPETENCE CENTER SOFTWARE ENGINEERING ITALY

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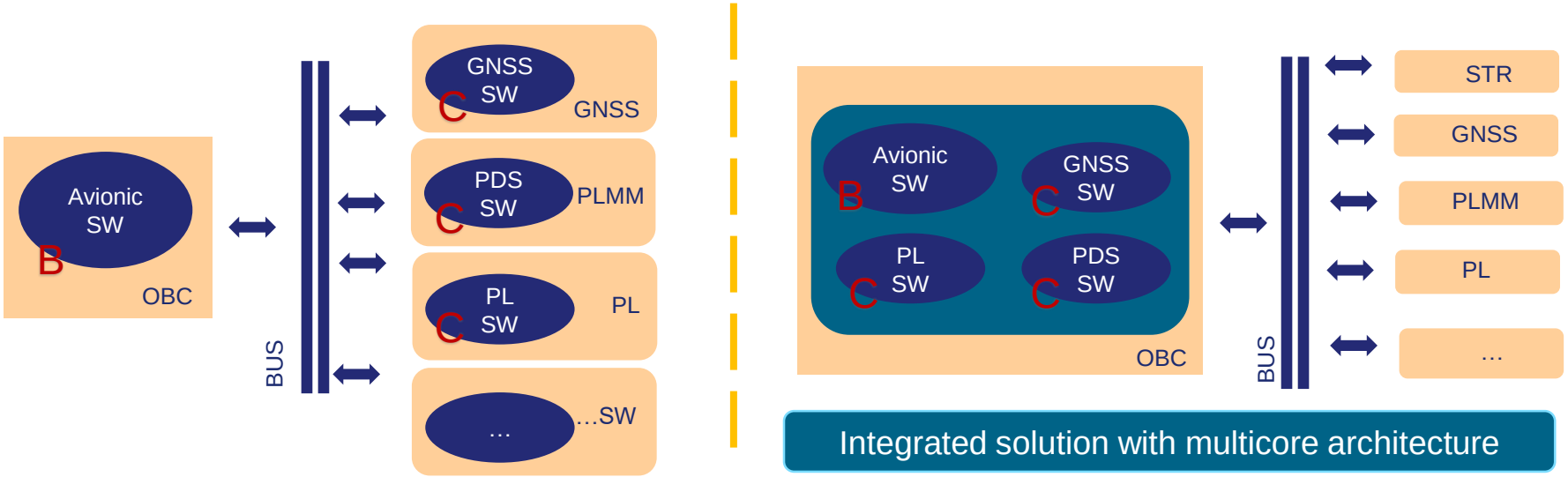
TOWARDS MIGRATION TO MULTICORE ARCHITECTURE

/// Integration of multiple SW on the same multi-core processor

- Reduce HW bill, Increases SW complexity

/// Need to manage different SW cat. level sharing the same resources

- Needs to isolate failure of less critical SW to prevent error propagation
- Time and space partitioning management



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MULTICORE SW INTEGRATION GUIDELINES

/// MAIN GOAL

- Integrate the monocore application over the same multicore processor

/// WAY FORWARD

- Identification HW resources to be shared
  - Link controller
  - Non volatile memories
  - OBC HW resources
- Evaluation of system performance to avoid loss of service
- Identification of a reliable method to isolate failures
- Develop a SW unified approach to develop new application

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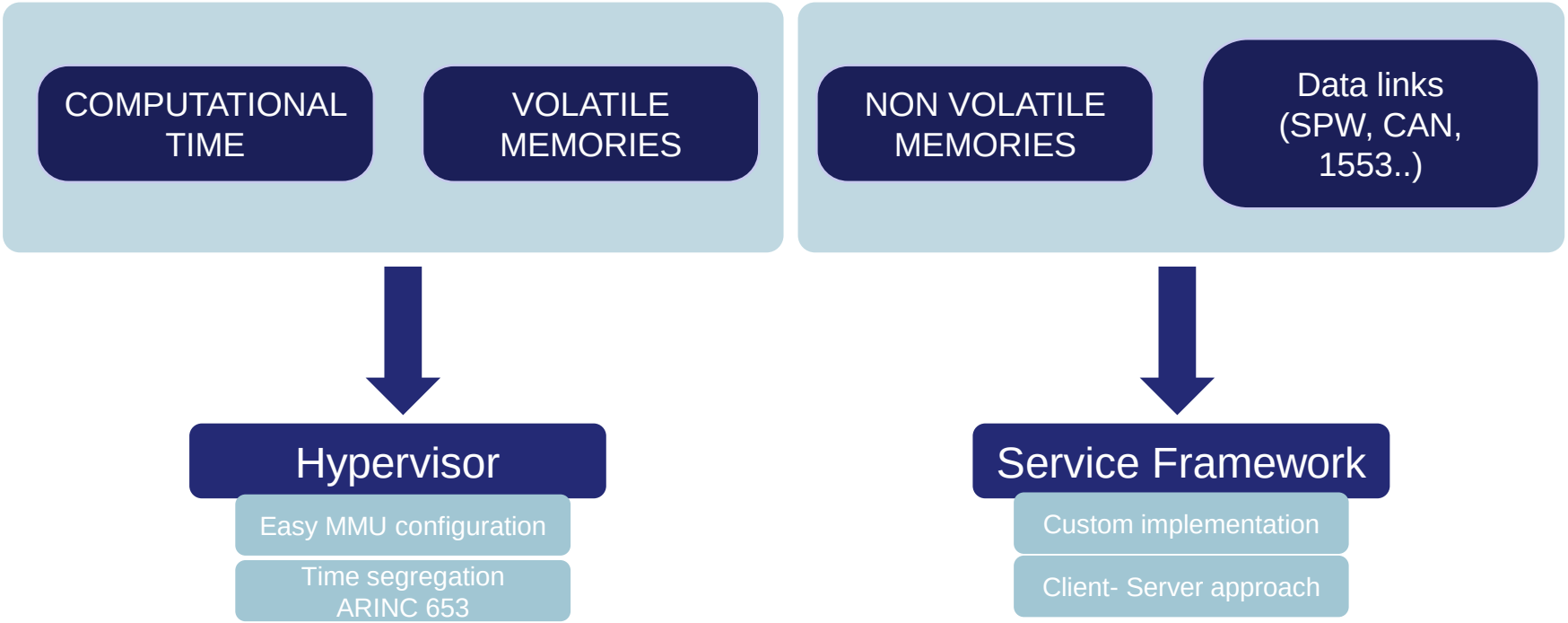
BASIC RESOURCE SHARING



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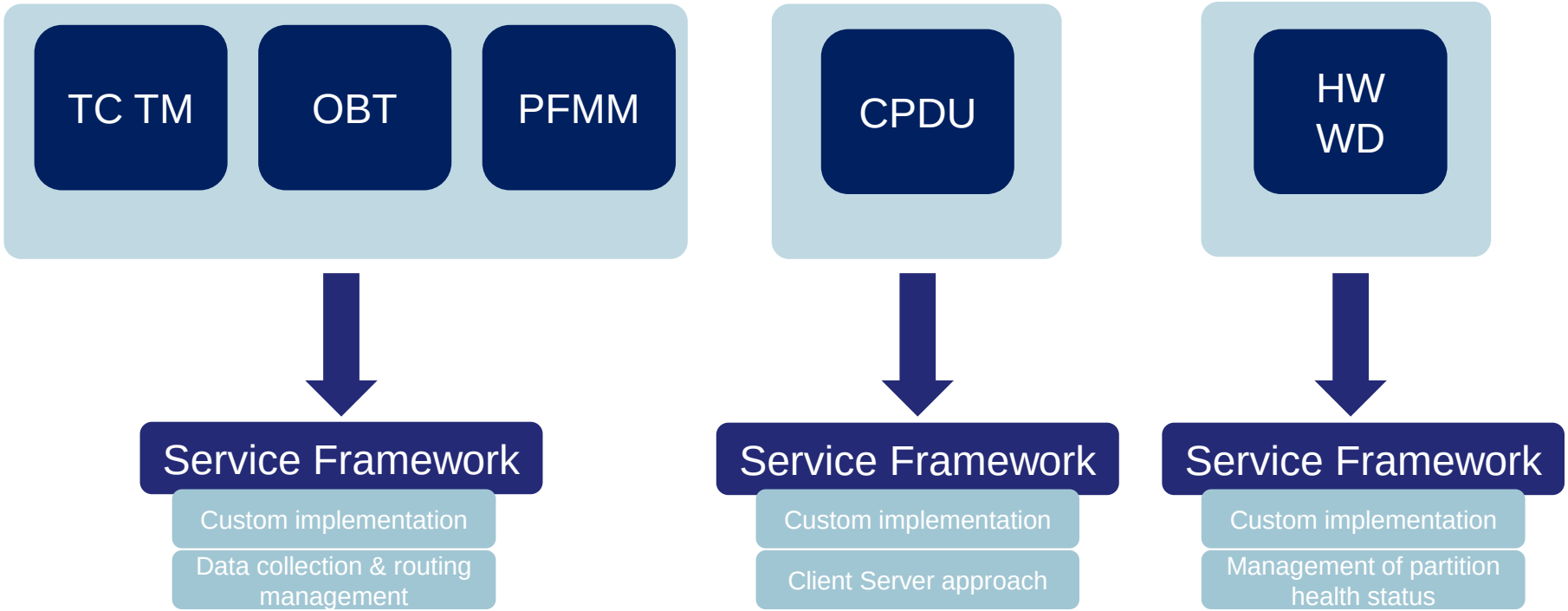
OBC RESOURCES SHARING



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APPLICATION SW DEDICATED RESOURCES

AVIONIC SW

- CAN
- 1553
- GR740 SPW ROUTER
  - In charge of initial configuration
  - 3 dedicated link
- GR740 UART

PL DATA SW

- MCPM SPW
  - 2 dedicated link

PL SW

- GR740 SPW
  - 1 dedicated link

GNSS SW

- FPGA COMPANION
  - GNSS correlator
  - RF board

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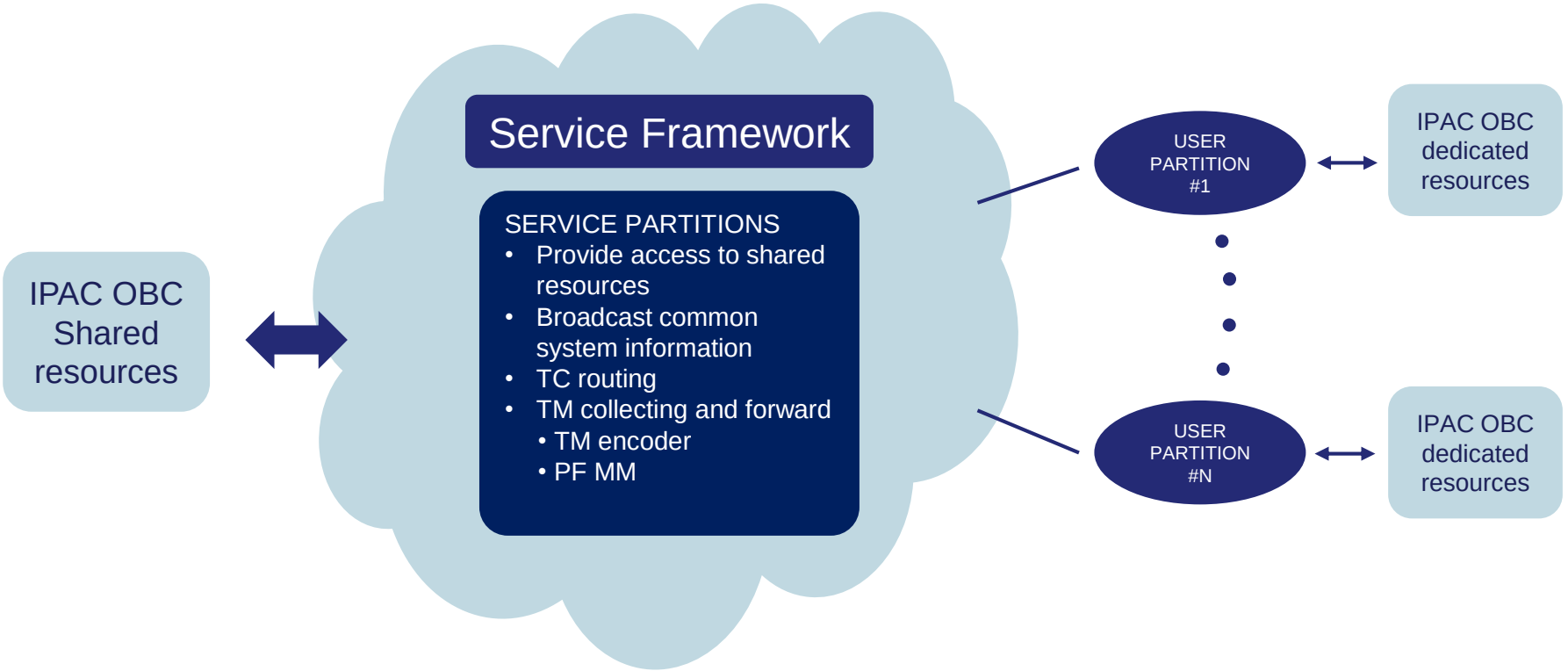
SERVICE FRAMEWORK CONCEPT



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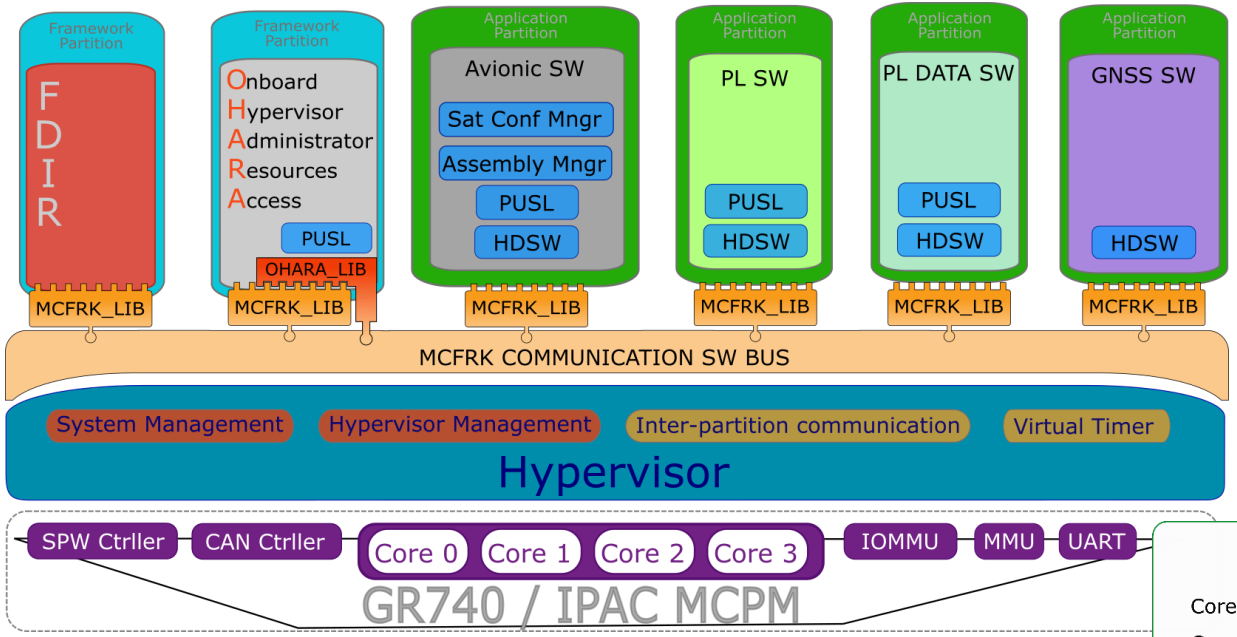
IPAC OBSW ARCHITECTURE



Multicore Architecture

GR740: Quad Core Leon4

Hypervisor Technology

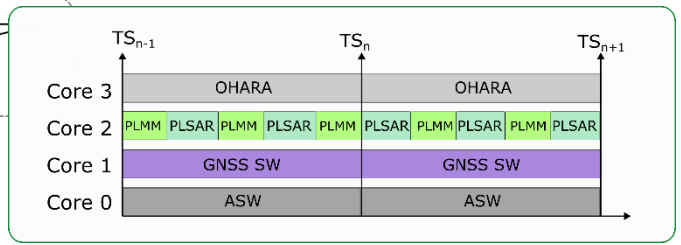
Space and time segregation

Services centralization

MCFRK_LIB: uniform approach

OHARA: server like approach

FDIR: Partition health status



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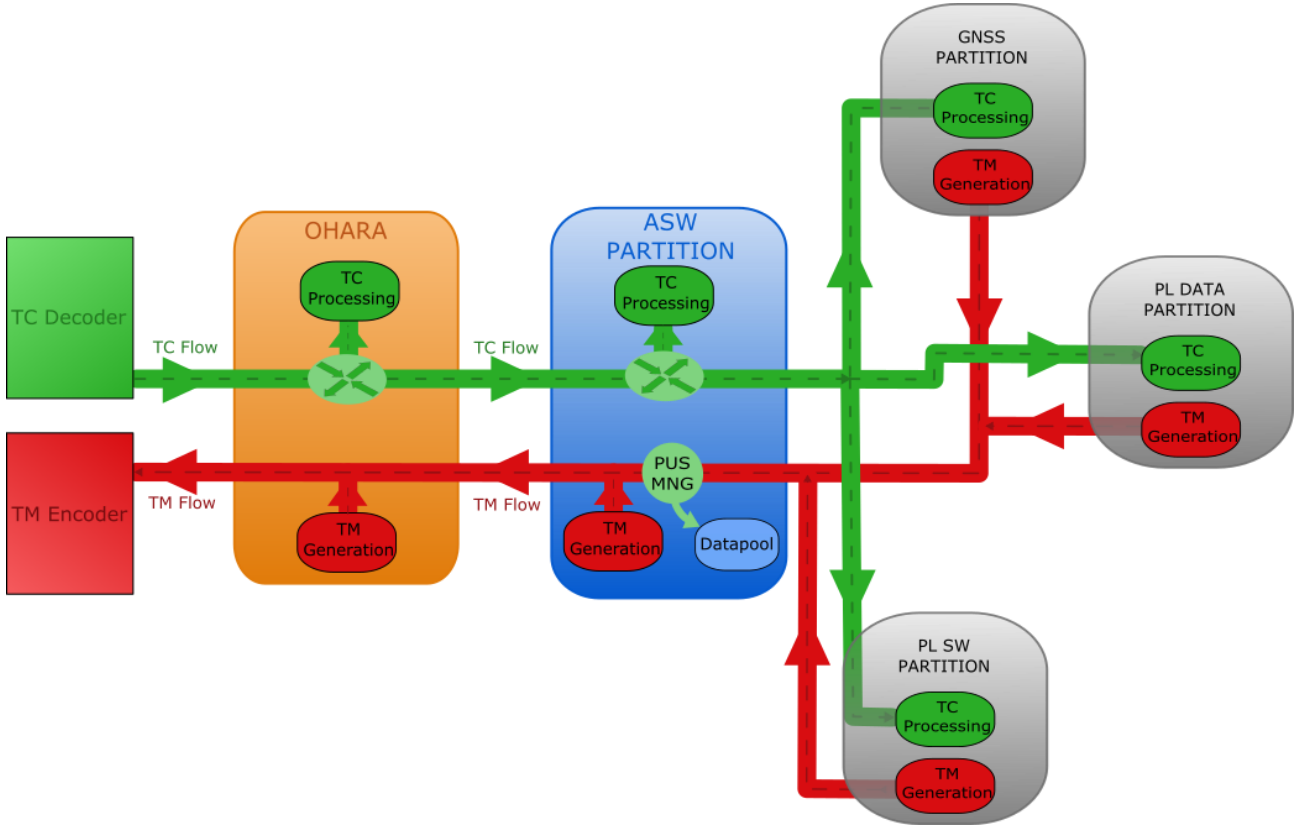
TC AND TM MANAGEMENT



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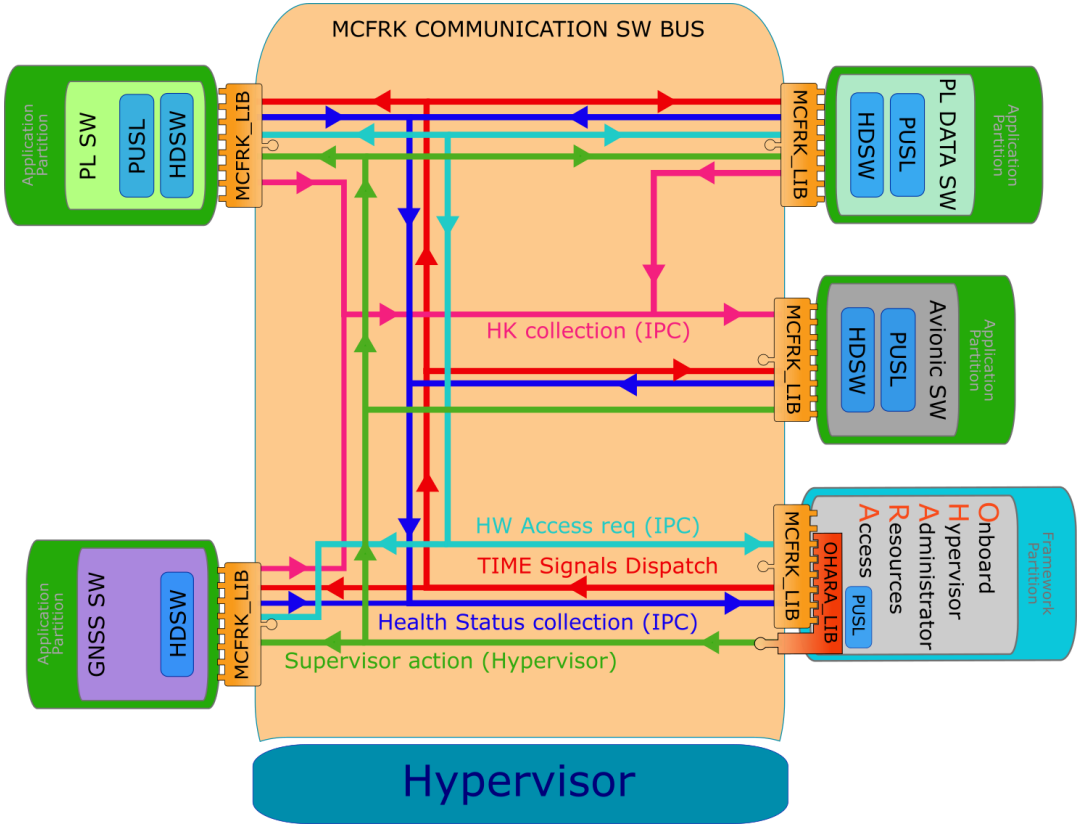
MCFRK SERVICES

- Client Server approach
  - Time information broadcasting
  - Health status collection
  - Watchdog implementation
  - Partition level recovery
  - HW access centralization



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TIME REFERENCE AND SYNCHRONIZATION

/// TIME REFERENCE (OBRT)

- IPAC provides a Time reference synchronized with the Global Reference Time
- The access to this service is exclusive to the Multicore Framework
- The multicore framework broadcast the OBRT to application partition filling the gap between the broadcasting time and the application partition requesting time

/// SYNCHRONIZATION

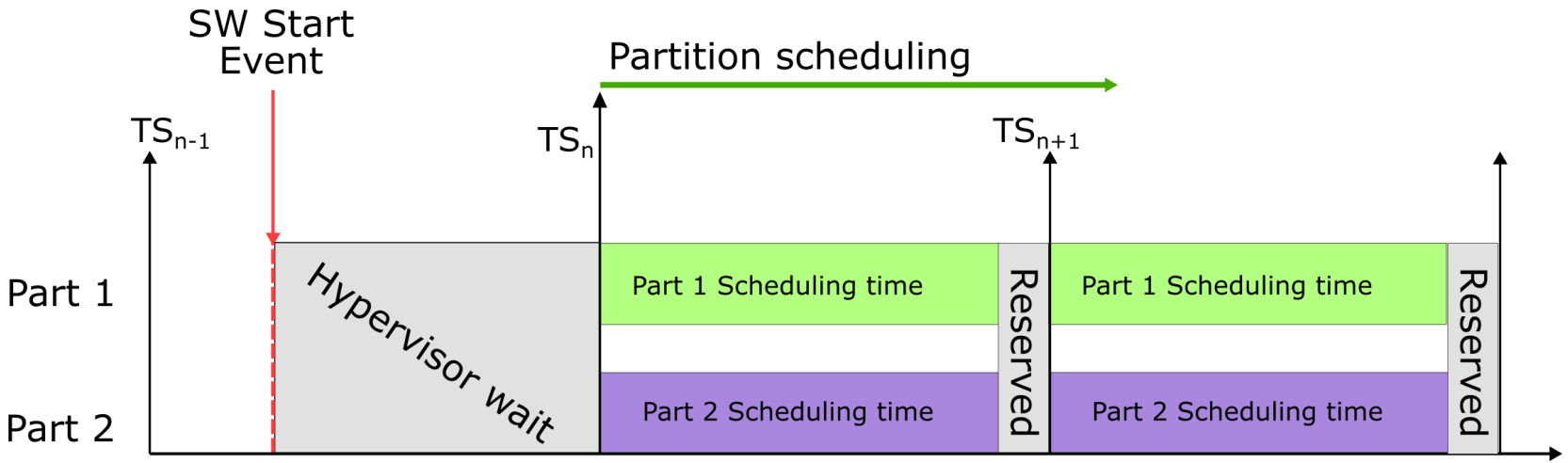
- Some application partition require to be synchronized with IPAC time event
  - ASW: to synchronize system activities and spread time event over the buses
- Time event provided by IPAC are:
  - **1 Hz** – Second pulse
  - **8 Hz** – Time slice
  - **32 Hz** – Real Time Clock

MAJOR FRAME SYNCHRONIZATION

/// Hypervisors provide the capability to synchronize the major frame to an HW event

/// The reserved time required is not compatible with our current GNSS SW application

- The time to be reserved at the end of Major Frame could compromise the GNSS solution precision



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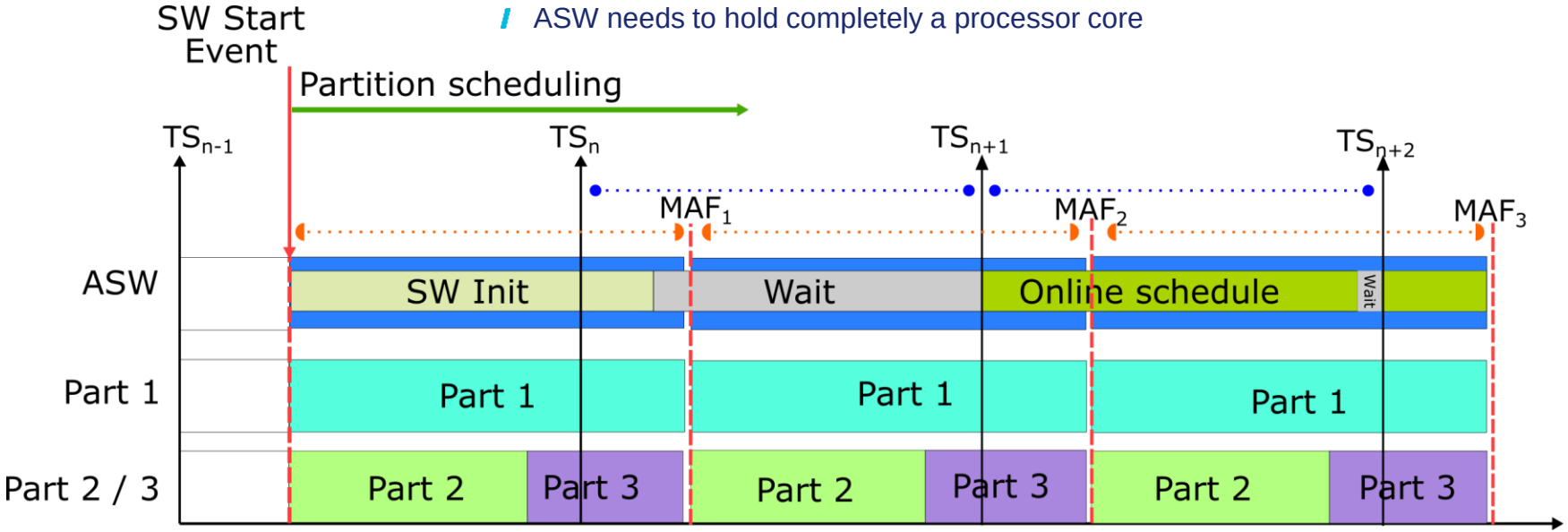
INTERNAL SYNCHRONIZATION

/// The synchronization event is provided to the only partition that need it

- Internal synchronization mechanism is implemented as without hypervisor
- The other partition can derive their synchronization wrt ASW
- ASW needs to hold completely a processor core



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MULTICORE SW RETURN OF EXPERIENCE

/// The hypervisor permits to easily integrate different type of application SW

/// Externalize in dedicated partition services to share OBC resources permits to reuse the Service Framework in different context

- E.g. we are working on sharing CCSDS CFDP protocol custom accelerator

/// Abstract the hypervisor services and develop API to access to the Service Framework permits to:

- Adapt different hypervisor without impact application SW
- Offer to eventual external application developer a well known environment
- Homogenize the application design and simplify the hypervisor configuration

/// The GR740 offers enough flexibility and performances to realize the described architecture

- E.g. the AMBA split configuration that enables a second CPU to still access the L2 cache while a cache miss is handled for another CPU