Linux goes to space in Ultra7

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NanoXplore Overview

- **Created in 2010** by three veterans of semiconductor industry with long experience in design, test and debugging of e-FPGA cores. *(MetaSystem, M2000, Abound Logic, then NX)*
- **2014 : start of FPGA**
- **2016 : SoC FPGA activities**
- **Fabless** semiconductor company located in France
  - Sevres : Headquarter – more than 70 R&D engineers
- The company is focusing on developing rad-hard FPGA qualified for space applications
- NX fully supported by

European SoC/FPGA, main stakeholders

Development (define, design, verify, Bring-up), SDK, FPGA tools, Sales and Customer Support

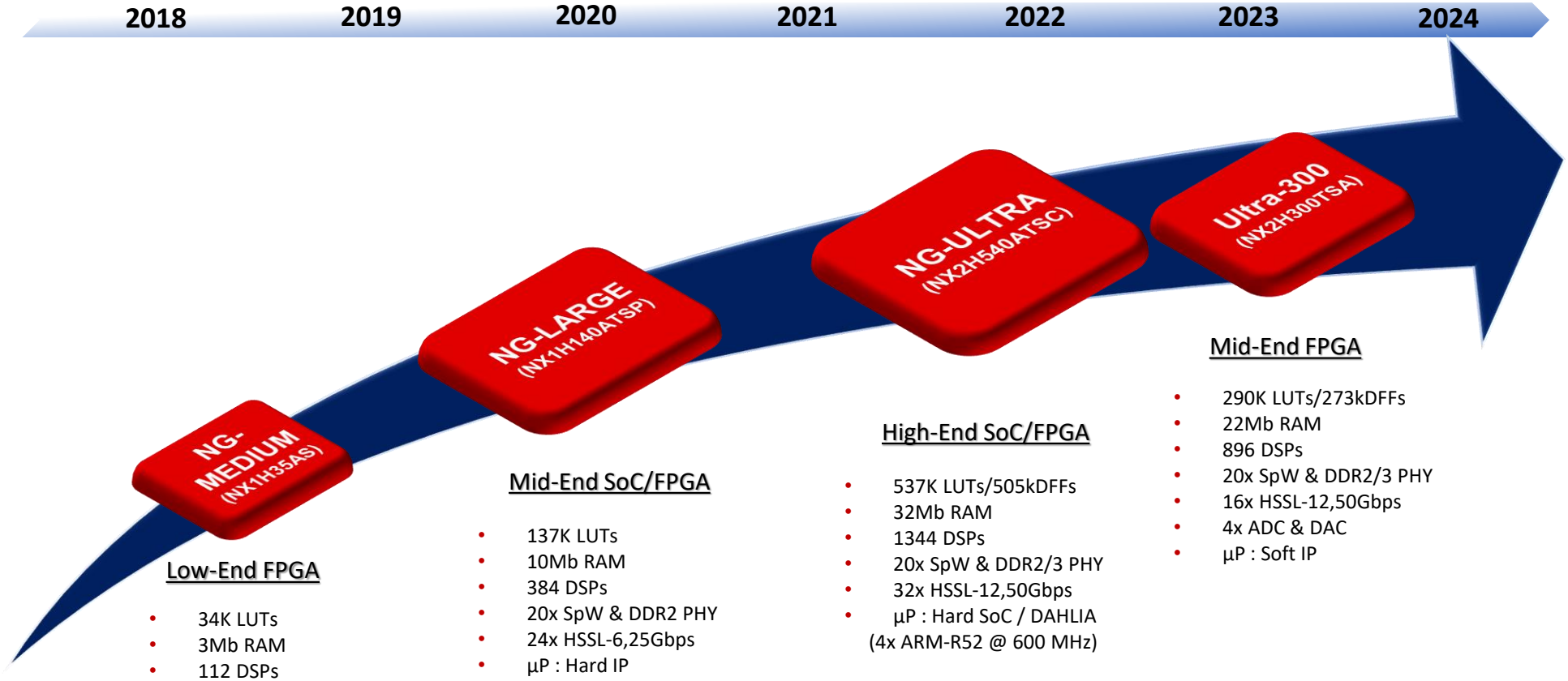
Foundry (manufacture), Packaging (Te2V involved in NG-LARGE), Test, Eval&Qual

Alpha customers for all BRAVE FPGAs and SoC/FPGAs (requirements definition, participation in review milestones, first users of the design kits, etc.)

For NG-ULTRA: also part of the development team

R&D activities contracts mainly from

Products offer Rad-Hard SoC/FPGA family



Low-End FPGA

- 34K LUTs
- 3Mb RAM
- 112 DSPs
- 16x SpW & DDR2 PHY
- No HSSL
- µP: Soft IP (Leon3 @ 35MHz)

Mid-End SoC/FPGA

- 137K LUTs
- 10Mb RAM
- 384 DSPs
- 20x SpW & DDR2 PHY
- 24x HSSL-6,25Gbps
- µP : Hard IP (ARM-R5 @ 200 MHz)

High-End SoC/FPGA

- 537K LUTs/505kDFFs
- 32Mb RAM
- 1344 DSPs
- 20x SpW & DDR2/3 PHY
- 32x HSSL-12,50Gbps
- µP : Hard SoC / DAHLIA (4x ARM-R52 @ 600 MHz)

Mid-End FPGA

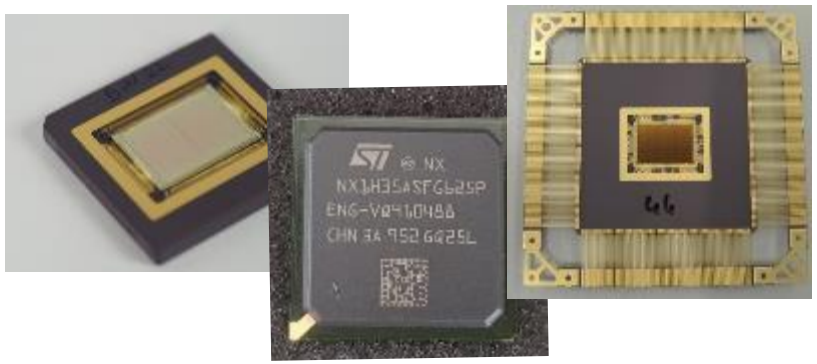
- 290K LUTs/273kDFFs
- 22Mb RAM
- 896 DSPs
- 20x SpW & DDR2/3 PHY
- 16x HSSL-12,50Gbps
- 4x ADC & DAC
- µP : Soft IP

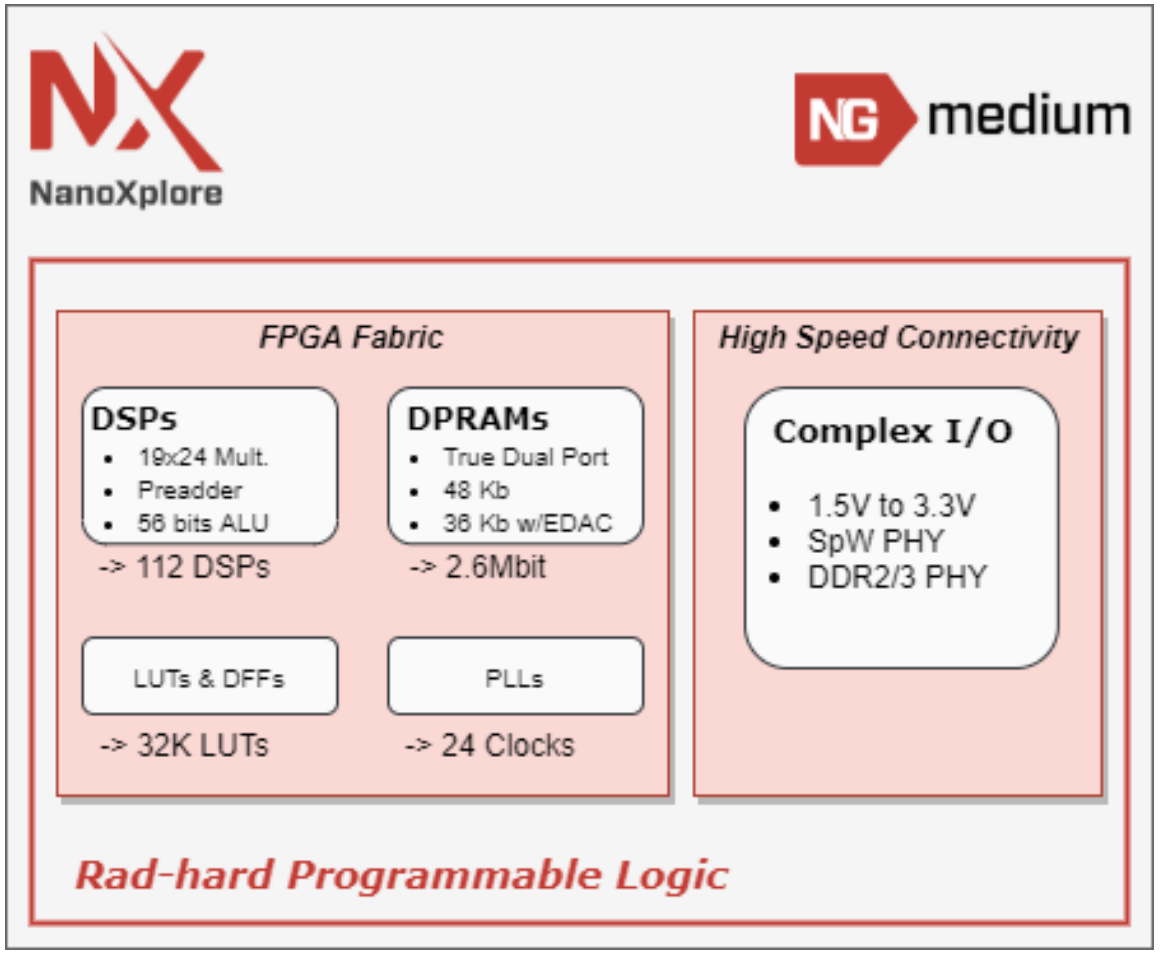
65 nm | 28 nm

NG-MEDIUM Overview

65nm CMOS

- Rad-Hardened By Design SRAM-based FPGA
- 32K LUT&DFF density
- 112 DSP
- 2.6Mb DPRAM
- Up to 374 User I/O
- SpW & DDR2 PHY & HSSL





NG-MEDIUM Qualification

ESCC9000 qualified (CQFP352 & CLGA625)

esa

European Space Agency
Agence spatiale européenne

Certificate of Qualification No. 382

This is to certify that NanoXplore, Sèvres , France has been qualified by ESA for the supply of Integrated Circuits, Silicon, Monolithic, 35KLUT Radiation-Hardened FPGA (NG-Medium) , for use in ESA space programmes, according to ESCC Generic Specification 9000 and associated Detail Specification 9304/010 as recommended by the Space Components Steering Board.

This certificate is valid until August 2024.

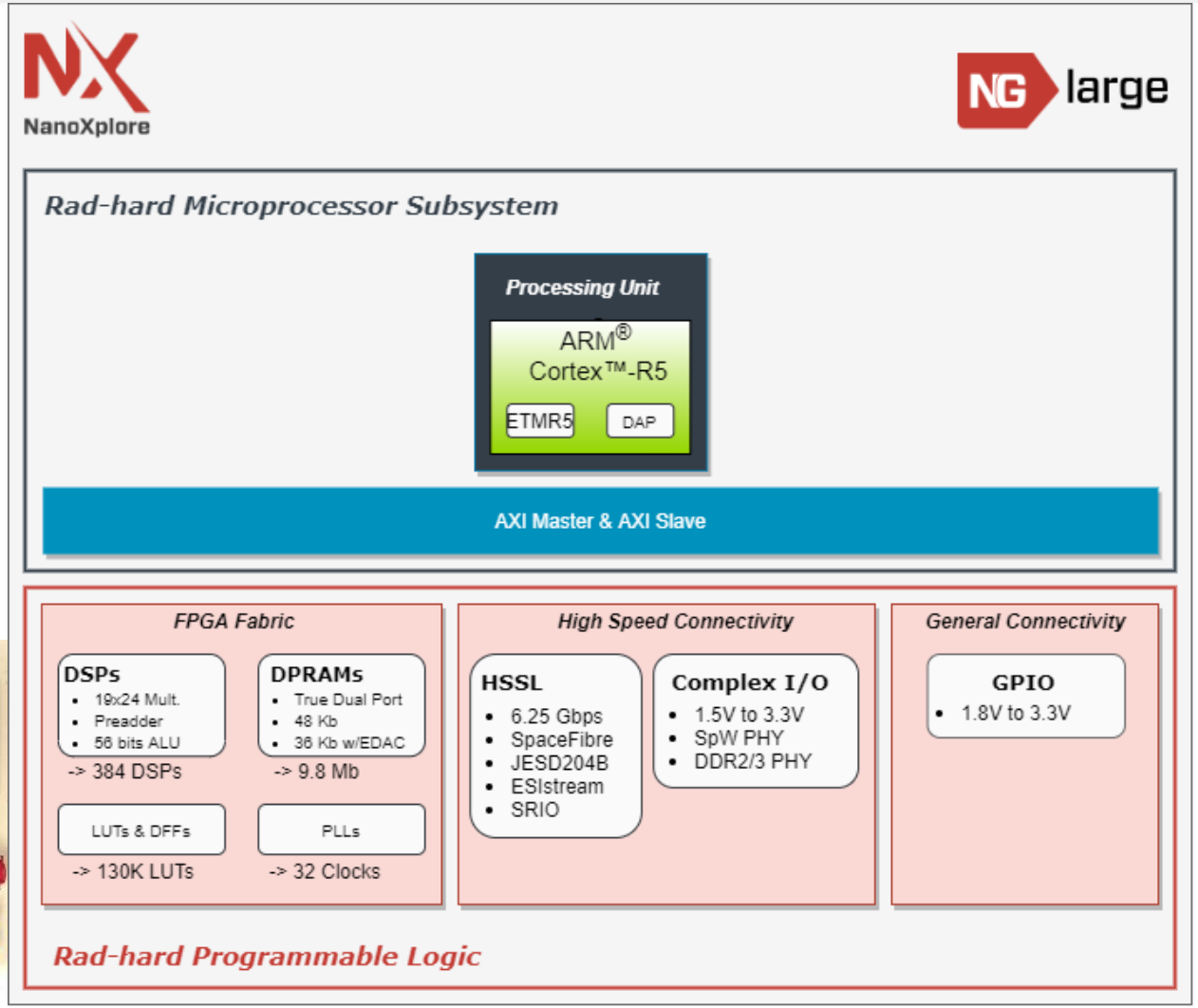
Head of the Product Assurance
and Safety Department

Date
31 August 2022

NG-LARGE Overview

65nm CMOS

- First FPGA with isolated CPU
- Rad-Hardened By Design SRAM-based FPGA
- ARM Cortex-R5
- 130K LUT&DFF density
- 384 DSP
- 9.8Mb DPRAM
- Up to 684 User I/O
- SpW & DDR2 & HSSL



NanoXplore

NG-ULTRA

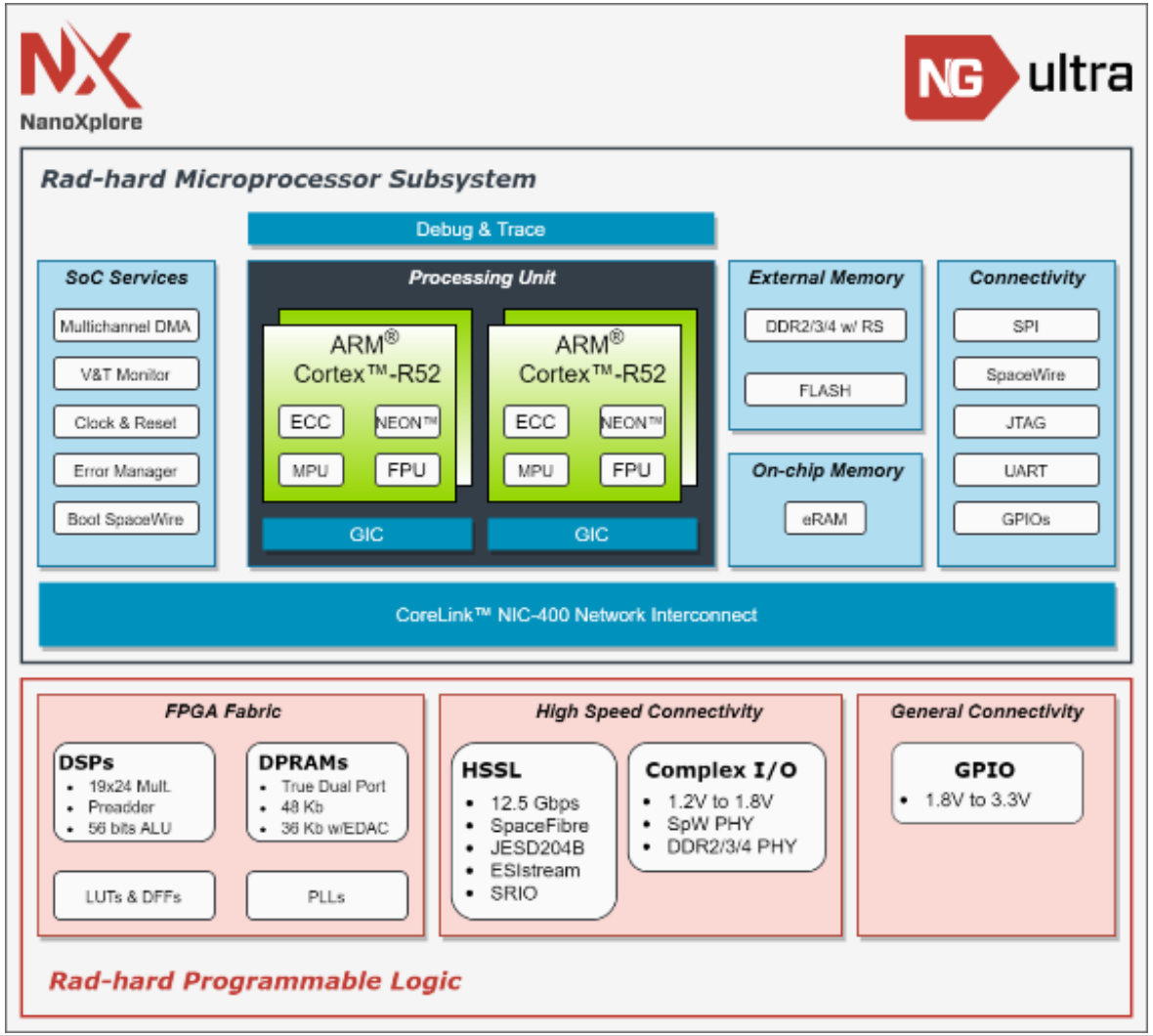
Overview

NG-ULTRA Overview

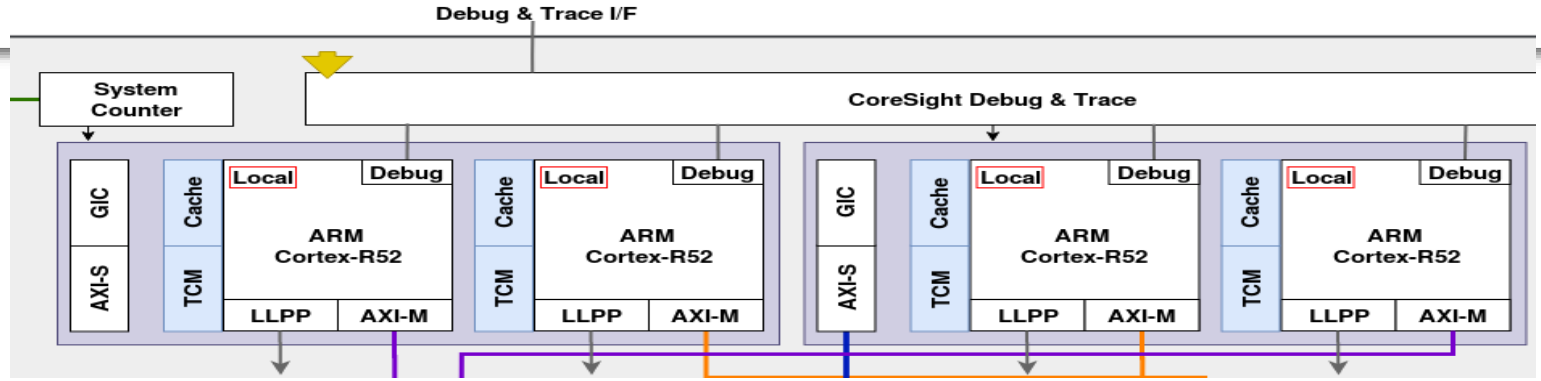
28nm FD-SOI

- Rad-Hardened SoC/FPGA
- Quadcore ARM R52 @ 600MHz each
- Up to 4200 DMIPS
- 2MB eRAM with ECC
- 16 DMA channels
- FLASH TMR

- ~500K LUT&DFF
- 1344 DSP
- 32Mb DPRAM
- Up to 740 User I/O
- SpW & DDR2/3/4 & HSSL
- Radiation performances
  - TID 50krads(Si)
  - SEL and SEE immune



Cortex-R52 in NG-ULTRA



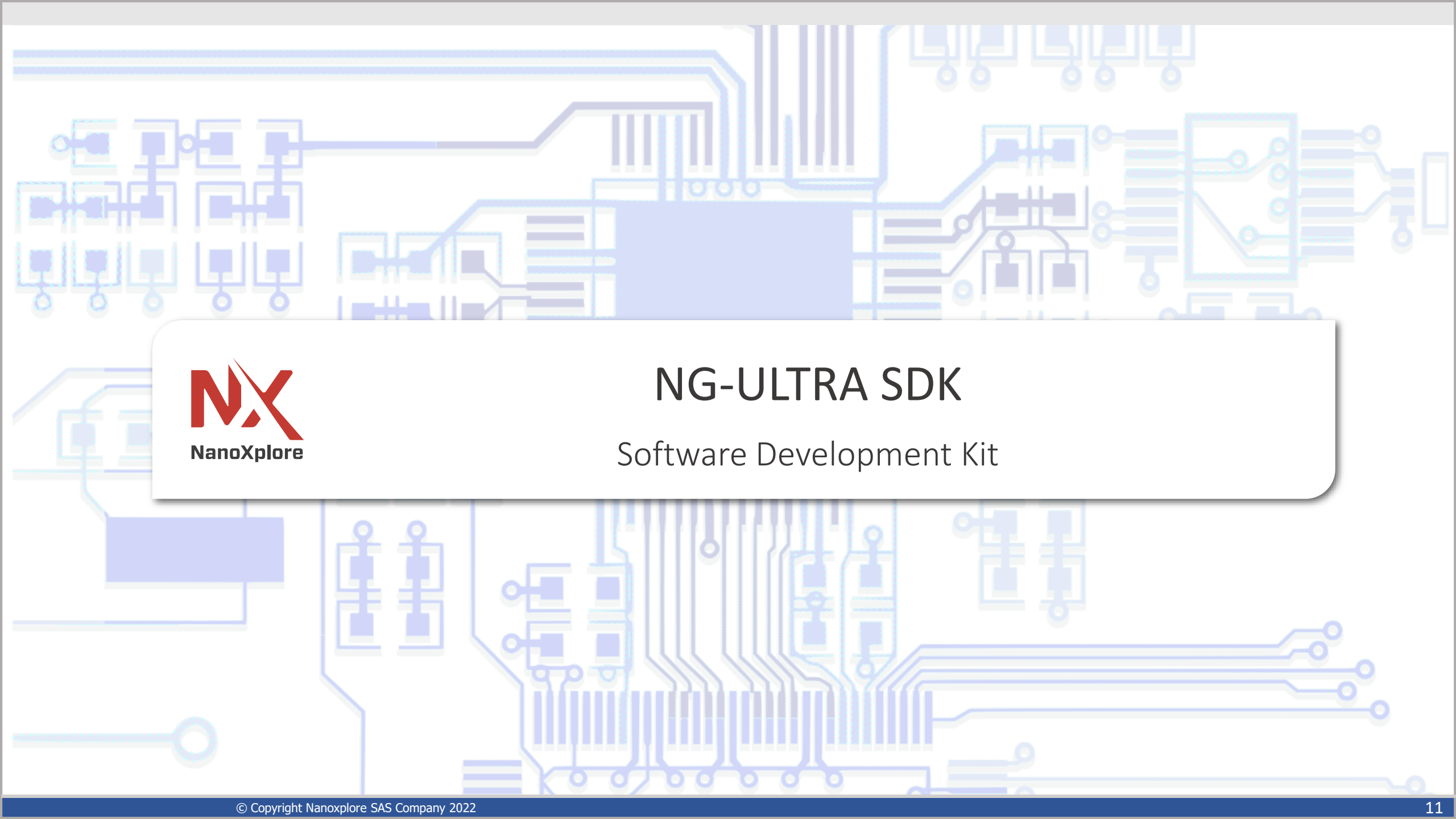
Cortex-R (ARMv8-R):

- Fast response
- Optimised for High-performance
- Hard real time application
- ECC protected memory
- 2.2 DMIPS/MHz @ 600MHz

- eRAM : 2MB with ECC

Debug using OpenOCD
Debug and TRACE supported by LAUTERBACH

Cortex-R52	
Data cache size	32KB
Instruction cache size	32KB
Advanced SIMD and floating-point	SIMD
ATCM	128KB (single-cycle access)
BTCM	128KB (single-cycle access)
CTCM	128KB (single-cycle access)
AXI4 Master	128 bits
AXI4 Slave	128 bits
AXI4 LLPP	32 bits



NG-ULTRA SDK

Software Development Kit

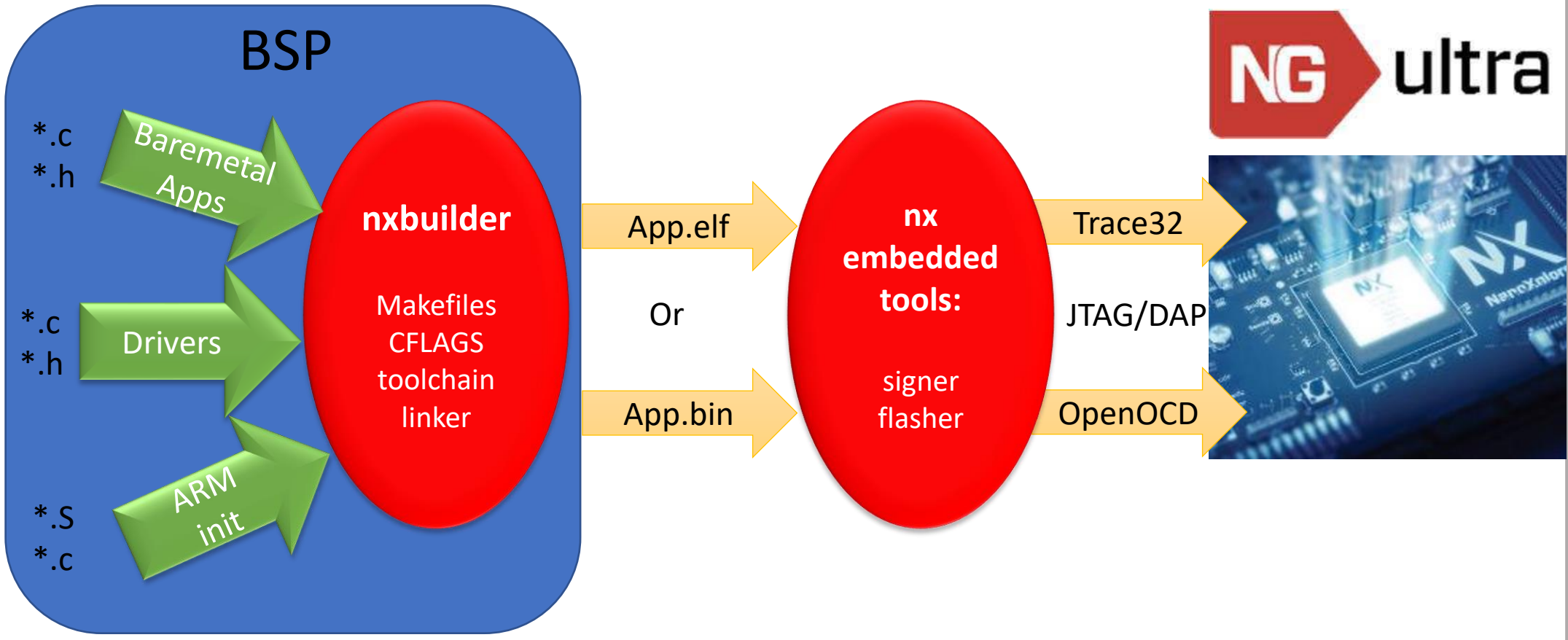
NG-ULTRA BSP

Board Support Package

- Generic build system for embedded software
  - Including Makefiles and generation instructions
  - Generic linker script
- Ready to use drivers
  - Flash, Clock & Reset, DMA, DDR, UART, eRAM, GIC…
  - ARM R52 init (crt0, handler, MPUs, stack…)
  - HAL and Helpers
- Example applications & demo

➢ Easy to use

Workflow



NX Embedded Tools

For NG-ULTRA

- Debugging facilities
  - Lauterbach (debug & trace)
  - OpenOCD support
- Flash programmer
- Bitstream loader
- Memory dumper using DAP (debug access port)
- BL1 signer
- Read temperature sensor

➢ More on the way...

NG-ULTRA BSP Drivers

Qualification

ARM R52:
Crt0, ASM,
Float, MPU

GiCv3

UART

Flash:
TMR, seq

Clock & Reset

eRAM:
Padding,
scrubbing

Qualified Code

System Counter

DDR & Reed Solomon

DMA

Led & GPIO

Coming qualified drivers

SpaceWire

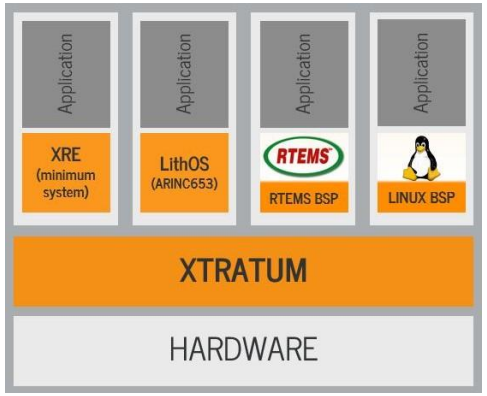
UART

Watchdog

SoC Monitor

OS Supports

For NG-ULTRA

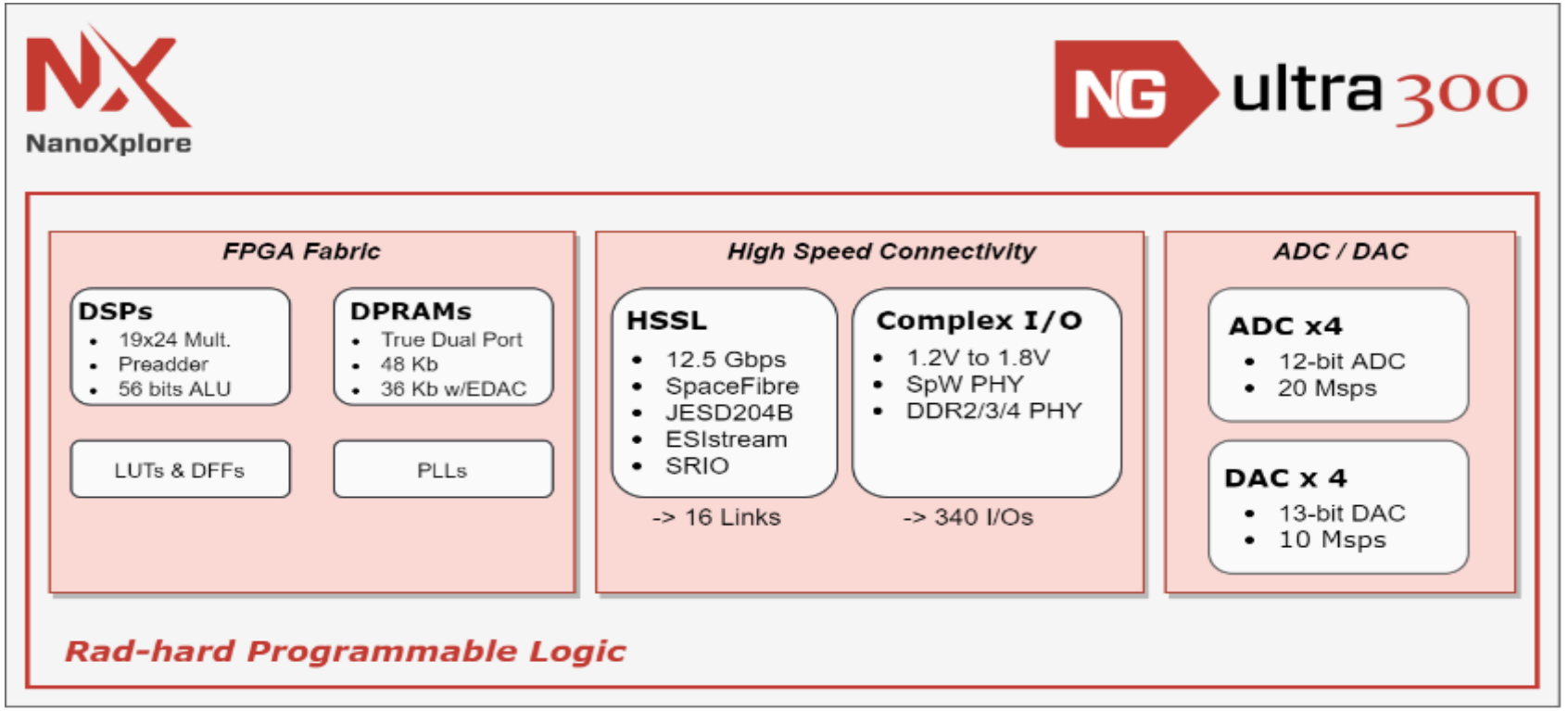


ULTRA 300 Overview

28nm FD-SOI

- Small Form factor ➔ FCBGA-484
- High pin count ➔ FCBGA-1152 and CLGA/CCGA-1152
- 300KLUT & DFF, 22Mb RAM and 900DSP blocks
- Embedded ADCs & DACs

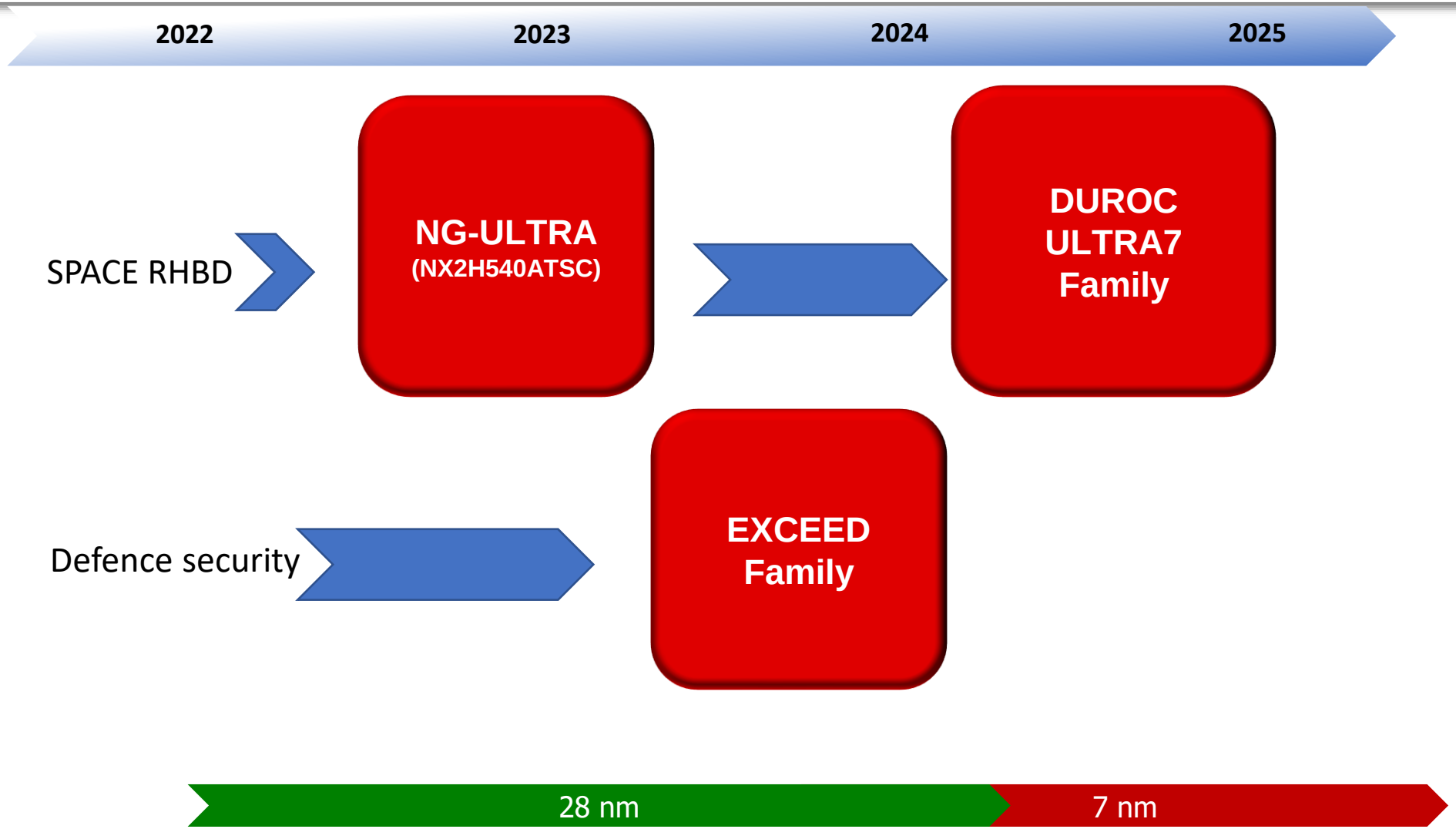
Low-Cost
Rad-Hardened
Low-Power



Excellent candidate for Companion Chips

SoC FPGA family

Roadmap



New Space Challenges

Embedded data center satellite

- Increase onboard processing
- Very high performance processing
- Tens of thousands of DMIPS
- Rich operating system -> Linux for Space
- Easy reuse of existing software
- Multimedia processing
- Improve power consumption
- Save data throughput between space and earth stations

From Real time to Application Processors

Take best of both worlds

NanoXplore

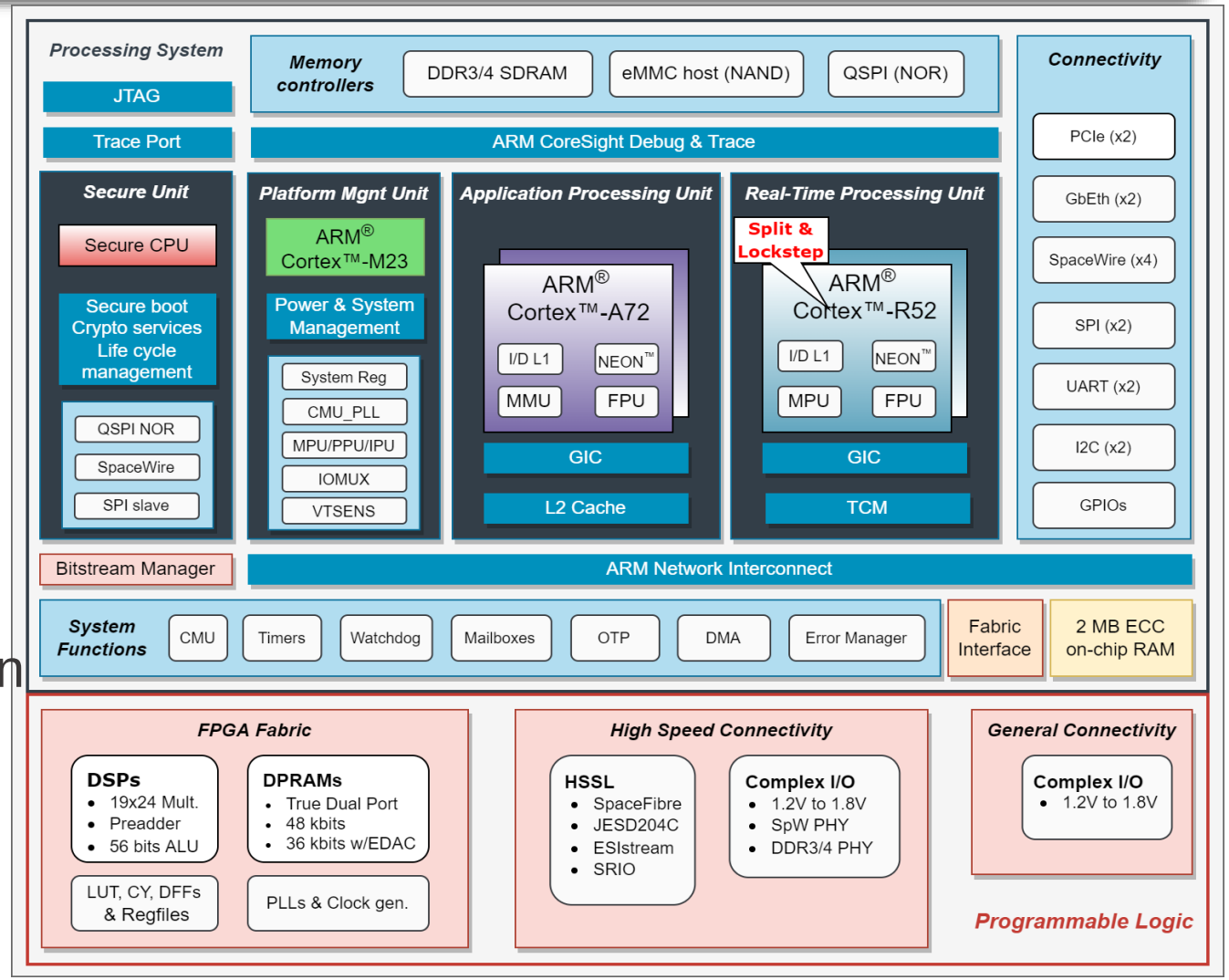
ultra 7

Overview

DURO ULTRA7 Overview

7nm FinFET technology

- Rad-Hardened SoC/FPGA
- Dual ARM R52
- Dual ARM A72 (32/64 bits)
- Boot CPU M23
- Secure Unit CPU
- 2MB eRAM with ECC
- DMA channels
- FPGA size under discussion



DURO C ULTRA7 features

- **Secure Unit**
  - Secure boot
  - Cryptographic services
- **Platform Management Unit**
  - System initialization
  - Low power processing
- **Application Processing Unit**
  - Rich OS applications
- **Real-time Processing Unit**
  - Deterministic real-time applications
- **System functions**
  - DMAs
  - CoreSight Debug & Trace
  - Secure & User OTP
- **Memories**
  - eRAM, TCM
  - DDR SDRAM, QSPI NOR Flash, eMMC
- **A set of standard peripherals**
  - PCIe, Eth, SpaceWire, SPI, UART, I2C, GPIO

Development strategy

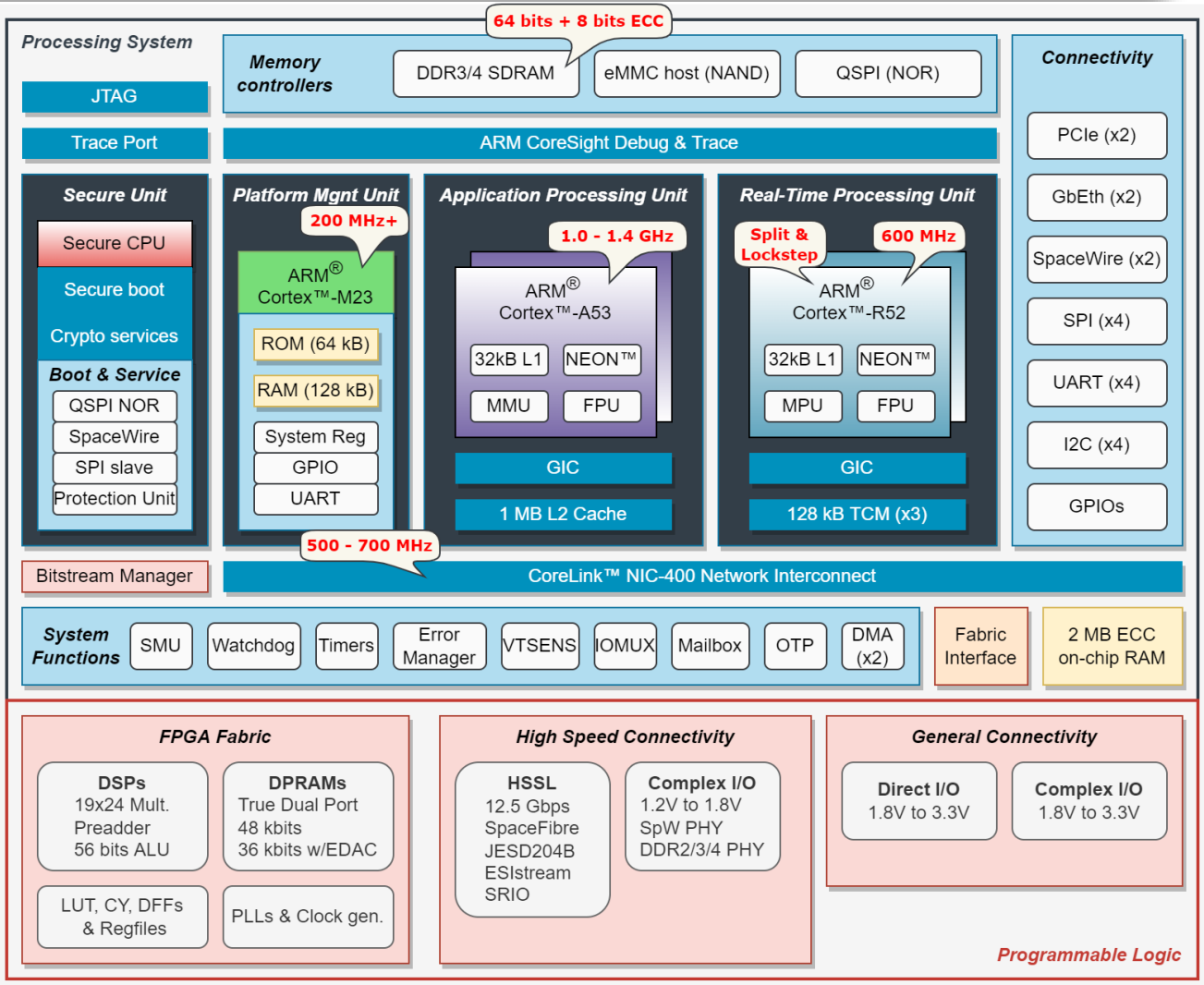
Intermediate strategy

- 7nm test chip with basic HW cells
- No rad hard 28nm SoC with Cortex-A CPU
  - Secure hardware implementation
  - Accelerate Software implementation
  - Secure boot definition and validation
  - Low power optimization
- Prototyping Platform before tape-out

Exceed Overview

No rad hard 28nm FDSOI technology

- No rad-Hardened SoC/FPGA
- Dual ARM R52
- Dual ARM A53 (32/64 bits)
- Boot CPU M23
- Secure Unit CPU
- 2MB eRAM with ECC
- DMA channels
- FPGA size under discussion



Time To Market

HW/SW prototyping

RTL
- CPUs
- IPs
- TOP

SW
- Secure BootROM
- CPU's init
- Drivers

Debug Probes

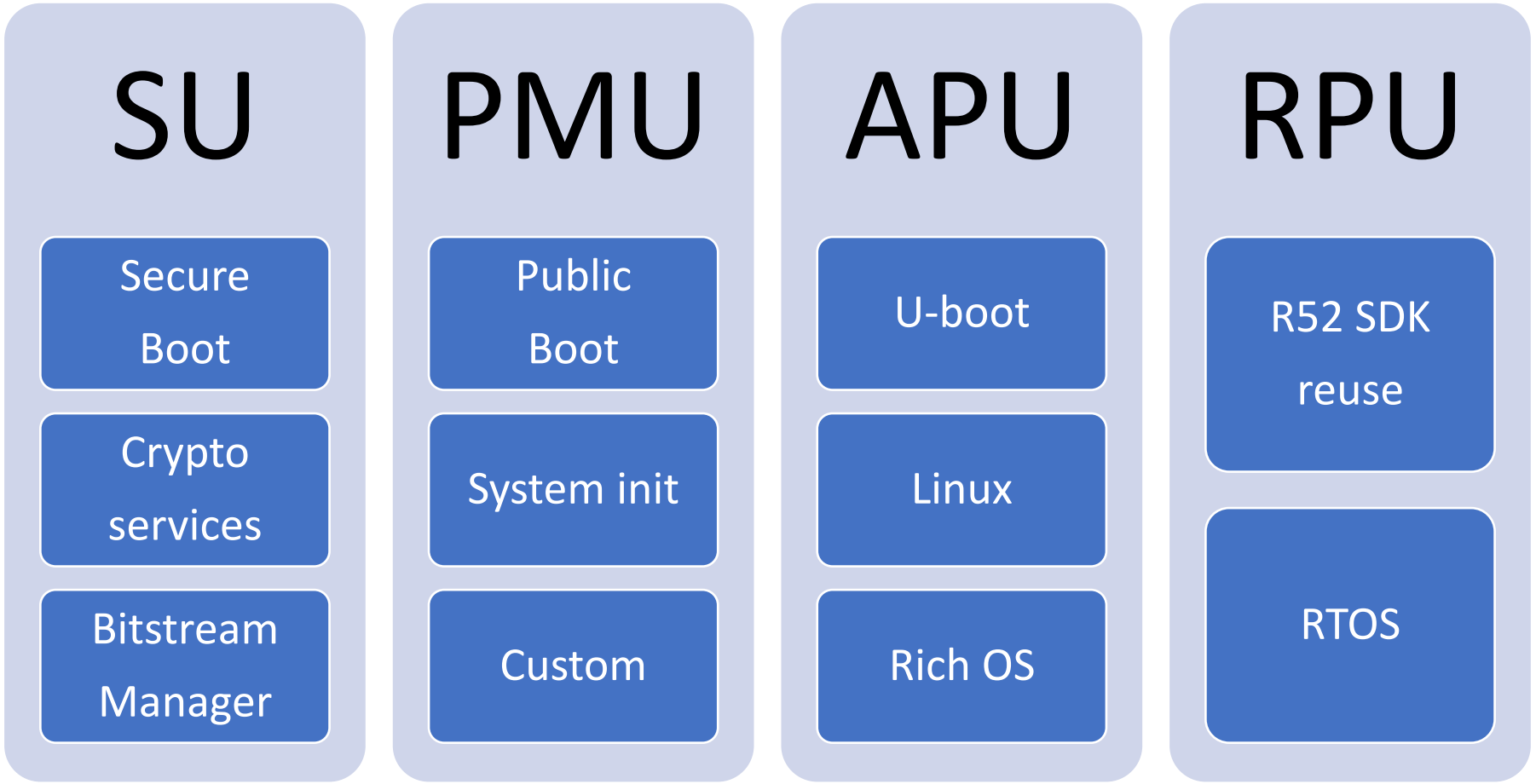
- HW/SW integration
- BOOTROM validation
- Functional tests

Waveform

JTAG

UART

Embedded Software Ecosystem



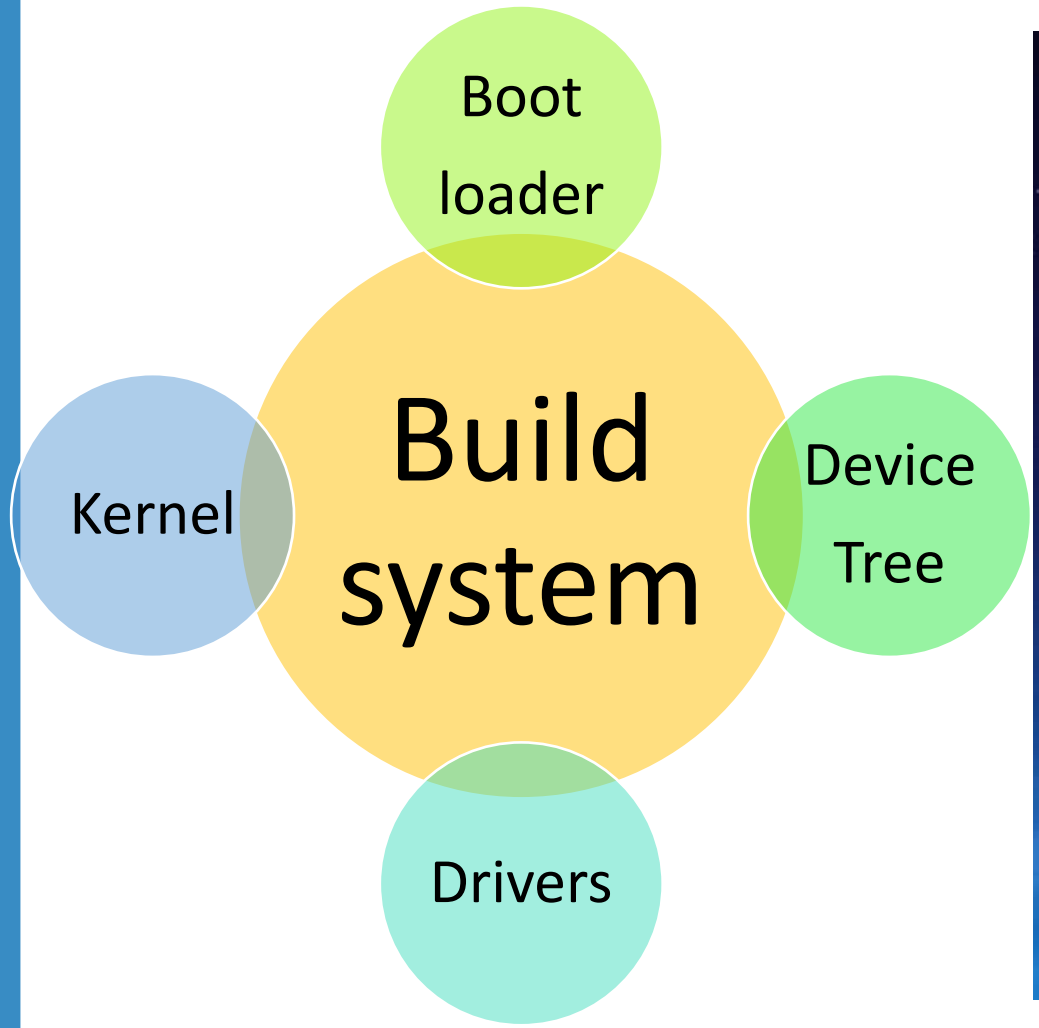
NanoXplore

Linux application use cases

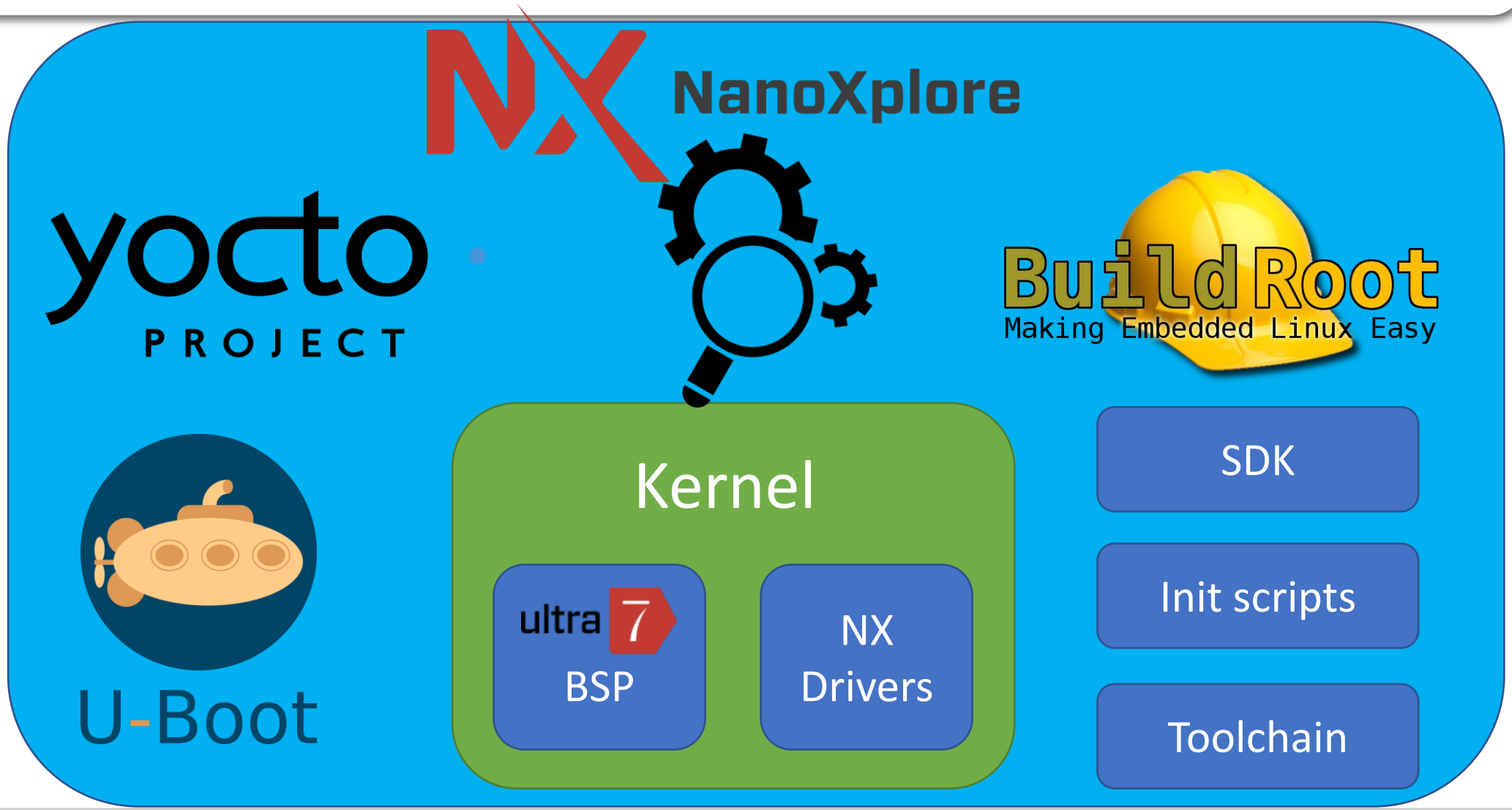
- Can be run natively and independently on Cortex-A
- Can be run natively but monitored by RTOS
- Can be run as guest on top of an hypervisor
- Inter processor communication ensured

Linux is ready to flight

Ready to use software



Linux software ecosystem



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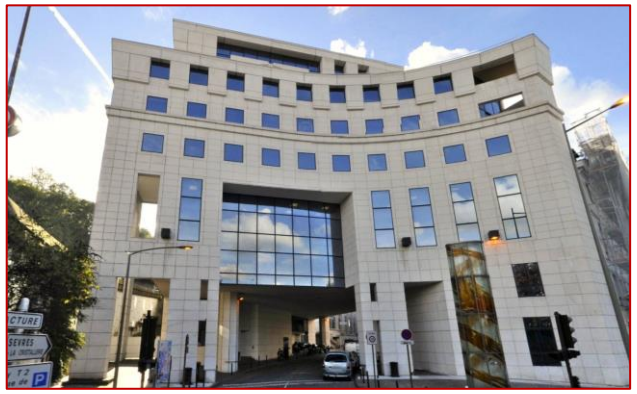

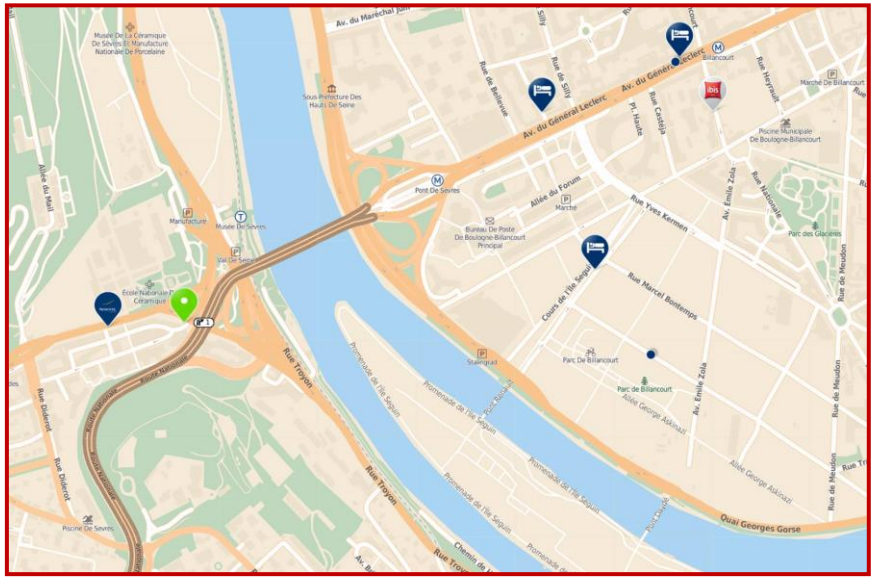

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