NASA's Vision for Spaceflight Computing

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Space Technology Mission Directorate (STMD) Strategic Thrusts

Go

Rapid, Safe, & Efficient Space Transportation

- Develop nuclear technologies enabling fast in-space transits.
- Develop cryogenic storage, transport, and fluid management technologies for surface and in-space applications.
- Develop advanced propulsion technologies that enable future science/exploration missions.

Land

Expanded Access to Diverse Surface Destinations

- Enable Lunar/Mars global access with ~20t payloads to support human missions.
- Enable science missions entering/transiting planetary atmospheres and landing on planetary bodies.
- Develop technologies to land payloads within 50 meters accuracy and avoid landing hazards.

Live

Sustainable Living and Working Farther from Earth

- Develop exploration technologies and enable a vibrant space economy with supporting utilities and commodities
  - Sustainable power sources and other surface utilities to enable continuous lunar and Mars surface operations.
  - Scalable ISRU production/utilization capabilities including sustainable commodities on the lunar & Mars surface.
  - Technologies that enable surviving the extreme lunar and Mars environments.
  - Autonomous excavation, construction & outfitting capabilities targeting landing pads/structures/habitable buildings utilizing in situ resources.
- Enable long duration human exploration missions with Advanced Life Support & Human Performance technologies.

Explore

Transformative Missions and Discoveries

- Develop next generation high performance computing, communications, and navigation.
- Develop advanced robotics and spacecraft autonomy technologies to enable and augment science/exploration missions.
- Develop technologies supporting emerging space industries including: Satellite Servicing & Assembly, In Space/Surface Manufacturing, and Small Spacecraft technologies.
- Develop vehicle platform technologies supporting new discoveries.

Advanced Avionics within NASA Space Technology Mission Directorate (STMD)

EXPLORE: Develop next generation high performance computing, communications, and navigation

Developing flight computing architectures and advanced avionics to enable increased onboard intelligence and autonomy future exploration missions in harsh environments

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Entry Descent & Landing (EDL)
Computing for Real-Time Precision Landing Algorithms (TX 9.0)

In Situ Resource Utilization (ISRU)
Computing for Autonomous Robotic Systems (TX 7.2.3)

Environmental Control and Life Support System (ECLSS)
Computing for Autonomous Clinical Care (TX 6.3.1)

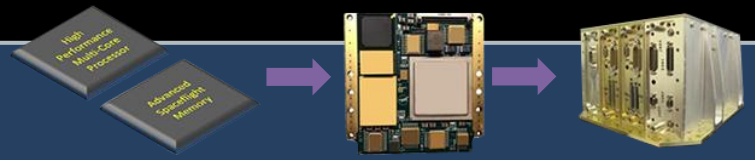
Avionics
TX 2.1 Avionics Component Technologies
TX 2.2 Avionics Systems and Subsystems
TX 11.1 Software Development, Engineering, and Integrity

Autonomous Systems & Robotics
Computing for State Estimation, Terrain Mapping and Classification, 3D Modeling, Object Recognition, Path Planning, Fault Prognosis, Anomaly Detection, Resource Planning and Scheduling, Autonomous Navigation/Obstacle Avoidance, Autonomous Management of In Situ Activities (TX 4.0)

Rendezvous & Capture
Computing for Rendezvous and Docking Algorithms (TX 4.5)

Sensors and Instruments
Computing for Instrument Control and Science Data Processing (TX 8.1, TX 8.3)

Advanced Avionics – Envisioned Future



HIGH PERFORMANCE SPACEFLIGHT COMPUTING

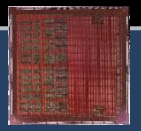
- Radiation-hardened general-purpose processor with increased performance and flexibility to adapt to mission specific performance, power, and fault tolerance needs
- Advanced spaceflight memory with radiation tolerance and increased capacity and performance
- Intelligent, efficient, multiple output Point-Of-Load (POL) power converters
- High performance Single Board Computer (SBC) incorporating high-performance general-purpose processors, advanced memory, point-of-load converters, and real-time operating system in industry standard form factors and bus architectures
- System software tools to leverage the capabilities and manage the complexity of advanced multi-core processors

INTERCONNECT

- Radiation-tolerant interconnects to support low latency onboard video, multi-gigabit instruments, onboard science, and enhanced autonomy applications; including end points, switches, physical layer devices, and software support
- Highly reliable, high-bandwidth deterministic wireless networks

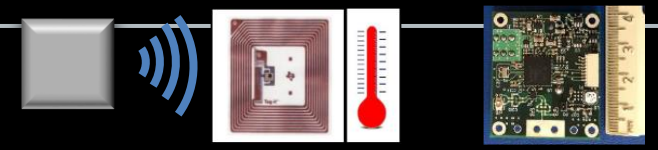
CREW INTERFACES

- Radiation-tolerant displays that can operate reliably for long durations mission beyond LEO
- Radiation-tolerant graphics processing that can operate reliably for long mission durations beyond LEO
- Heads Up Displays for Exploration EVA
- Crew voice and audio systems for deep space missions providing efficient compression of multiple streams, acoustic echo and noise cancellation, speech recognition and voice control, and wireless capabilities



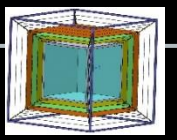
OTHER COMPUTING ARCHITECTURES

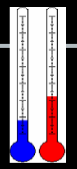
- Artificial Intelligence (AI) coprocessors to enable autonomous landing, surface navigation, robotic servicing/assembly, fault detection/mitigation, distributed systems operations, science data processing, and tip and cue for remote sensing missions
- Spaceflight quantum computers
- Low power embedded computers to support distributed robotics architectures



DATA ACQUISITION

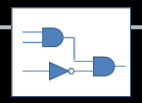
- Wireless sensor networks to reduce harness mass and complexity, simplify integration and test, and improve system flexibility, serviceability, and expandability
- Low-cost, robust, high-accuracy data acquisition systems to enable distributed in situ monitoring of structures and subsystems on cost constrained missions

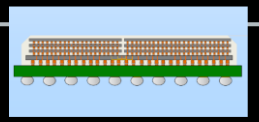




EXTREME ENVIRONMENT AVIONICS

- Extreme temperature electronics capable of operating in environments with both high radiation and wide temperature ranges, including lunar/planetary surfaces and nuclear systems
- Avionics packaging and thermal management technologies to enable avionics operation in extreme environments



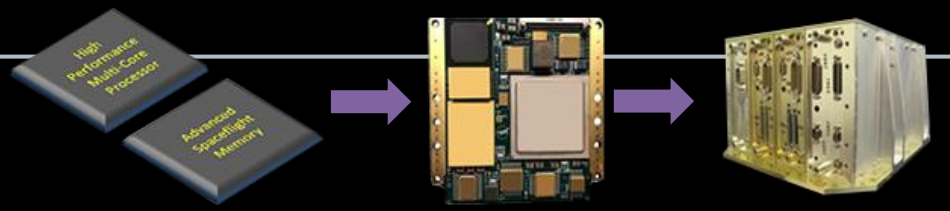


FOUNDATIONAL TECHNOLOGIES

- Advanced 2.5D/3D packaging and heterogeneous integration enabling miniaturization and improved performance
- Advanced semiconductor process nodes and libraries to enable next generation radiation hard devices
- Low-cost, radiation-hardened mixed-signal ASICs

All activities depicted not currently funded or approved. Depicts "notional future" to guide technology vision.

Advanced Avionics – Envisioned Future



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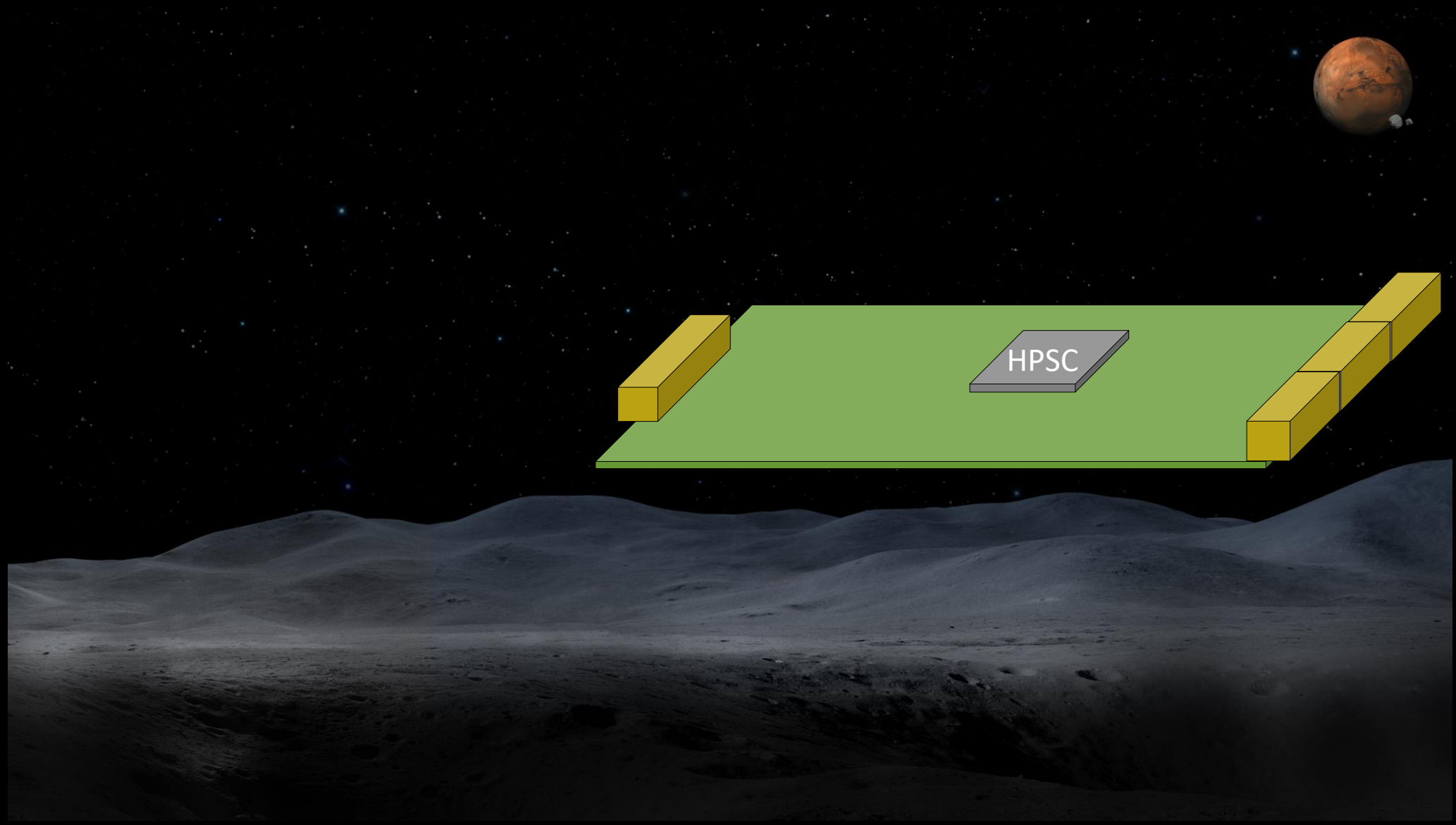
Computing Technologies – System Context



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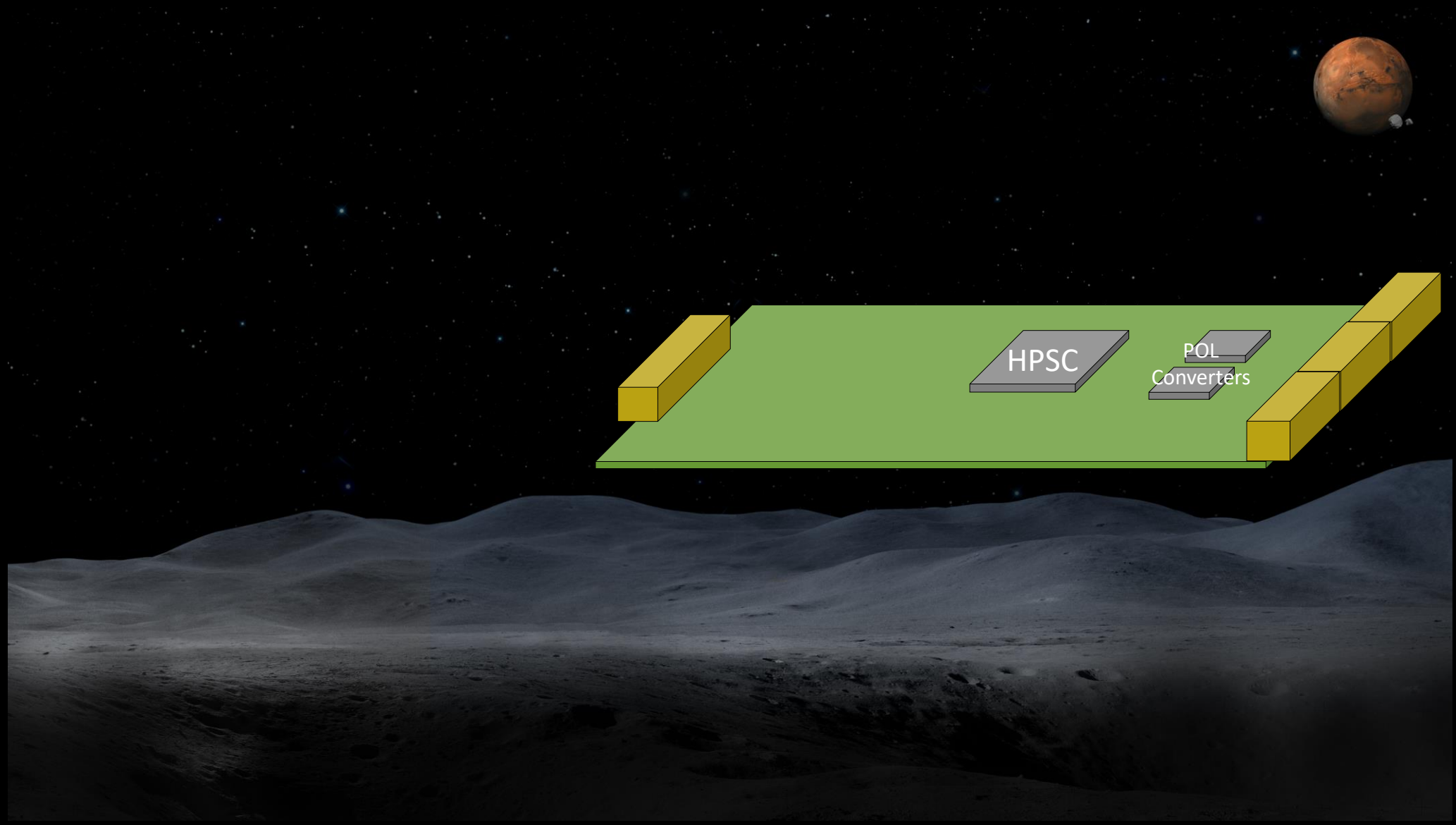

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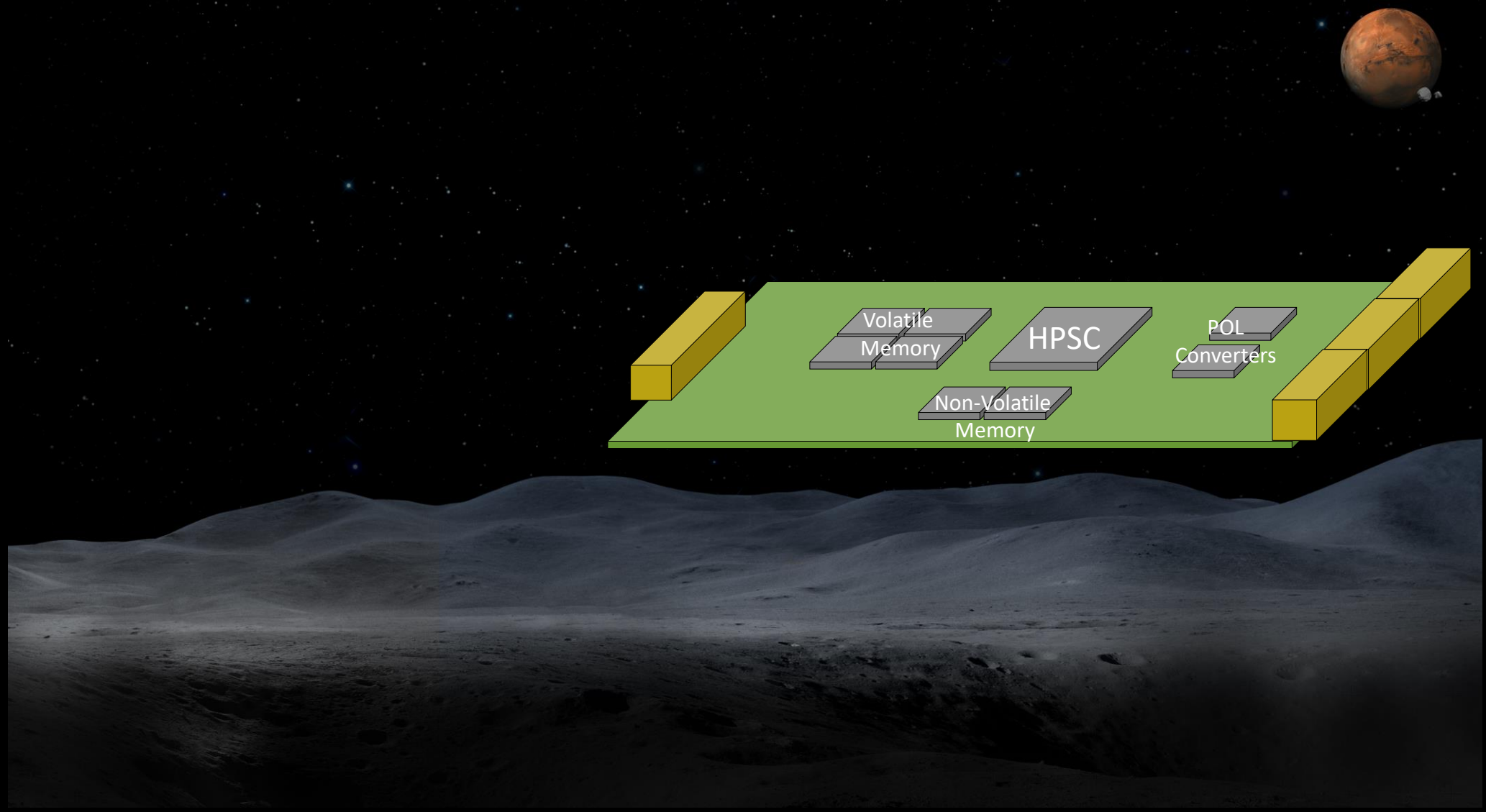

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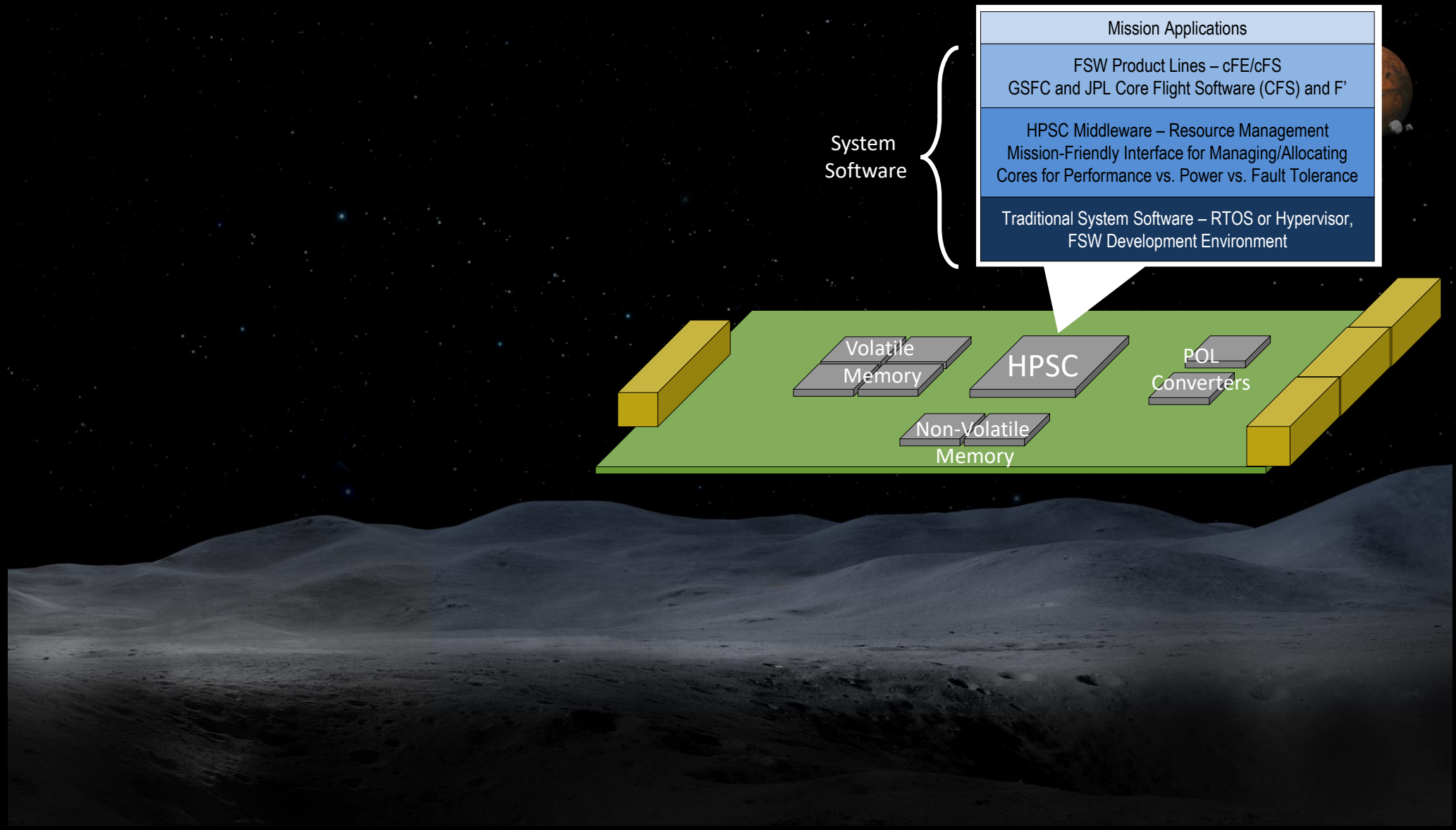

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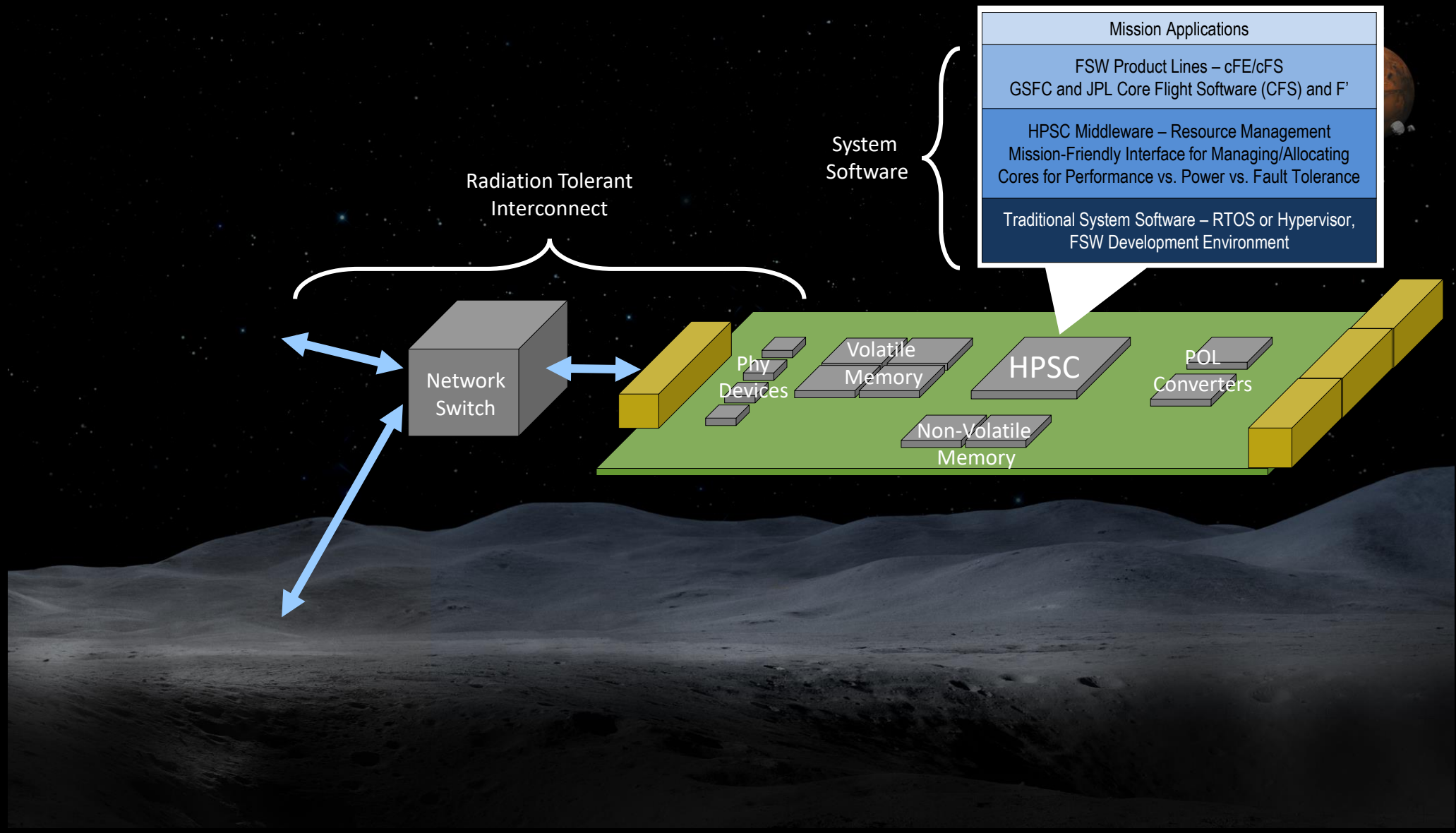

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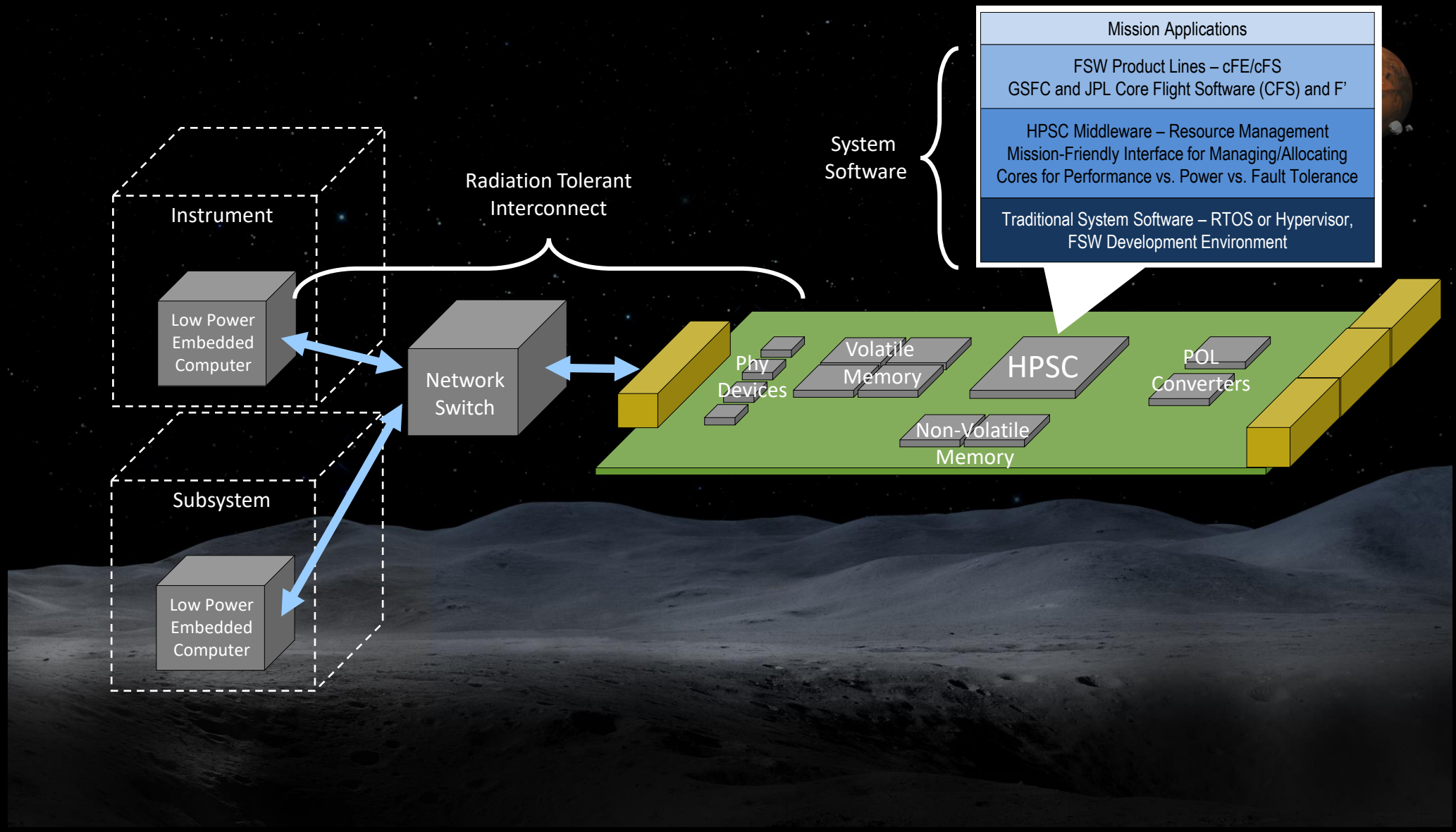

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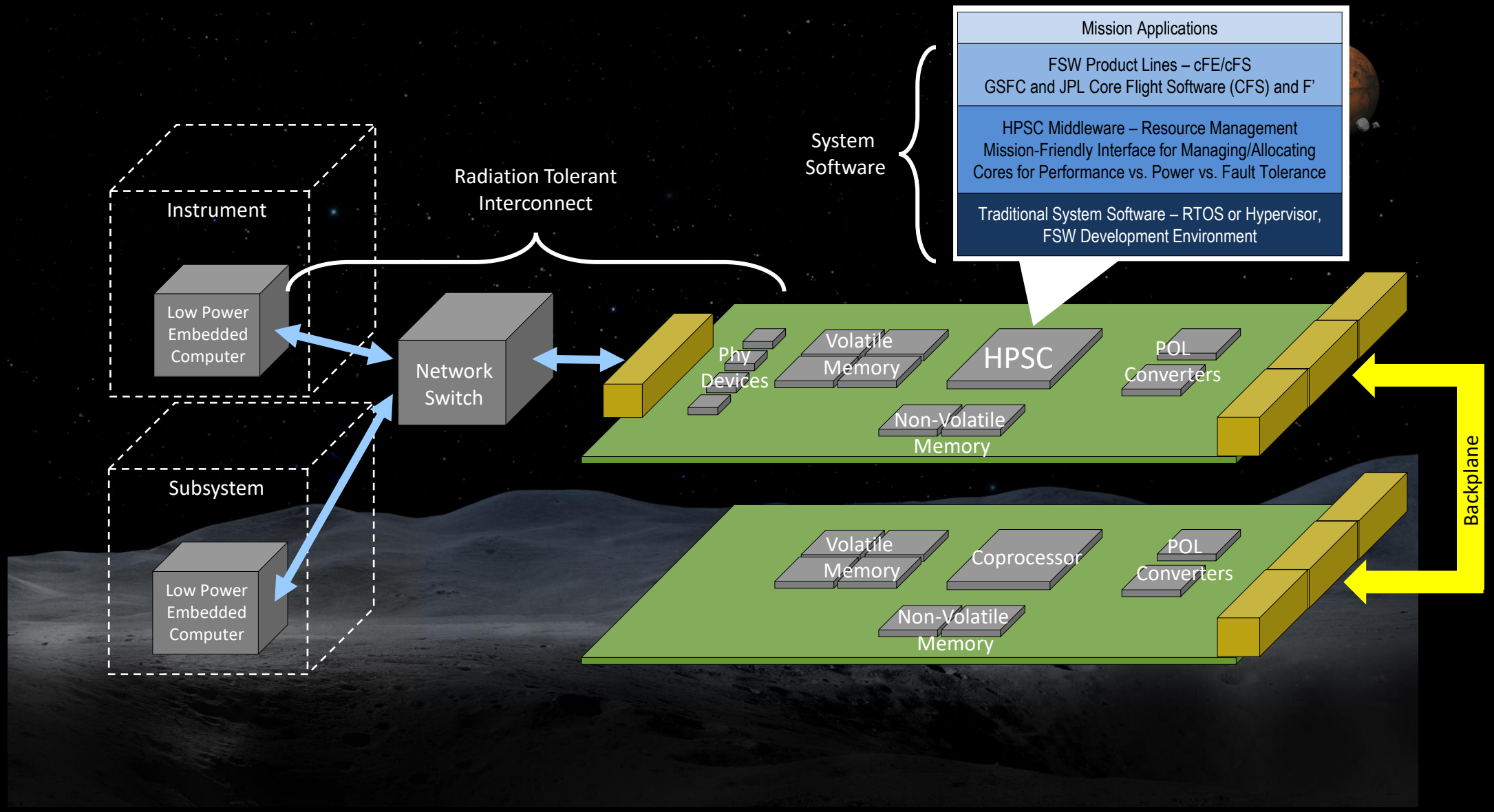
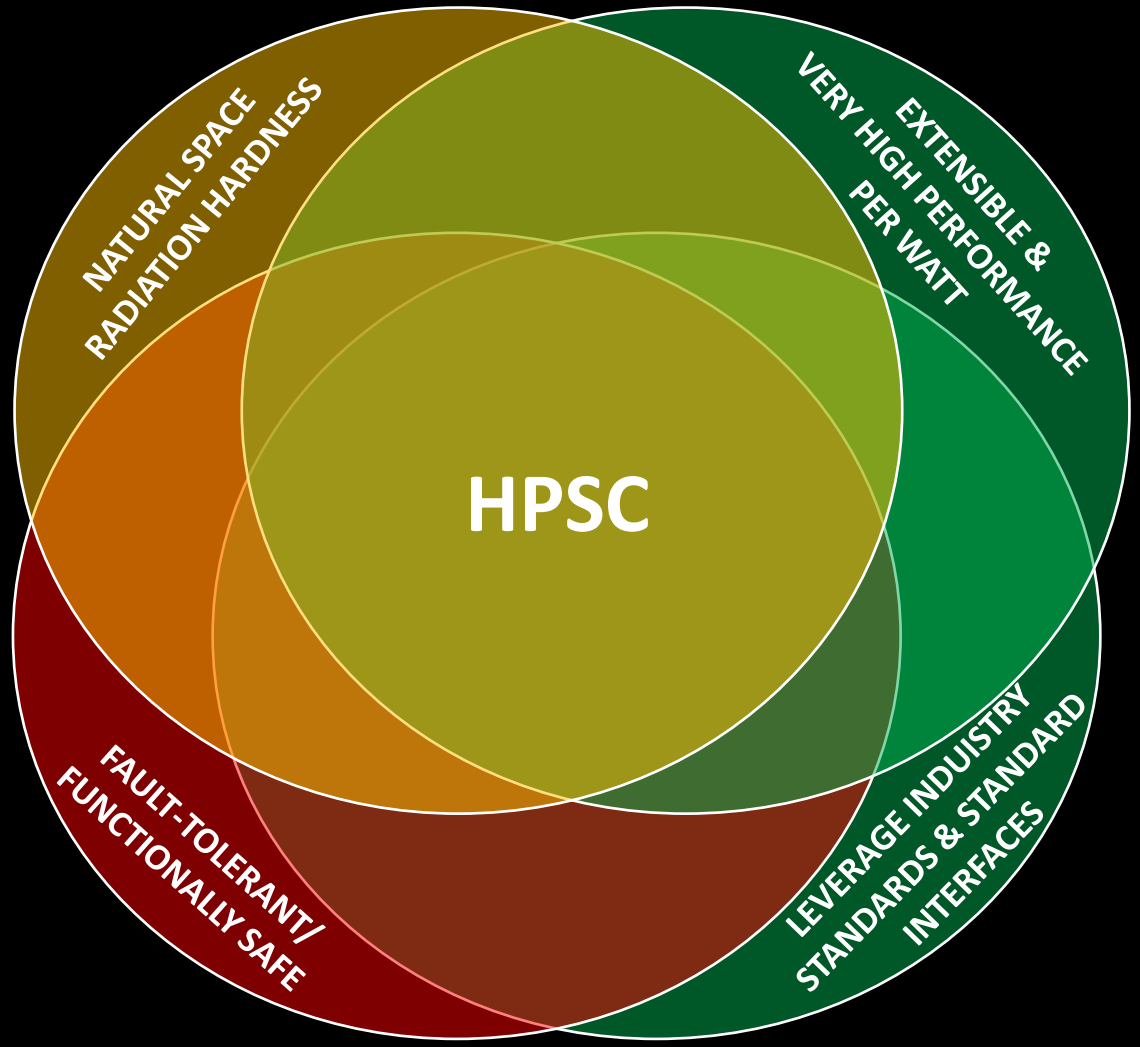


High Performance Spaceflight Computing (HPSC) Prime Directive

Deliver modern disruptive and extensible performance, performance per watt, and fault-tolerance to enable NASA & JPL to support the ever-increasing levels of mission autonomy and complexity while simultaneously reducing development cost, risk, and time



HPSC Overview

Following an HPSC concept study phase, Microchip was selected to develop the HPSC – including processors, evaluation boards, and system software

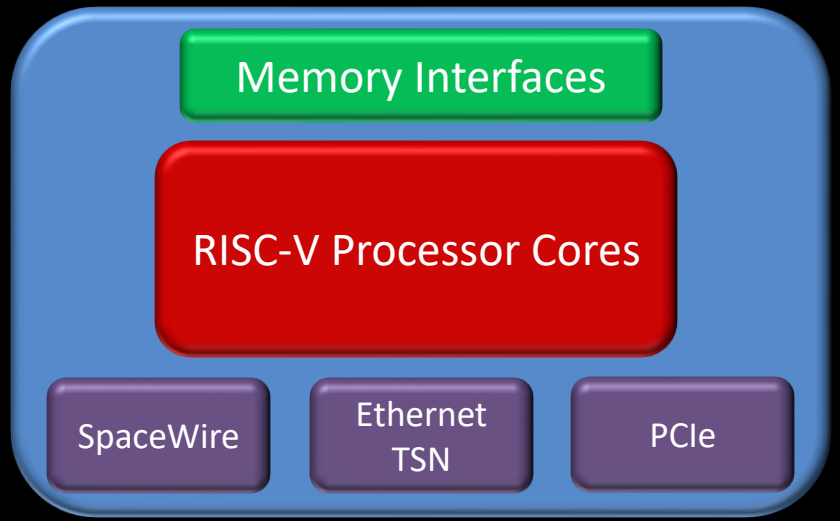
- $50 million firm-fixed-price contract was awarded
- Microchip is contributing significant research and development costs to complete the project
- Estimate prototype SoCs and evaluation boards available in 2024 and space qualified SoCs in 2025
- Target to have QML-Y qualified parts

Key HPSC features

- Based on the RISC-V ISA
- Achieves 100X scalar processing performance improvement over the existing RAD750 processor
- Provides vector processing and machine learning acceleration capabilities that are unavailable from current spaceflight processors
- Provides a wide envelop for power/performance/fault tolerance scaling

Interfaces supported

- Ethernet with Time Sensitive Networking (TSN)
- PCIe
- SpaceWire



HPSC Processor

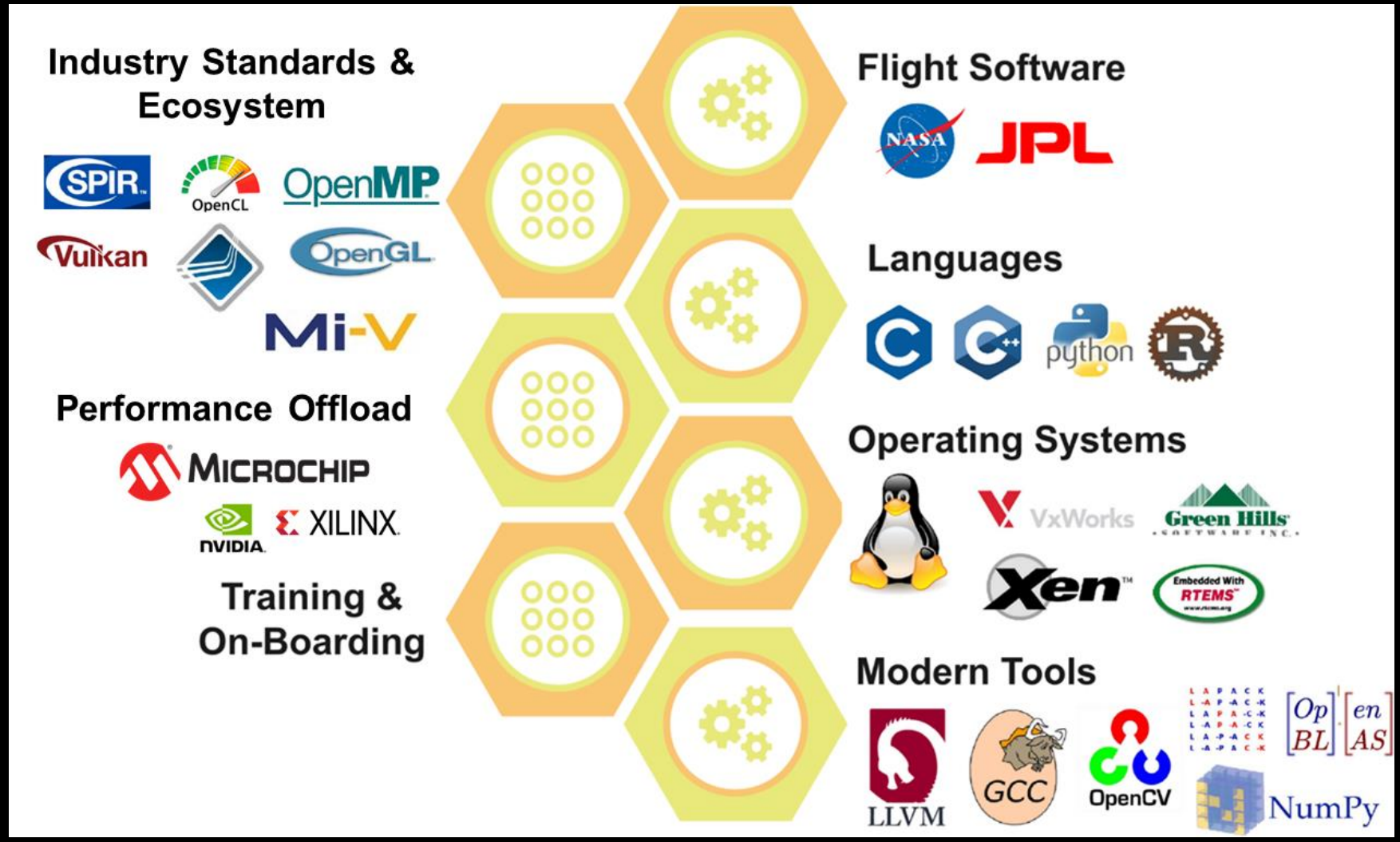
HPSC Software Ecosystem

Modern tools and leading-edge industry standards allows targeting of arbitrary compute devices

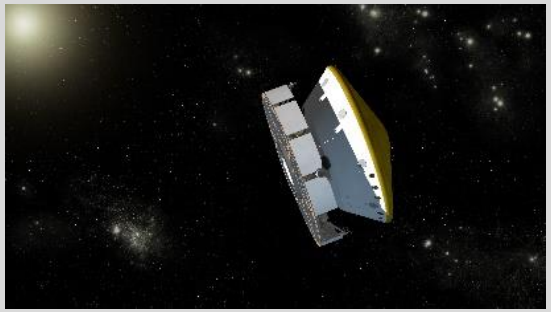
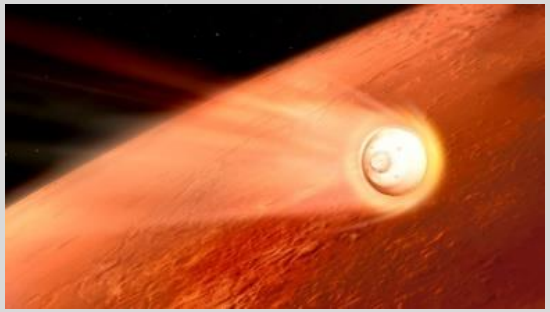
Enables extensible and reusable development efforts

Takes advantage of commercial and open-source efforts

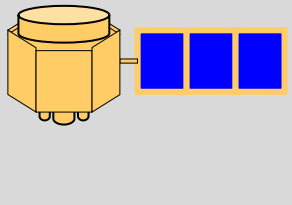
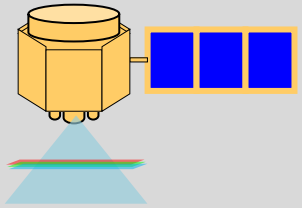
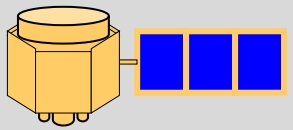
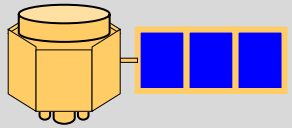
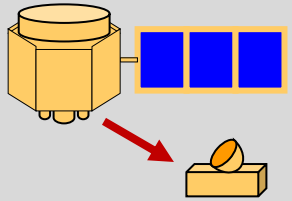
Standardized training and support



Power/Performance Scaling Use Cases

Planetary Use Case		
Cruise Phase	Entry Descent and Landing (EDL)	Science Operations
		
• Low processing bandwidth for housekeeping functions • Low power dissipation	• High processing bandwidth with image processing tasks in tight control loops • Robust fault tolerance • High power dissipation	• Varying processing bandwidth • Varying fault tolerance (mobility operations vs. science data processing) • Varying power dissipation

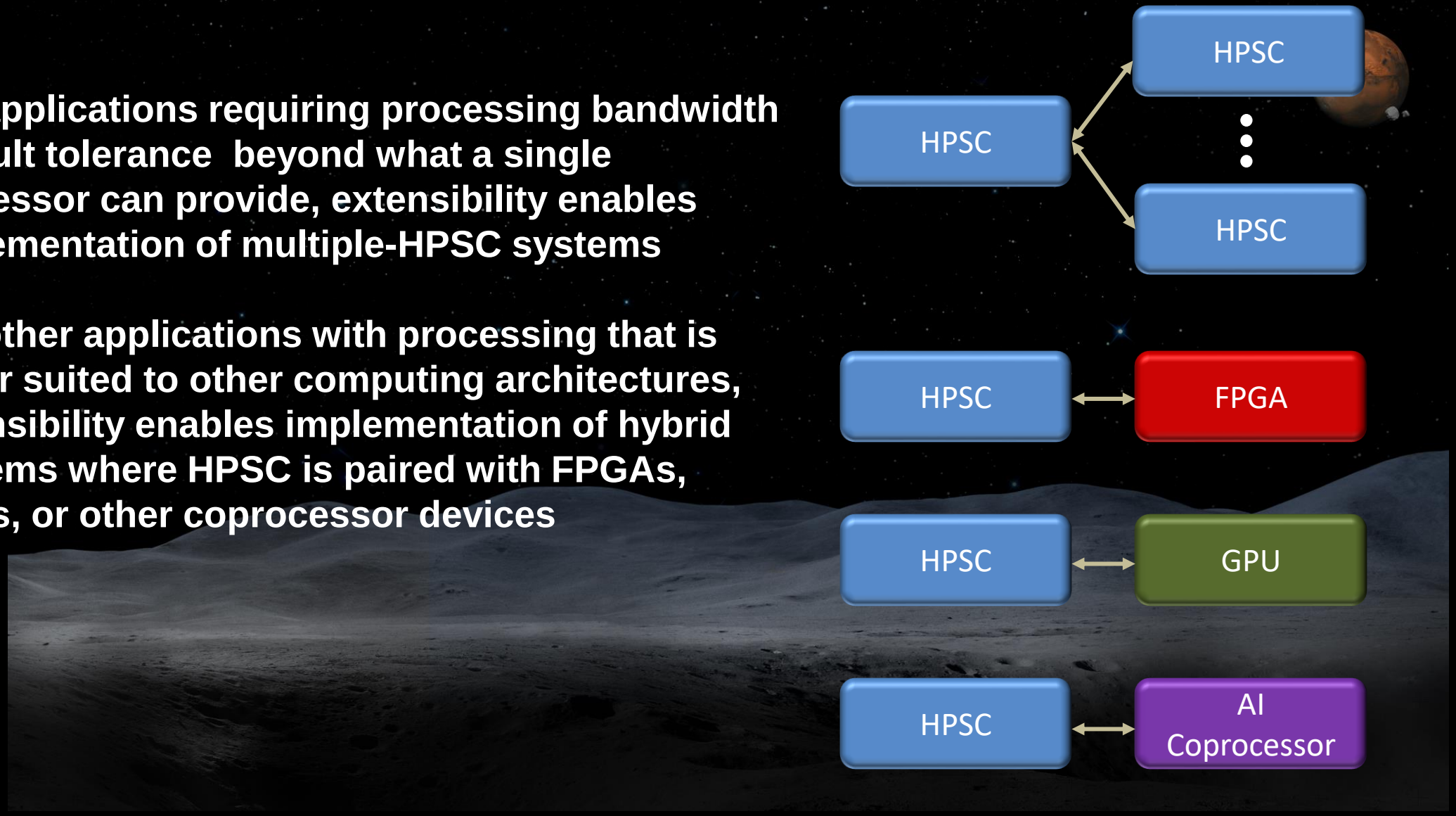
Power/Performance Scaling Use Cases

Earth Observing SmallSat Use Case				
Quiescent	Data Acquisition (Tasked via ground command or triggered from Ground or Sensor Web)	Onboard Processing for Data Reduction	Quiescent	Downlink
				
• Low processing bandwidth for housekeeping functions • Low power dissipation	• Moderate processing to manage data acquisition • Moderate power dissipation	• High processing bandwidth High power dissipation	• Low processing bandwidth for housekeeping functions • Low power dissipation	• Moderate processing to manage data acquisition • Moderate power dissipation

Extensibility

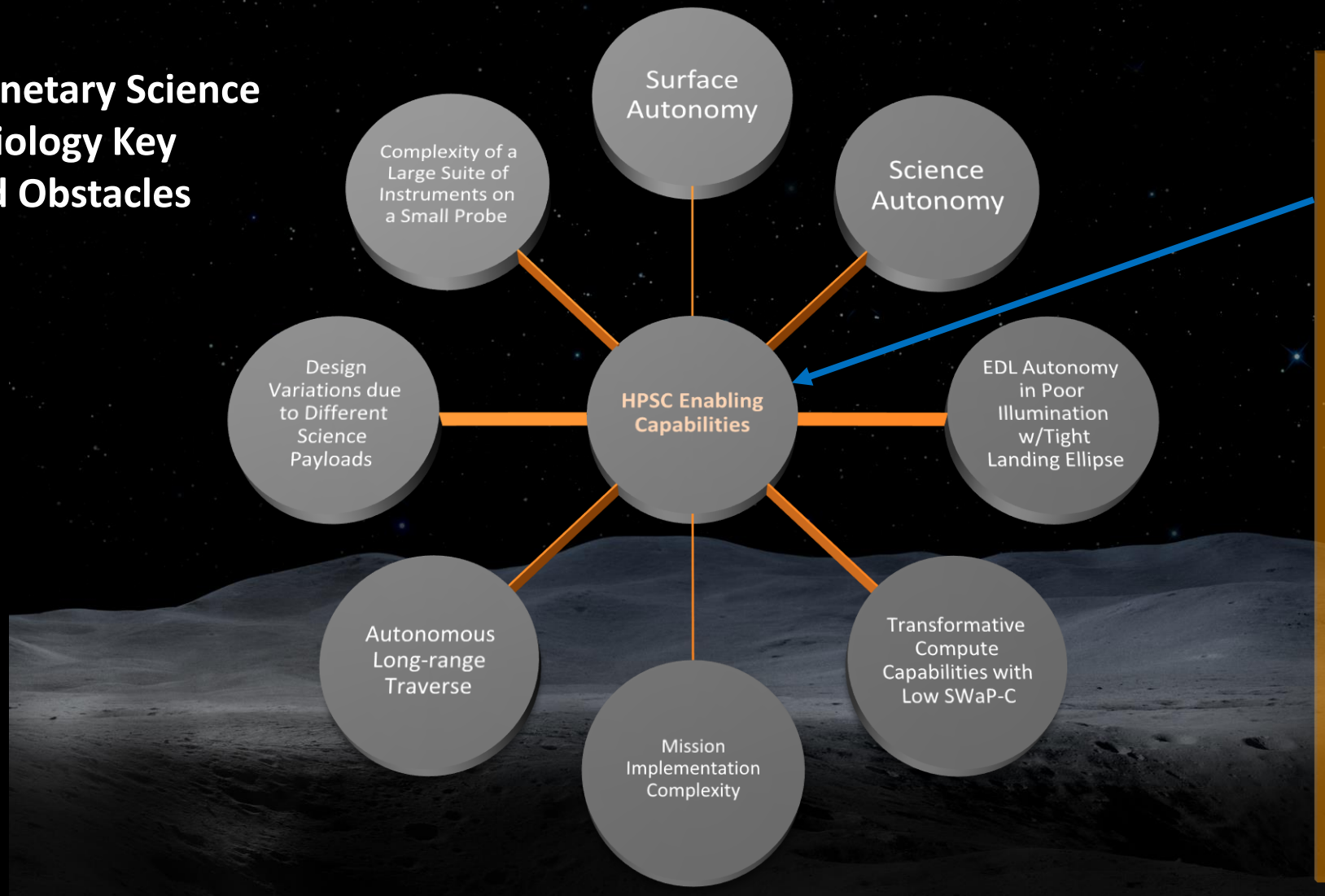
For applications requiring processing bandwidth or fault tolerance beyond what a single processor can provide, extensibility enables implementation of multiple-HPSC systems

For other applications with processing that is better suited to other computing architectures, extensibility enables implementation of hybrid systems where HPSC is paired with FPGAs, GPUs, or other coprocessor devices



Mission Drivers for High Performance Spaceflight Computing - Planetary

NASA Planetary Science & Astrobiology Key Identified Obstacles



HPSC Enabling Capabilities

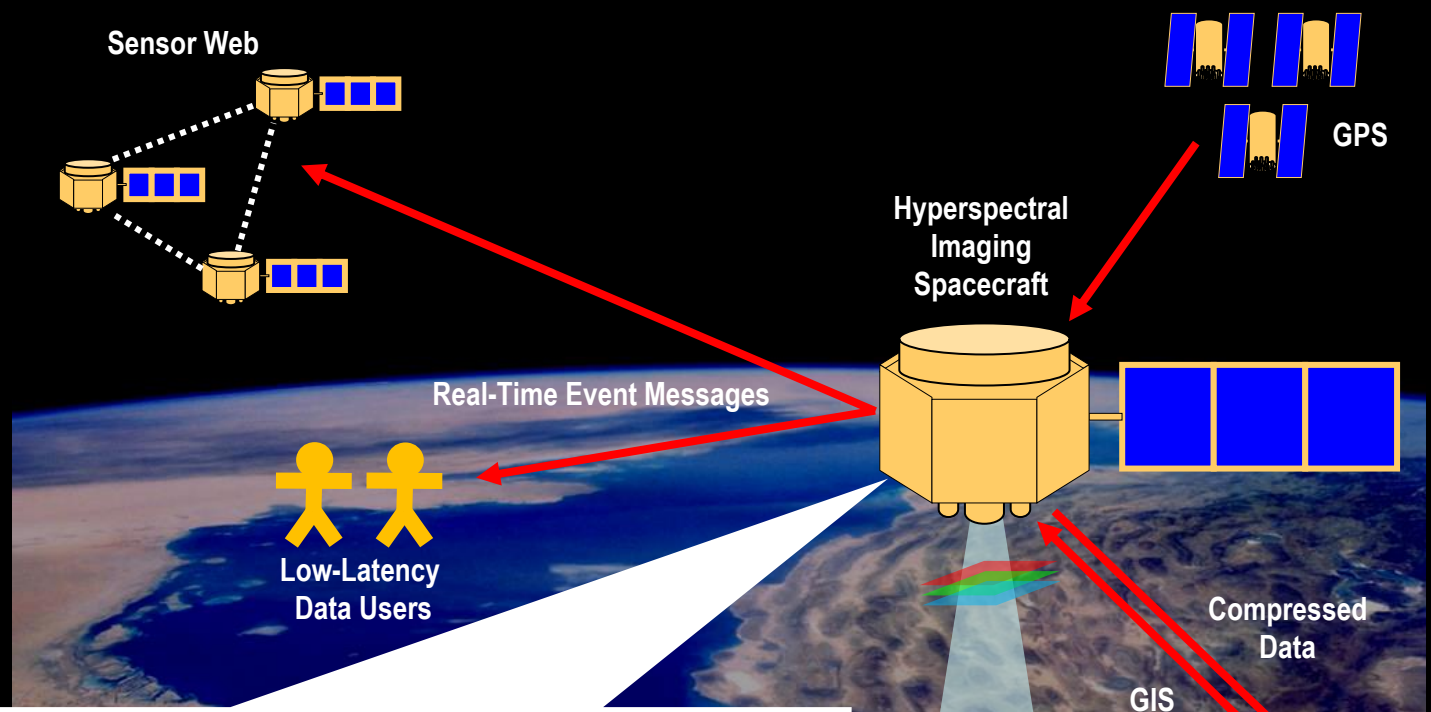
- 100x (or more) performance gain over current space compute with same power.
- Very high performance per SWaP-C.
- Dynamically scalable power & performance.
- Fault-tolerance and radiation tolerance.
- Extensible performance & power enabling mission customization.
- Reduced development time & cost.
- Ease of implementation variations (support of SW defined capabilities).

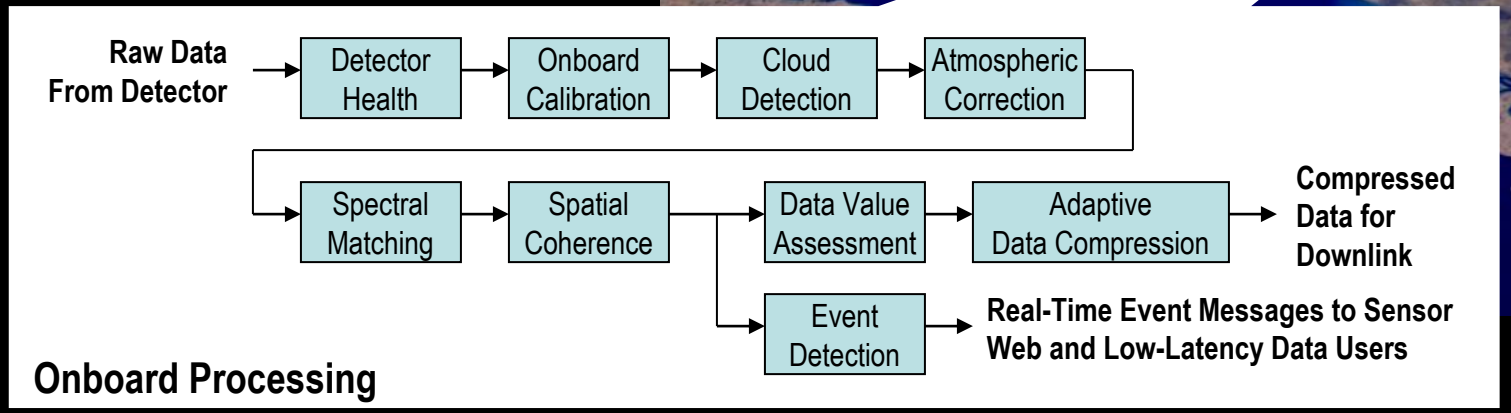
HPSC Addresses a Significant Number of Key Identified Mission Obstacles

Mission Drivers for High Performance Spaceflight Computing – Earth Science

Hyperspectral Earth Imaging Mission

- HPSC provides the processing bandwidth necessary to ingest and process hyperspectral sensor data, and perform onboard event detection and data reduction
- HPSC vector processing capabilities should allow processing to migrate from FPGAs into the processor, thereby simplifying application development

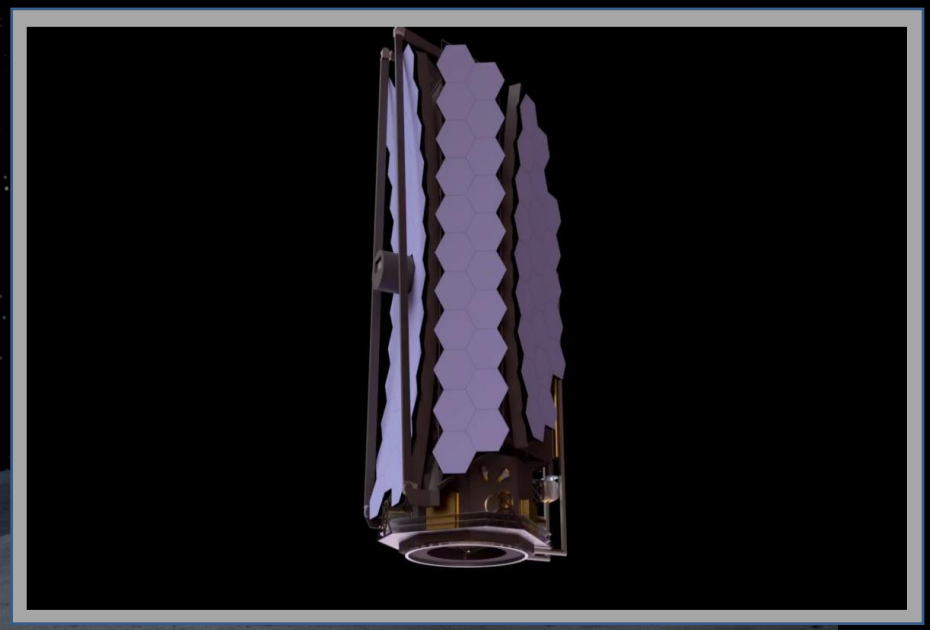




Mission Drivers for High Performance Spaceflight Computing – Astrophysics

Large UV/Optical/IR (LUVOIR) Telescope

- HPSC processing bandwidth enables high contrast imaging for starlight nulling
- HPSC is being considered [M. Bolcar, NASA GSFC, IEEE SCC 2021] for the primary CPU for the system (execution of all algorithms, controlling deformable mirrors, execution of all control loops)
- Separate array of FPGA's with 20GB of memory for the inversion of very large matrices and execution of FFTs for the control algorithms



Leveraging HPSC vector processing could reduce the number of FPGAs used in LUVOIR, which would improve SWaP-C efficiency and simplify algorithm implementation

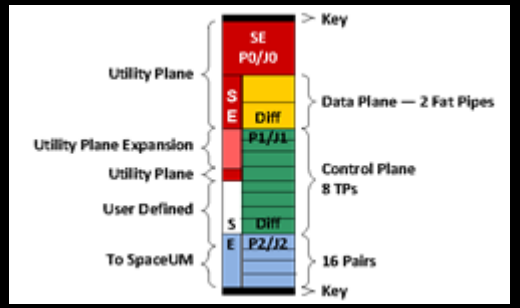
NASA and SpaceVPX

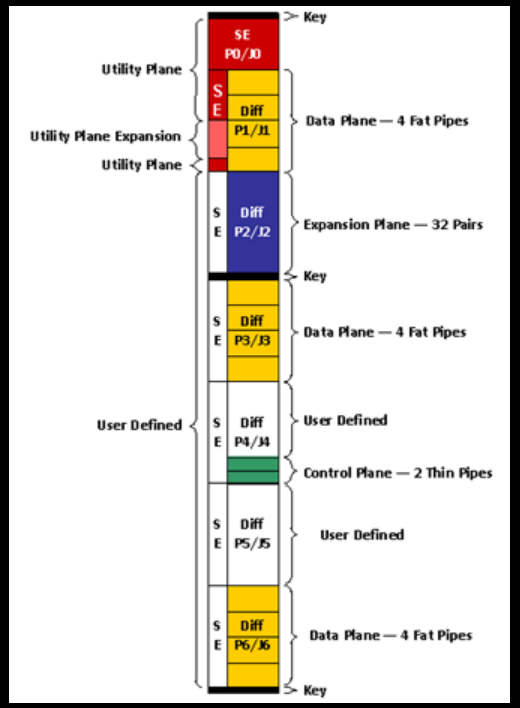
As NASA exploration moves beyond low-Earth-orbit (LEO), the need for interoperable avionics systems becomes more important due to the cost, complexity, and the need to maintain distant systems for long periods

The existing SpaceVPX industry standard addresses some of the needs of the space avionics community, but falls short of an interoperability standard that would enable reuse and common sparing on long duration missions and reduce NRE for missions in general

A NASA Engineering & Safety Center (NESC) study was conducted to address the deficiencies in the SpaceVPX standard for NASA missions and define the recommended use of the SpaceVPX standard within NASA

The future infusion of HPSC into SpaceVPX systems was a consideration in this study





3U and 6U Slot Profiles [VITA-78]

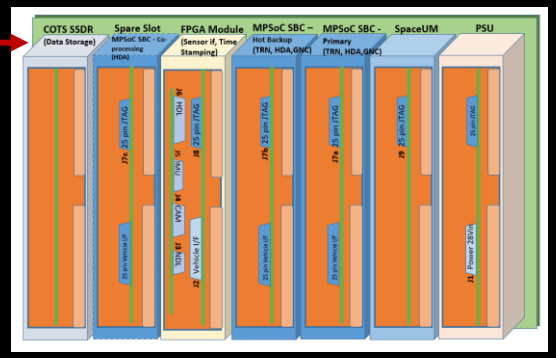
SpaceVPX Overview

SpaceVPX is an architecture standard that defines modules, backplanes, and chassis for spaceflight avionics boxes (the SpaceVPX standard is managed by VMEbus International Trade Association (VITA) as VITA-78)

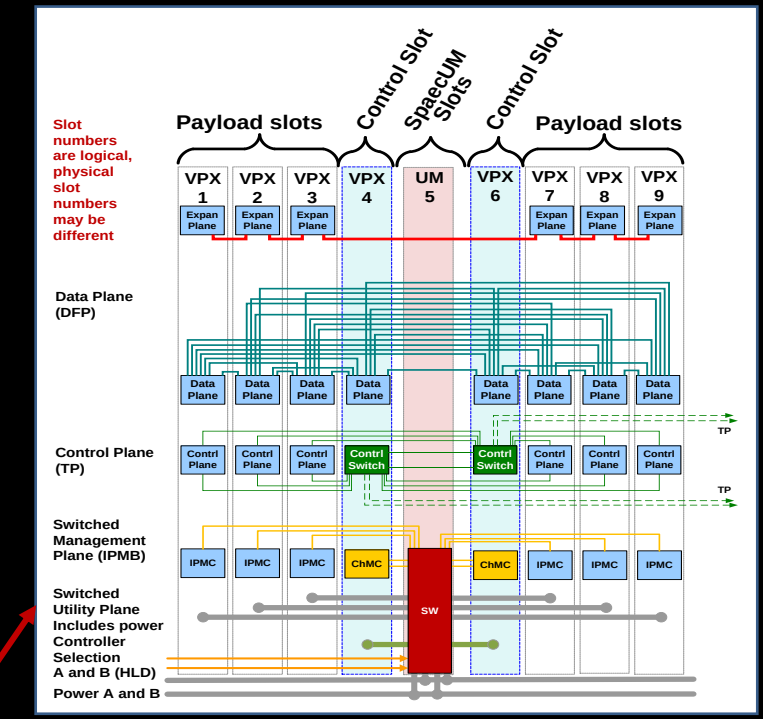
SpaceVPX adapts a Modular Open System Approach (MOSA), derived from VPX and OpenVPX (VITA-65), for space

SpaceVPX defines several general module types and how they can be interconnected, using the concept of "profiles"

- Slot Profile – A physical mapping of ports onto a slot's backplane connectors
- Module Profile - Extends a slot profile by mapping protocols to a module's ports and defines physical dimensions
- Backplane Profile - Defines number and types of modules supported and their interconnection topology



Profile Name	Data Plane 4 FP	Expansion Plane P2/J2	Control Plane 2 TP	User Defined
	DP01 to DP04		CPtp01 to CPtp02	P3/J3, P5/J5
MOD6-PAY-4F1Q2T-12.2.1-1-cc	sRIO 2.2 at 3.125 Gbaud per Section 5.2	sRIO 2.1 at 3.125 Gbaud per Section 5.2	SpaceWire per Section 5.2.1	User Defined DIFF pins



[VITA-78]

Over 40 specific slot "profiles" define the backplane signal interconnection for different variants of these module types

To be presented remotely at the 2022 Avionics, Data, Control and Software Systems Workshop (ADCSS'22), Noordwijk, Netherlands, October 25-27, 2022.

SpaceVPX Challenges

It is possible to implement two different modules that are fully compliant with SpaceVPX yet cannot interoperate

- Modules with different form factor and depth complicate chassis implementation
- Even modules with identical slot profiles will not talk to each other if one uses SpaceWire and the other SRIO for datal plane network protocols

The immense flexibility of SpaceVPX can limit interoperability

- The standard defines modules with widely varying physical dimensions
  - Form factor (3U and 6U)
  - 4 options for module length
- **There are 48 separate slot profiles defined (not including variations in length and pitch)**
- SpaceVPX does not specify a single network protocols for the control and data planes
  - Possible options include SpaceWire, SpaceFibre, Serial RapidIO (SRIO), Ethernet
- User defined signals

Interoperability guidelines are needed to constrain the configuration, design choices and usage of SpaceVPX, enabling systems that can be composed of modules from different developers

- Ensure that NASA developed modules can be used across multiple missions and applications
- Allow industry to develop SpaceVPX modules that meet NASA mission needs

Other aspects of the SpaceVPX standard present challenges for NASA

- Required redundancy in several areas limits the development of single string systems
- Limits types of fault tolerance architectures and implementations (natively only supports dual redundancy, and does not map directly to other system level fault tolerance patterns)

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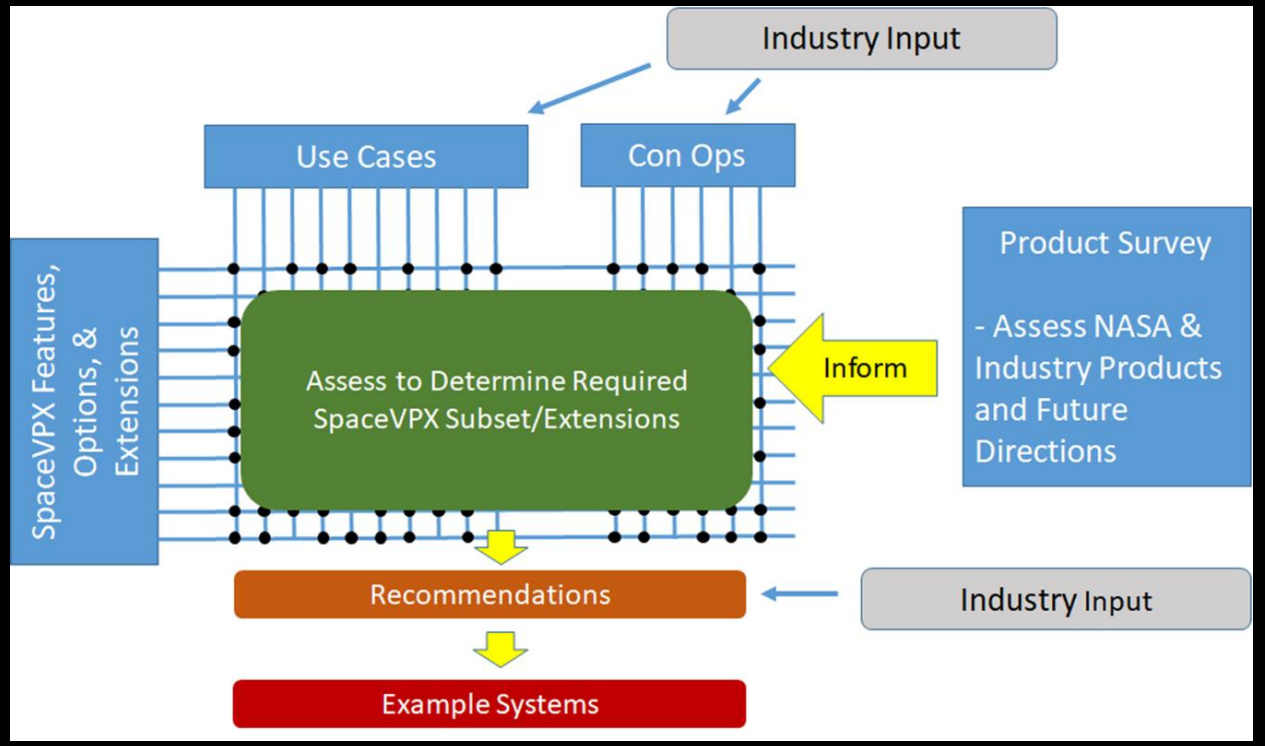
NASA SpaceVPX Study Approach

The effort was divided into the following tasks:

- Notional use case analysis
- Product surveys
- Study focus area analysis
  - Interconnect
  - Power management and distribution
  - Form factor and daughtercards
  - Fault tolerance
- Engagement with other organizations
- Definition of proposed NASA SpaceVPX specification
- Identification of candidate modules
- Definition of example SpaceVPX systems



Study Approach

Use Case Analysis

Notional use case analysis provided an understanding of the breadth of implementations that SpaceVPX must accommodate and the features, capabilities, and interfaces that are needed to implement a broad range of NASA avionics systems

The following was assessed for each of the12 use cases

- Orbit / Destination
- Mission Criticality
- SWaP Sensitivity
- Block Diagrams
- Required Interfaces
- Timing and Deterministic Constraints
- Power Architecture
- Redundancy and Fault Management

Notional Use Case	Brief Description
Crewed Mission Avionics (*)	Implementation of Vehicle Control Unit (VCU) and Time Triggered Ethernet (TTE) switch
Crewed Mission Robotics and Surface Vehicle	Implementation of 'Robonaut type' avionics and lunar rover avionics
SmallSat	Combined C&DH and instrument processing in single chassis for an Evolved Secondary Payload Adapter (ESPA) -class mission
On-orbit Servicing, Assembly, and Manufacturing (OSAM)	Implementation of avionics for onboard servicing, assembly, and manufacturing robotics
Science Rover	Robotic science rover avionics
Precision Landing Processor	Implementation of the SPLICE DLC
High Data Rate Missions (3)	High bandwidth Synthetic Aperture Radar (SAR)
	Spectroscopy (based on EMIT mission concept)
	Advanced Earth observing hyperspectral instrument
Low/Medium Data Rate Mission	Generic telescope mission concept with moderate data rates (less than 0.5 Gbps)
Communication Relay Spacecraft	Orbital optical communication relay payload based on Laser Communication Relay Demonstration (LCRD)
HPSC A-Team Use Cases	A hybrid of autonomous planetary mission use cases derived from a JPL HPSC A-Team study

Proposed NASA SpaceVPX Specification

	Proposed NASA Specification
RT-1	**General** Support dual redundant and single string SpaceVPX systems.
RT-2	**Power distribution and management** Utilize the 5-output SpaceUM (SLT3-SUM-5S1V3A1R1M3C-14.7.2) for 3U implementations with a 5V main power voltage. Utilize the 8-output SpaceUM (SLT6-SUM-8S3V3A1B1R1M4C-10.8.1) for 6U implementations with +12, +5, and +3.3 main supply voltages.

RT-3	**Interconnect**
	Support the following interconnect protocols:
	• Data Plane – Support for Ethernet 10GBASE-KR as specified in IEEE 802.3ap with support for TSN as specified in IEEE 802.1AX, CB, AS, Qbv, Qav, Qci, Qcc, and 802.1Q clauses 8.6.5.1 and 8.6.8.2
	• Control Plane - SpaceWire as defined in ECSS-E-ST-50-12C
	• Expansion Plane – JESD204C
	• Expansion Plane – Support for PCIe Gen 3.1
	• Utility Plane – IPMI and DAP as specified in VITA-78
	• User Defined signals with the requirement that they are user programmable
	  • SERDES.- 1600mV peak-to-peak AC-coupled differential signaling; 8b/10b encoding; data rates of 1.25 Gbps, 2.5 Gbps, 3.125 Gbps, 5 Gbps, 6.25 Gbps, and 10 Gbps (note that some modules may not support all of these rates)
	  • Single ended - 2.5V LVCMOS signaling
	• Low-Rate Interconnect – I2C
	• JTAG
	• Provide pin on a front panel to disable JTAG for flight.

Proposed NASA SpaceVPX Specification

	Proposed NASA Specification
RT-4	**Form Factors and Daughtercards** Support 3U and 6U – 220mm form factors. Support for XMC and/or FMC daughtercards on SpaceVPX FPGA-based modules. Combined 3U/6U chassis as needed.
RT-5	**Fault tolerance** Adopt fault tolerance methodologies as defined in VITA-78.
RT-6	**Backplanes and Chassis** Use VITA-78 identified passive backplanes.
RT-7	**Connectors** Utilize SpaceVPX module and backplane that comply with VITA-46.
RT-8	**VITA-78 features not be used to ensure future interoperability** • Specified chassis and backplane profiles. • SRIO on data plane (can be implemented with User Defined SERDES). • SpaceFibre on data plane (can be implemented with User Defined SERDES). • System Controller interfacing to 4 SpaceUM modules (recommendation is 2). • Support for heritage cPCI modules. • Support for 2-output 3U SpaceUM (SLT3-SUM-2S3V3A1B1R1M4C-14.7.1). • Support for VBAT voltage. • System management discrete input and output interfaces. • Full latitude on user defined signal usage .

Proposed NASA SpaceVPX Specification

The following features are proposed that are not currently in VITA-78:

- Explicit support for single string systems
- Using Ethernet/TSN for data plane
- Use of PCIe 3.1 for expansion plane
- JESD-204C support for high bandwidth digitizers
- Constraints on user defined signals
- Explicit daughtercard support

Candidate Module Definitions

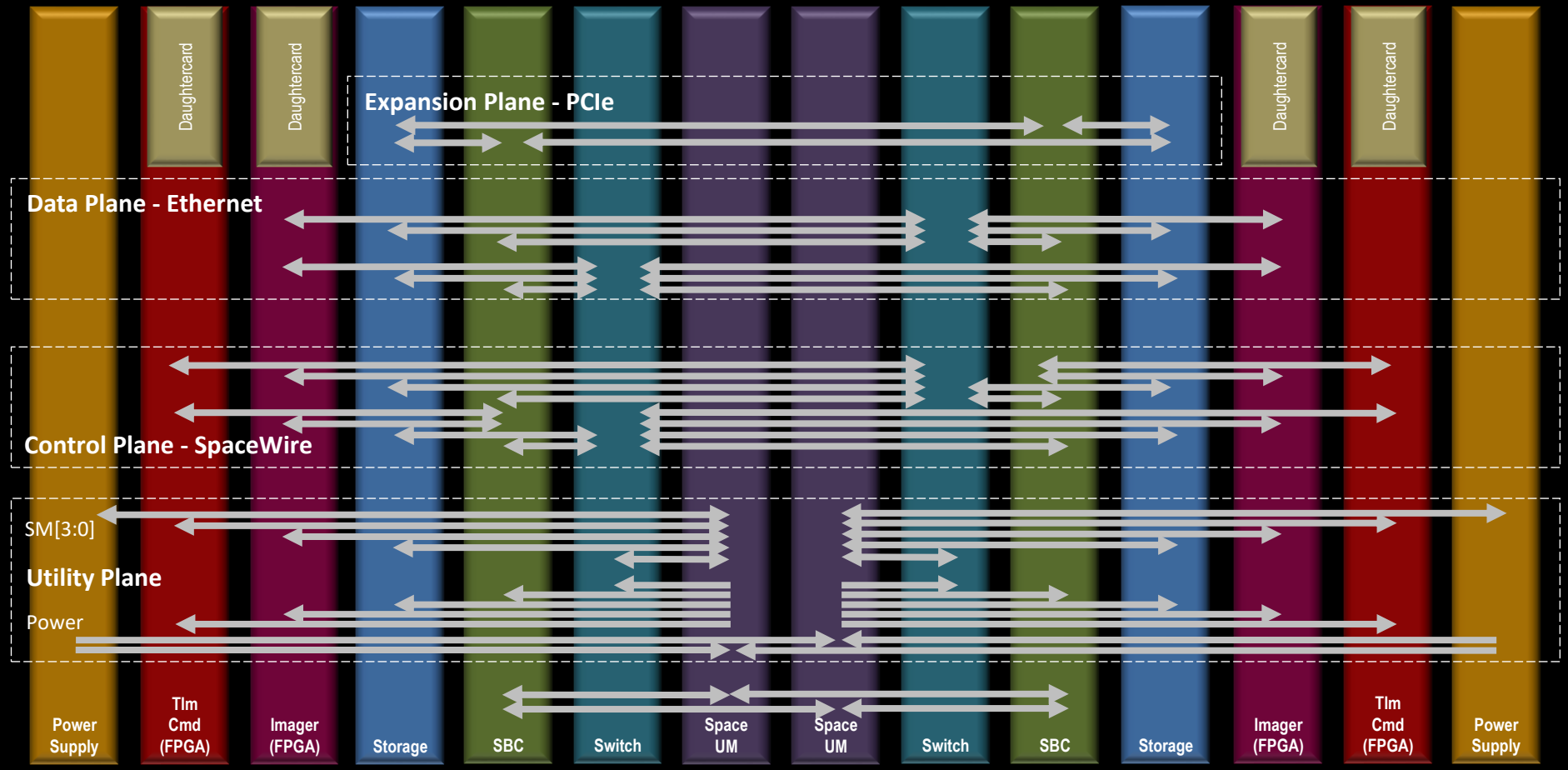
Based on the use cases and the proposed NASA SpaceVPX specification, candidate modules were defined

- Single Board Computer (SBC)
- High Density FPGA
- Low Density FPGA
- Storage
- Digitizer
- Switch

Example Systems

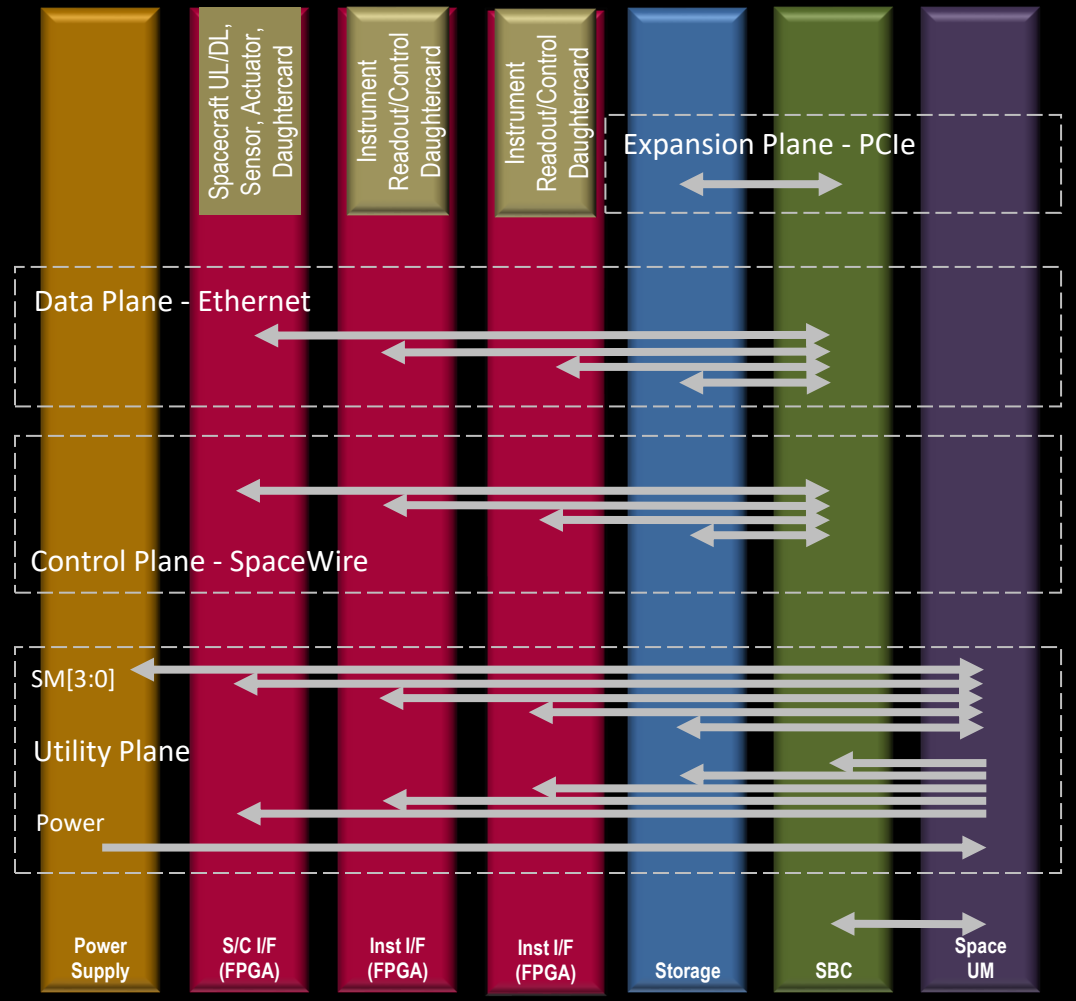
Based on the candidate module definitions and proposed NASA SpaceVPX specification, example systems were defined

- Redundant 3U system
- Single string 3U systems (SmallSat avionics, instrument controller)
- Minimalist systems
- Interim systems supporting legacy cPCI modules



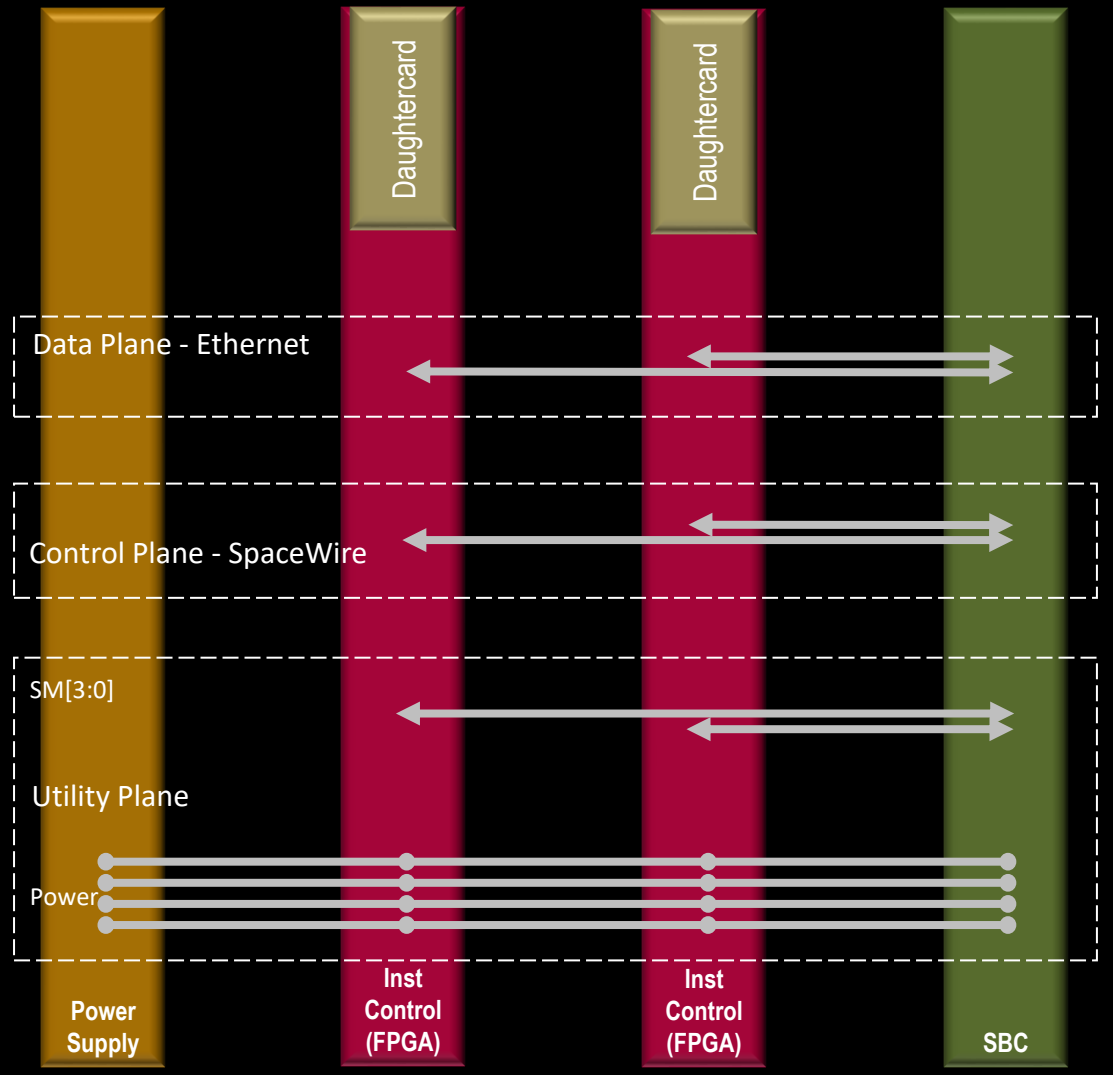
Redundant 3U System

Example Systems



Single String 3U SmallSat Avionics

Example Systems



Minimalist System

In Closing …

NASA has released its envisioned future for advanced avionics

- We welcome your input!

The High Performance Spaceflight Computing (HPSC) processor development is key to NASA's envisioned future

- 100X the scalar processing performance of the existing RAD750
- Vector processing and machine learning acceleration
- Wide range of power/performance/fault tolerance flexibility

NASA has recently completed a study to assess SpaceVPX interoperability challenges and define a proposed solution

- Using the NASA study recommendations as a starting point for discussion, NASA would like to engage with the spaceflight avionics community to determine if consensus can be readily achieved on developing a SpaceVPX VITA78 'dot spec' that enhances interoperability
- Again, we welcome your input!

Questions?

Acronym List

ADCSS	Avionics, Data, Control and Software Systems	GPS	Global Positioning System	OpenCV	Open Source Computer Vision
AC	Alternating Current	GPU	Graphics Processing Unit	OpenGL	Open Graphics Library
AI	Artificial Intelligence	IEEE	Institute of Electrical and Electronics Engineers	OpenMP	Open Multiprocessing
ASIC	Application Specific Integrated Circuit	IPMI	Intelligent Platform Management Interface	OSAM	On Orbit Servicing Assembly and Manufacturing
cFE/cFS	Core Flight Executive/Core Flight Software	HPSC	High Performance Spaceflight Computing	PCIe	Peripheral Component Interconnect Express
cPCI	Compact Peripheral Component Interconnect	HW	Hardware	POL	Point of Load
CPU	Central Processing Unit	I/O	Input/Output	RISC	Reduced Instruction Set Computer
C&DH	Command and Data Handling	ISA	Instruction Set Architecture	RTOS	Real Time Operating System
DAP	Direct Access Protocol	ISRU	In Situ Resource Utilization	SAR	Synthetic Aperture Radar
DLC	Decent and Landing Computer	JESD	Joint Electron Device Engineering Council Standard	SBC	Single Board Computer
ELCSS	Environmental Control and Life Support System	JPL	Jet Propulsion Laboratory	SCC	Space Computing Conference
EDL	Entry Descent and Landing	JTAG	Joint Test Action Group	SERDES	Serializer Deserializer
EMIT	Earth Surface Mineral Dust Source Investigation	LCRD	Laser Communication Relay Demonstration	SPIR	Standard Portable Intermediate Representation
ESPA	Evolved Expendable Launch Vehicle (EELV) Secondary Payload Adapter	LEO	Low Earth Orbit	SPLICE	Safe and Precise Landing – Integrated Capabilities Evolution
EVA	Extra-Vehicular Activity	LLVM	Low Level Virtual Machine	SRIO	Serial RapidIO
FFT	Fast Fourier Transform	LTV	Lunar Terrain Vehicle	STMD	Space Technology Mission Directorate
FPGA	Field Programmable Gate Array	LUVOIR	Large Ultraviolet Optical Infrared Surveyor	SW	Software
fps	Frames per Second	LVCMOS	Low Voltage Complimentary Oxide Semiconductor	SWaP-C	Size Weight and Power, and Cost
FMC	FPGA Mezzanine Card	ML	Machine Learning	TTE	Time Triggered Ethernet
FSW	Flight Software	mV	Millivolt	TSN	Time-Sensitive Networking
Gbps	Gigabyte	NASA	National Aeronautics and Space Administration	VCU	Vehicle Control Unit
Gbps	Gigabits Per Second	NESC	NASA Engineering & Safety Center	VITA	VMEbus (Versa Module Eurocard Bus) International Trade Association
GCC	Gnu Compiler Collection	OpenCL	Open Computing Language	XMC	Express Mezzanine Card