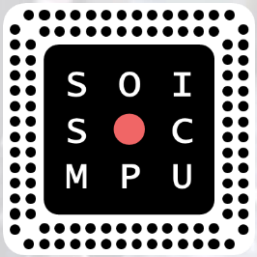

Introduction of a Space Glade Micro Processing Unit for Future Space Applications

Keita Sakamoto

Japan Aerospace Exploration Agency (JAXA)

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1. Background

- ✓ Space activities has started since 1955 in Japan. (2003 ~ JAXA)
  - ✓ About 35 types of rockets have been developed and launched. (More than 300 satellites)
  - ✓ EEE parts for space-use have been supporting to do space activity for a long time.

☐ **H-2**
- **1988 ~ 1999**

Purely Domestic

☐ **H-2A**
- **2001 ~**
- **for almost satellites**

Domestic & Overseas

☐ **H-2B**
- **2009 ~ 2020**
- **for cargo**

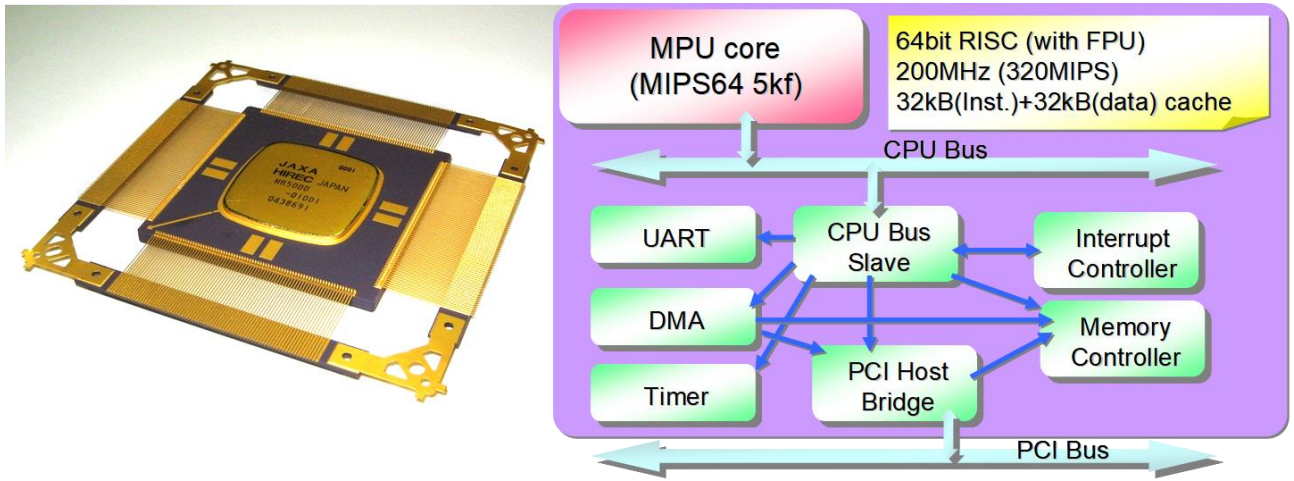
Domestic & Overseas

☐ **H-3**
- **Under development**

COTS-base

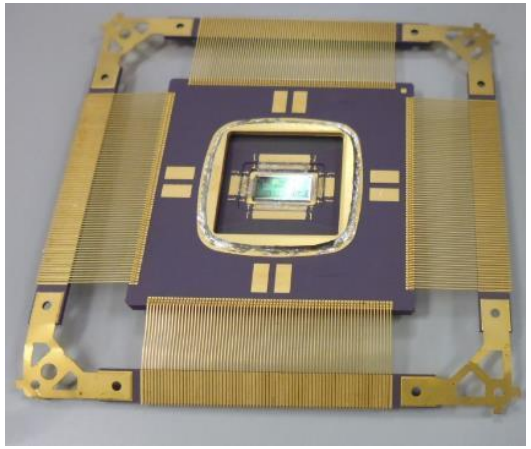
1. Background

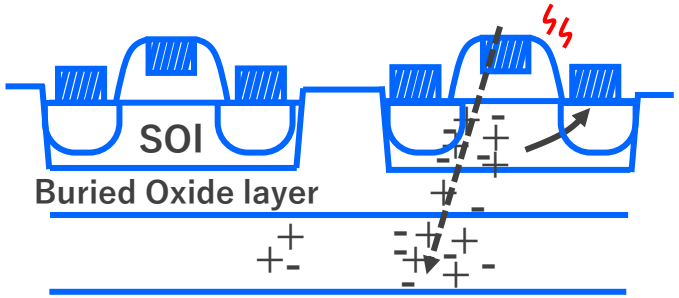
Current MPU: HR5000 (Bulk CMOS) and HR5000S (SOI)



- MIPS64 5kf architecture with on-chip peripherals.
- 0.18μm commercial CMOS process.
- 200MHz operation (320MIPS)
- JAXA qualified. (Mar. 2007)

SOI Process
0.15 um





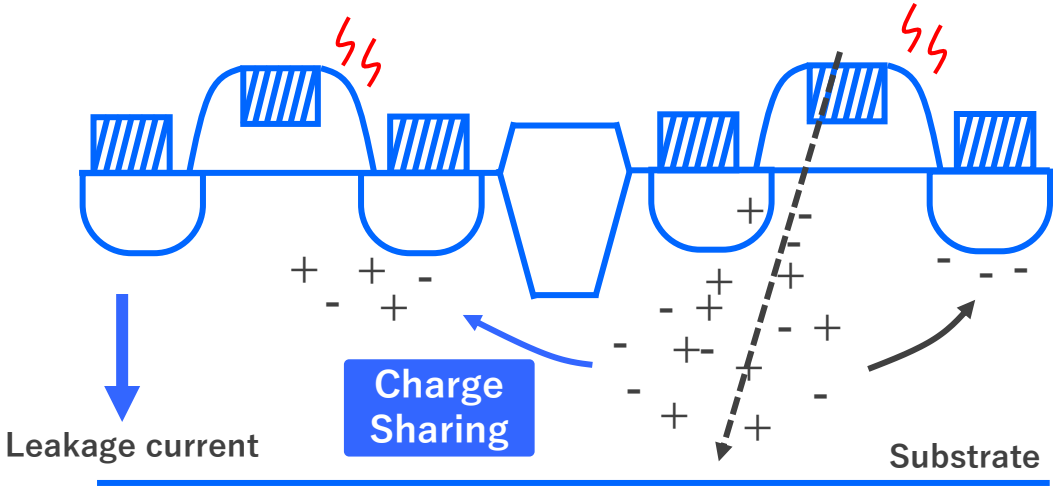
Conceptual drawing of SOI process

SOI technology is introduced to the MPU as a radiation hardening methodology

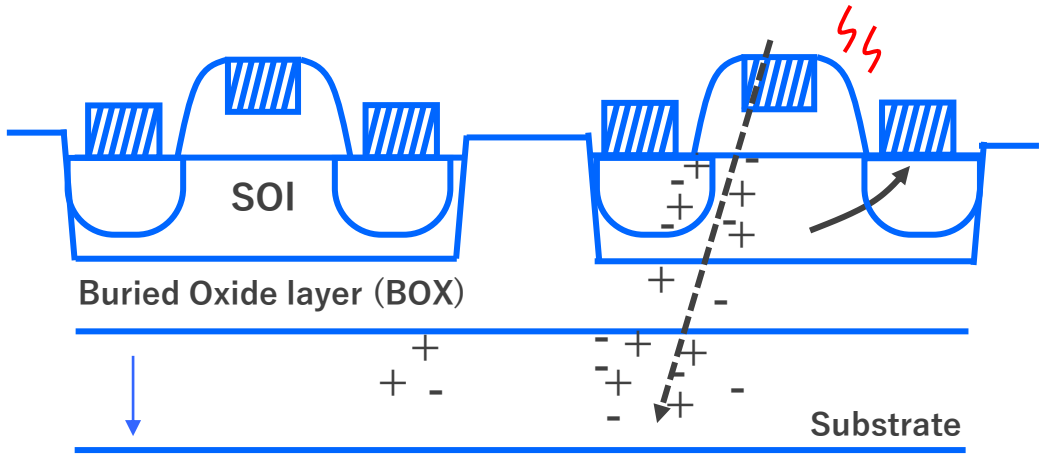
1. Background

The differences between Bulk process and SOI process

Bulk

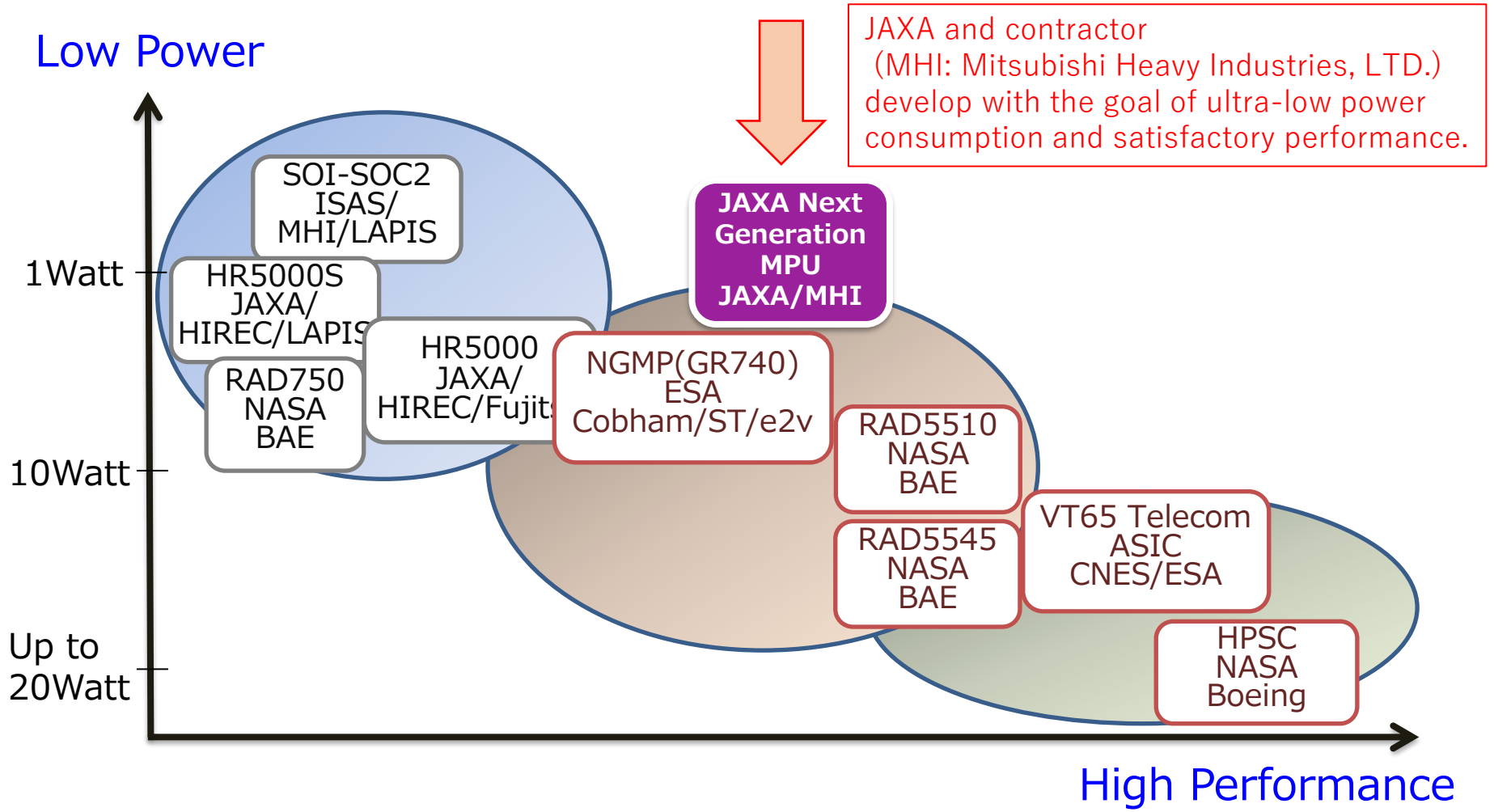


SOI



- Advantages of SOI process
  - Device structure of SOI process itself can prevent charge sharing effect ➔ Good Radiation Tolerant
  - Leakage current can be well suppressed. ➔ Low power consumption

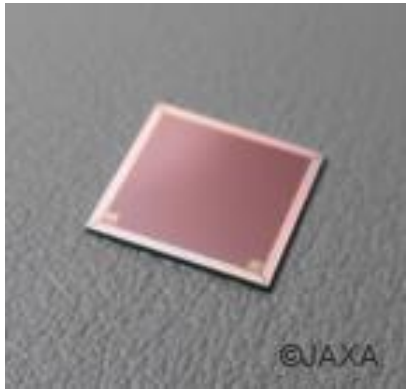
2. Benchmarking



Position of JAXA Next Generation MPU in Global MPU Tendency

3. Device features of the next MPU

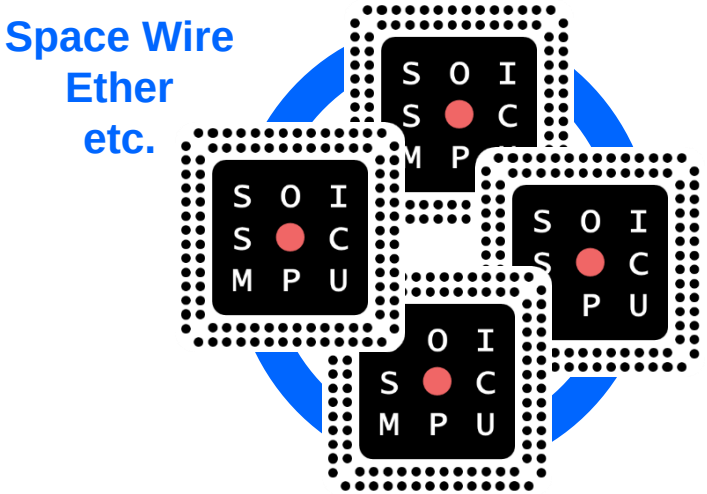
- Micro Processing Unit (MPU) for next decade
  - Dual Core processor (RXv3, Renesas Electronics)
  - A variety of Interface protocols (Space Wire, Ethernet,..etc)
  - High reliability as a space glade (JAXA-QTS-2010)
  - On-chip code memory (SRAM)
- Features
  - Low power consumption; SOI process
  - High Radiation tolerance
  - Cluster connection for High Availability (HA) and/or High-Performance Computing (HPC)

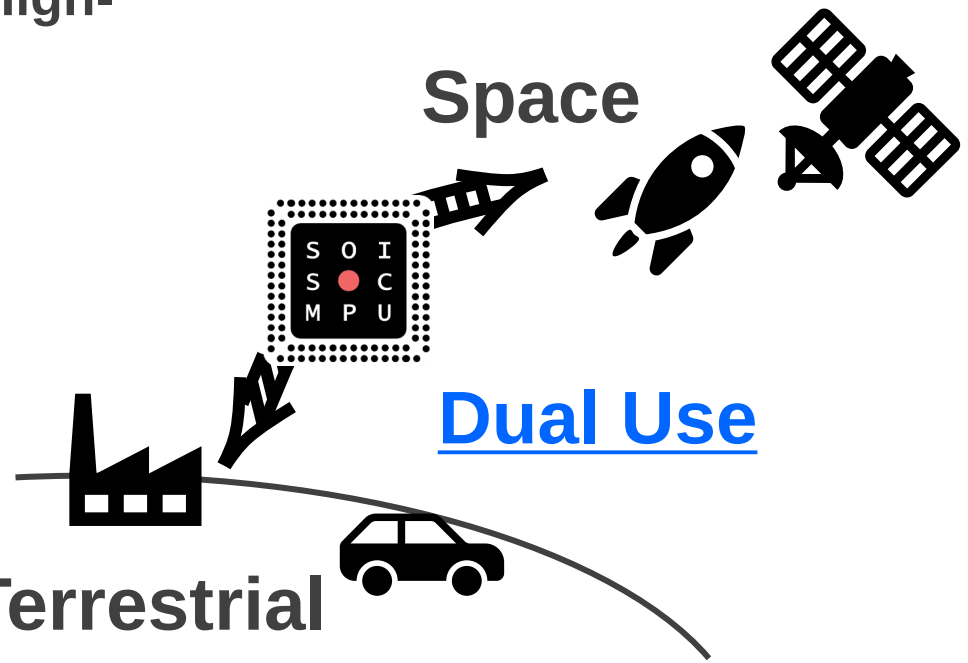


Engineering Model sample

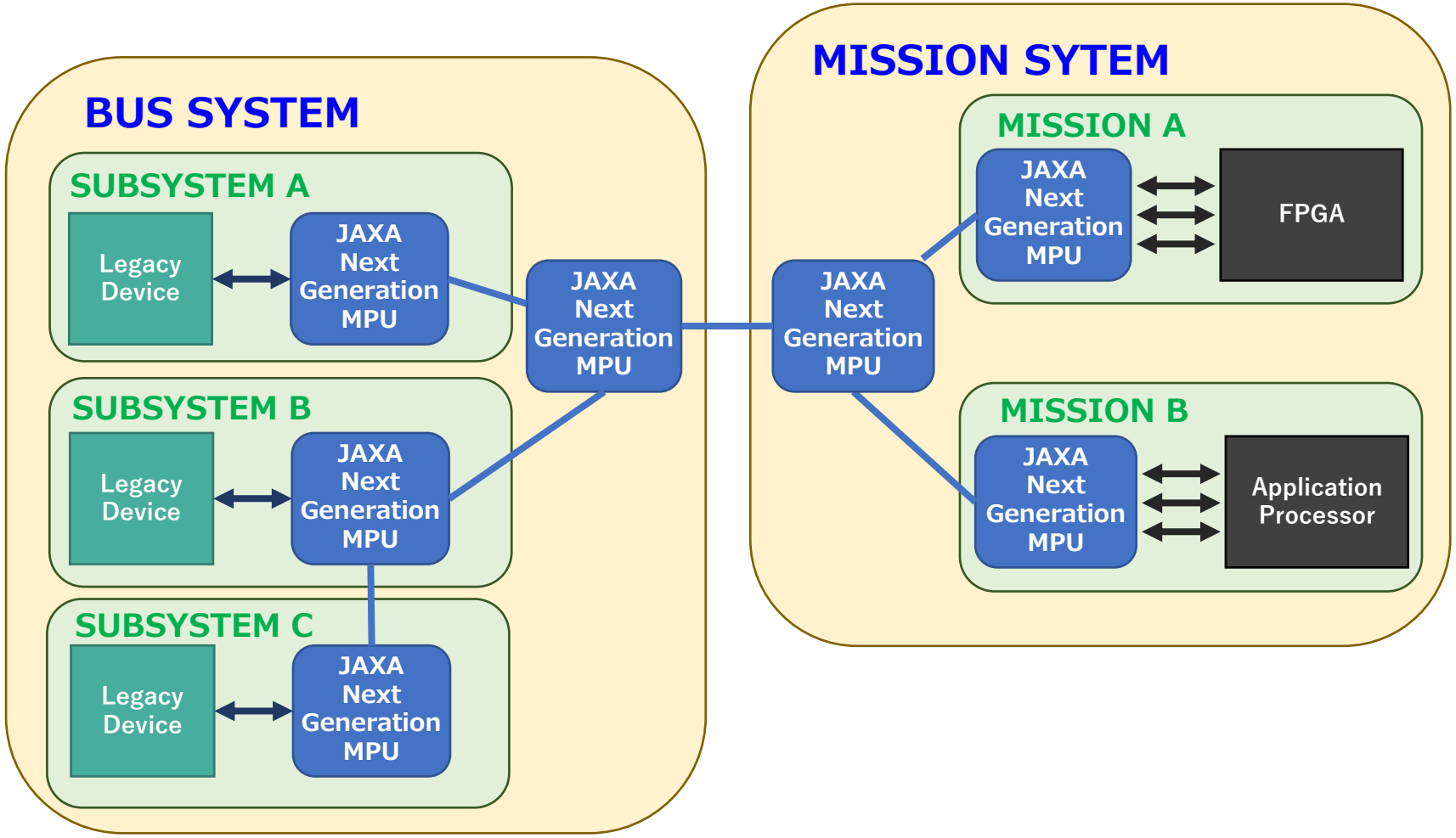
Concept

- Dual Use
- Low power
- High reliability
- Middle performance
  - ➡ Cluster connection





3. Device features of the next MPU



Various I/Os widely support from legacy devices to future interfaces.

Network I/Os improve development efficiency by distributed system.

4. Target specifications

Architecture

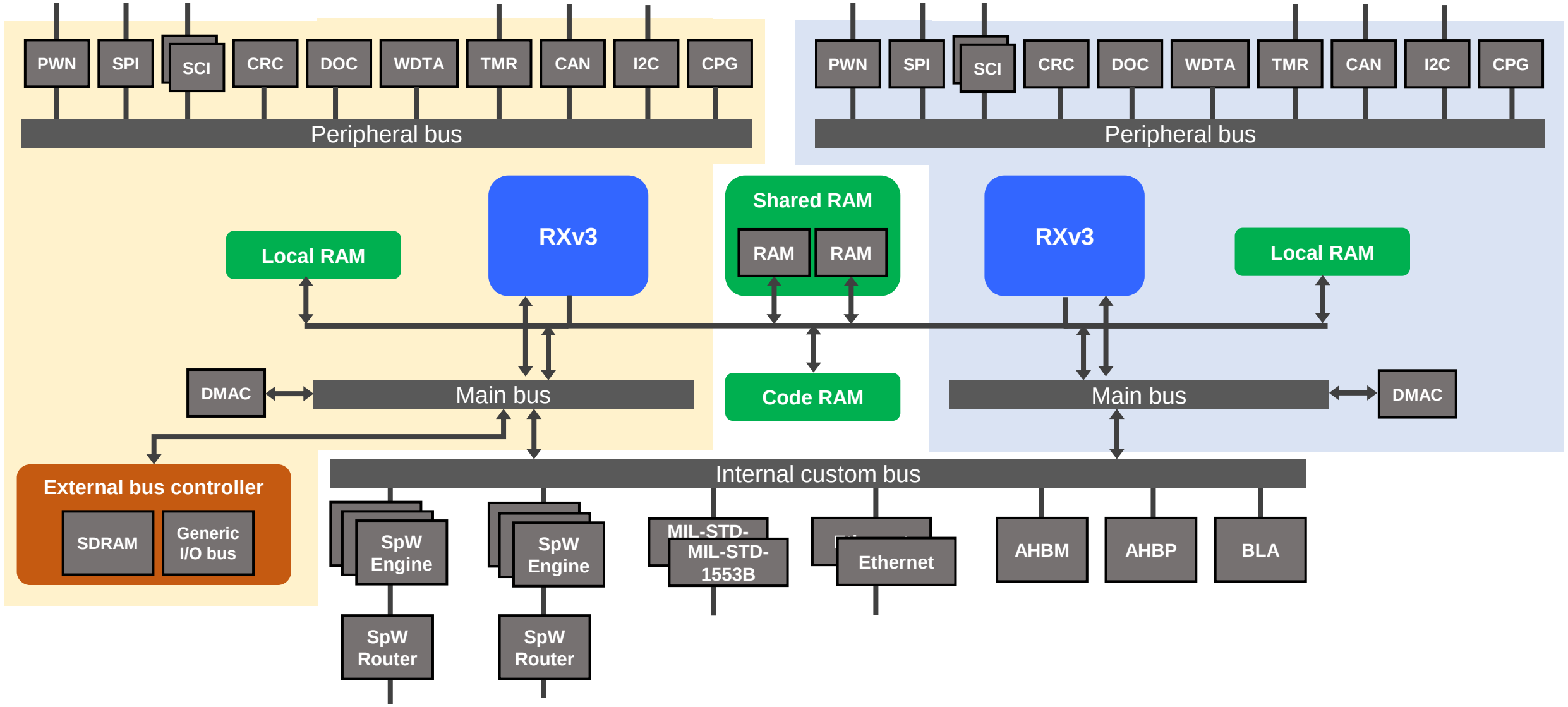
SoC: interfaces

Qualification & Reliability

Function	Parameter	Description
Core & Memory	Dual Core (RVv3)	Double-precision floating point
	Frequency	250 MHz (900 CoreMark; 10x larger than that of current MPU) @PVT=Typical
	On-chip memory	HD-SRAM w/ EDAC ・Instruction-RAM ・Data-RAM RHBD-SRAM w/ EDAC ・Data-RAM
	Power consumption	< 1 W @PVT=typical
Interface	Space Wire Driver	6 channels
	Ethernet	2 channels
	MIL-STD-1553B	2 channels
	CAN	2 channels
	SCI	4 channels
	SPI	2 channel
	I2C	2 channel
Hard-Macros	Security-IP	Elliptic Curve Cryptography

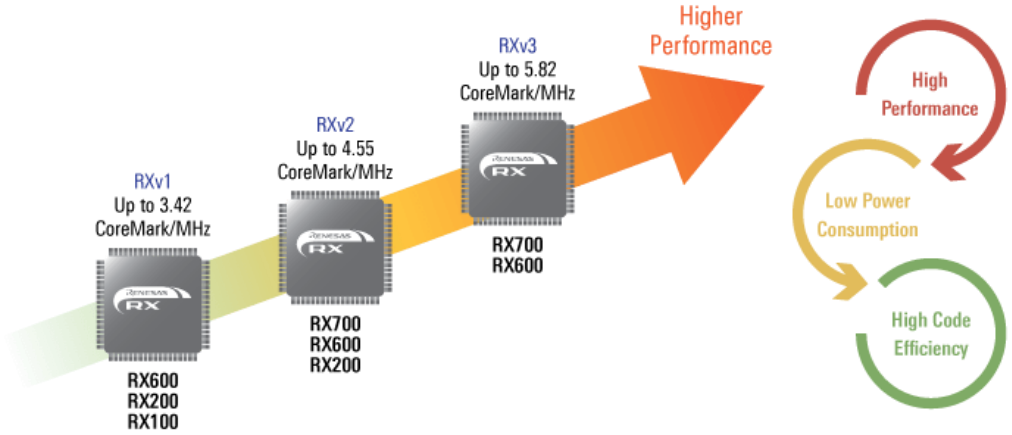
Qualification guideline	Target
JAXA-QTS-2010C	Specification for space glade LSI

5. Device architecture (Function block diagram)



5. Device architecture (RXv3)

- RXv3-based Core architecture (We combined an FPU module with RXv3 architecture)
- One of the RX-series (Renesas) which is implemented into industry, commercial, etc.



- 32bit CISC Harvard Architecture
- 5-stage pipeline
- FPU
- Up to 6.01 Coremark/MHz
- Low power consumption

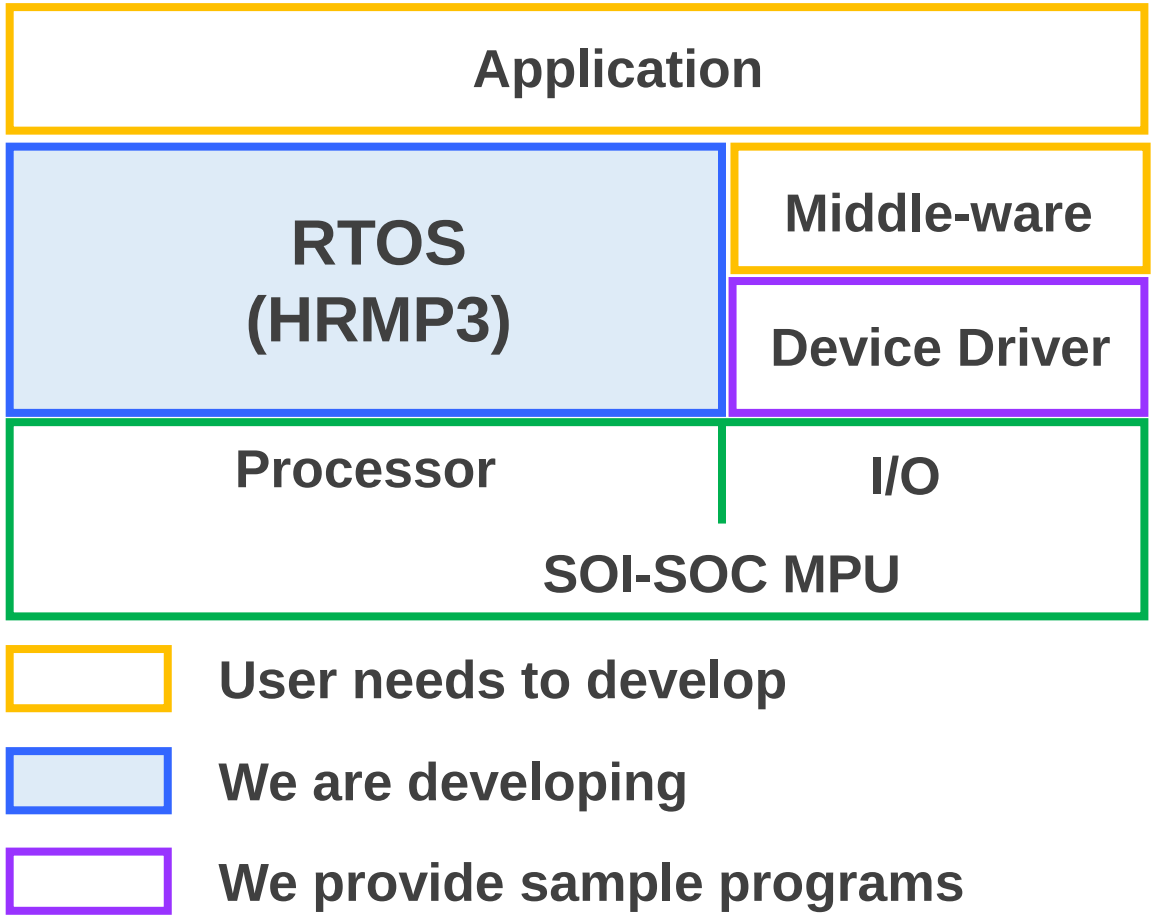
https://www.renesas.com/jp/en/products/microcontrollers-microprocessors/rx-32-bit-performance-efficiency-mcus/rx-features

- Evaluated score on the SOI-SOC MPU (Engineering model)

Device	Score [Coremark/MHz/Core]	
	CPU0	CPU1
HR5000S	1.54	-
SOI-SOC MPU	4.82	-
SOI-SOC MPU	2.61	2.6

6. Operating System

- Realtime Operating System (RTOS) which is suitable for our MPU is under developing.
  - Base model is TOPPERS/HRP (High Reliable system Profile) kernel (HR5000S).
  - Beta-version has already released and built in the MPU (EM) for evaluation.
  - Evaluation combined RTOS with Printed Circuit Board has completed.



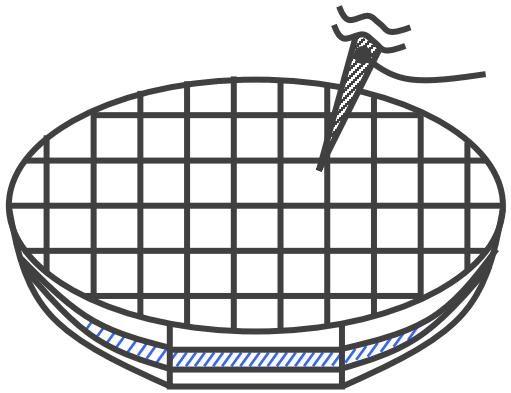
On-orbit demonstration under cinsideration

7. Evaluation (Wafer-test)

☐ Function ✓ Completed

- Memory built-in self test (M-BIST) for static random-access memory (SRAM) region
- DC function test
- AC function test
- Loose function test
- SCAN test for distributed logic circuit (combinational logic & sequential logic)
- PLL function

Desired logic functions were validated



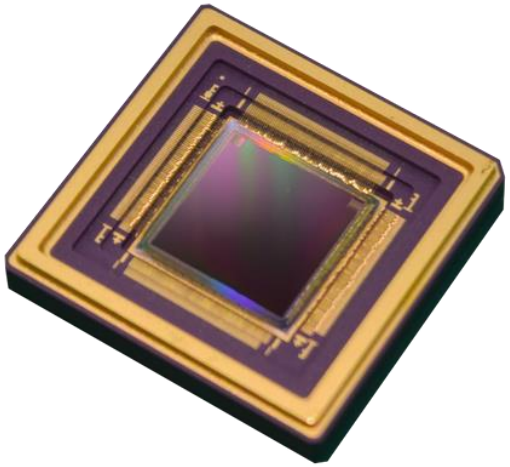
☐ Performance ✓ Completed

- SCAN test for critical path of distributed logic circuit
- IDDQ, IDDA

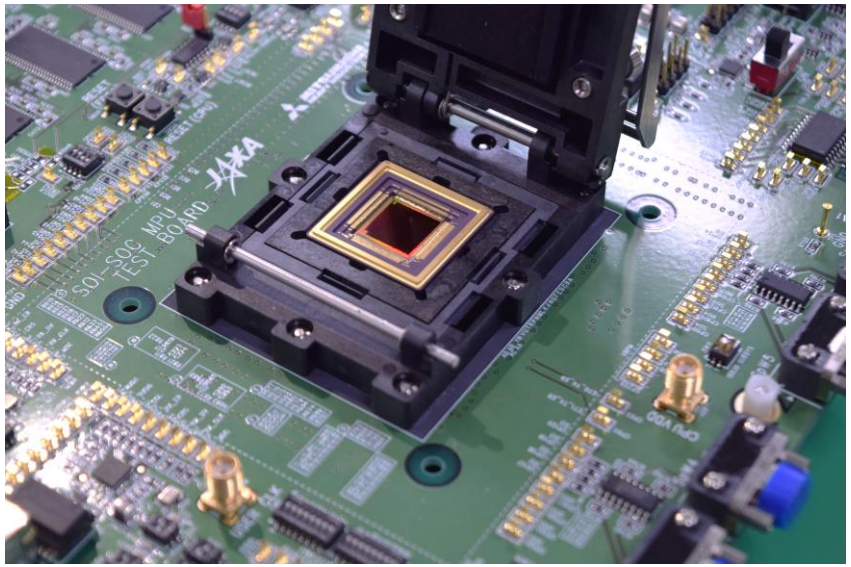
Operating frequency & power consumption were validated

7. Evaluation (On-board test)

- We’ve designed and manufactured printed circuit boards for evaluation test
  - Electronical evaluation (including operating performance)
  - Functional evaluation (including communicate with peripheral chip)
    - Quick-sort
    - CoreMark Score
    - Space Wire communication program
  - Radiation test (SEE, TID)



Photograph of EM-chip assembled on a BGA package



Photograph of evaluation board

7. Evaluation (Brief summary of the test results)

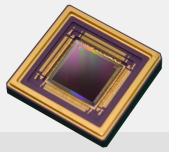
☐ **Below table shows the test results of both electrical and radiation test**

Evaluation	Result	Comment
Frequency	280 MHz (max.) @PVT=Typical	Benchmark program (CoreMark)
Performance [CoreMark@250MHz]	800 ~ 1200	Depending on the operating configuration
Power Consumption	0.787 W @PVT=Typical	CPU0: CoreMark CPU1: Space Wire
Radiation	• SRAM w/ RHBD: 40 MeV/(mg/cm^2) • SRAM w/ EDAC: 40 MeV(mg/cm^2) • SEL: ≧ 80 MeV/(mg/cm^2) @ 125^{o}C • EM-chip: ≦ 100FIT	

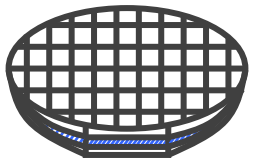
8. Development schedule

- Wafer process has been finished
- Wafer Test and assembly are on-going
- Final qualification test will start soon
- Development of this MPU will be finished until the middle of JFY 2023

Phase	~ JFY2021	JFY2022				JFY2023	
		4	7	10	1	4	7
EM	Evaluation (EM-chip)						
QM		QM design	Wafer fabrication (BBM, ES)	Wafer test Assy.			
			Wafer fabrication(QM)		Wafer Test & Assy. & Final Qualification Test		



- Completed !
  - Wafer Electrical Test
  - Board Electrical Test
  - Radiation Test
  - OS verification
  - Preliminary Qualification Test



Thank you for your kind attention

URL of this MPU

http://www.kenkai.jaxa.jp/eng/research/soisoc/soisoc.html

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