Microchip Radiation Tolerant FPGAs

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

Tim Morin

March 15, 2023

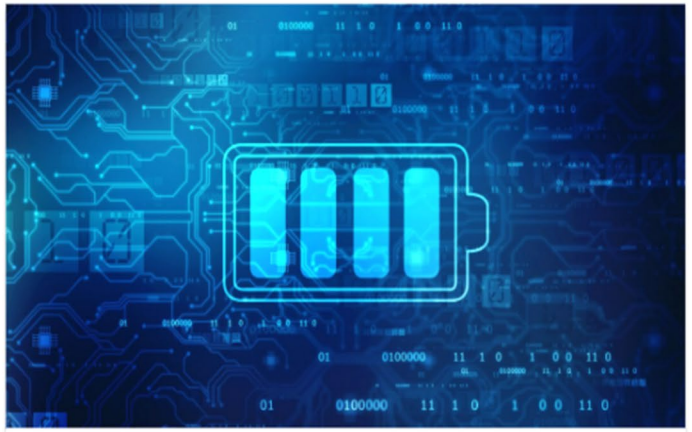
Agenda

- **Quick Product Update**
  - RT PolarFire® FPGA
  - RTG4™ FPGA

- **Microchip and RISC-V – The Road Less Traveled**

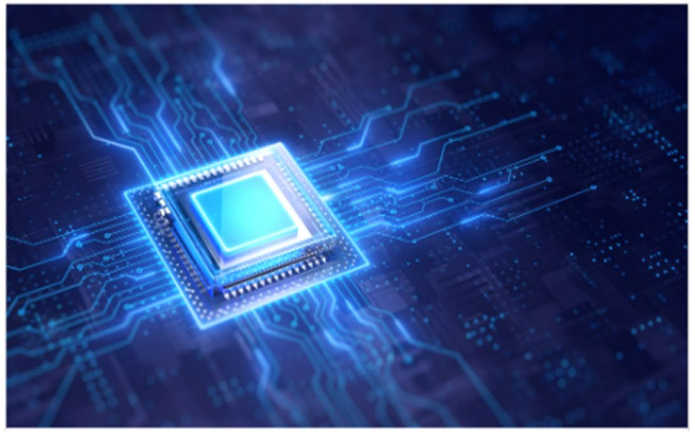
Microchip FPGA Vision and Differentiation

To enable innovation by offering the most power-efficient programmable solutions



2x

Power Efficiency



Exceptional Reliability

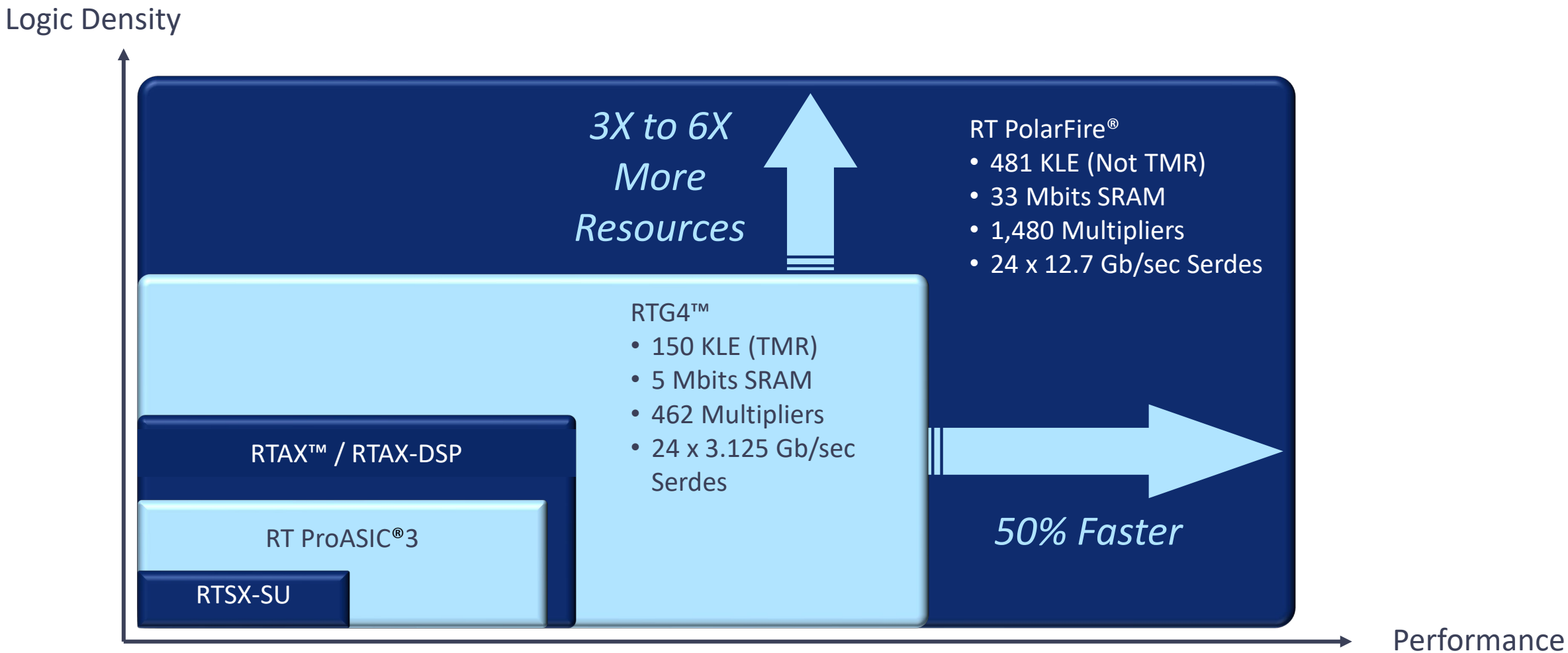
Zero Configuration Upsets

Military-Grade Security

Best Anti-Tamper and Cybersecurity

MICROCHIP

RT FPGA Families



MICROCHIP

RT PolarFire® FPGA Overview

- **Two versions**
  - RTPF500T
  - RTPF500ZT

- **Both derived from commercial PolarFire**
  - 28 nm SONOS: Non-volatile and reprogrammable
  - Hermetically sealed, ceramic column grid array package
    - 1509 solder columns (Six Sigma copper spiral columns)
  - Robust TID, 100 krad
  - No configuration upsets
    - LET 80 MeV-cm^2/mg, fluence more than 5E^8 ions/cm^2
  - SEFI in reset circuit
    - 1 in 187 years, in GEO solar min

- **RTPF500ZT has enhanced capabilities**
  - Better SEL GPIO Performance
  - Better on-orbit programming methodology

RTPF500T Status

- **Qualification and availability schedule**
  - Engineering models, PolarFire dev kit–Available NOW
  - RT PolarFire dev kit with RTPF500T–Expected May 2023
  - MIL-STD-883B qualification for RTPF500T completed
    - B-flow and E-flow flight models available to lead times

MICROCHIP

RTPF500T/RTPF500ZT Radiation Summary

Fabric Flops / LSRAM

- SEU in flip-flops report

SEU	Errors /bit-day, Geo Solar Min	
	Fabric Flip Flops	Fabric LSRAM
Unprotected	~ $1e^{-7}$	~ $5e^{-8}$
Protected (TMR/EDAC)	~ $1e^{-11}$	~ $5e^{-15}$

Flip Flops : TMR with constrained placement

LSRAM : EDAC (SECDED)

RTPF500T/RTPF500ZT Radiation Summary

GPIO SEL

GPIO V_{DDI}	GPIO V_{DDAUX}	RTPF500T SEL LET_{TH} (MeV.cm²/mg)	RTPF500ZT SEL LET_{TH} (MeV.cm²/mg)
3.3V +3%/-5%	3.3V +3%/-5%	25*	37**
2.5V +3%/-5%	2.5V +3%/-5%	58	80
1.8V ±5%	2.5V +3%/-5%	58***	80****

Notes:

* Destructive SEL observed in RTPF500T 3.3V at LET > 25 MeV.cm²/mg

** Destructive SEL observed in RTPF500ZT 3.3V at LET 68 MeV.cm²/mg

*** Tested MPFS250T and saw SEL at LET=66, but since the LET_{th}=58 at 2.625V, LET_{th} should be equal or better at 1.89V

**** Not tested, but since we meet LET=80 at 2.625V, we should meet LET=80 at 1.89V

No other destructive SEL observed unless board decoupling capacitor requirements are not followed.

No uSEL observed on (VDD25/VDDA25) on RTPF500ZT

No SEL observed on HSIO

MICROCHIP

RTPF500T vs RTPF500ZT

		RTPF500T	RTPF500ZT
Part numbers start with		RTPF500T, RTPF500TL, RTPF500TS, RTPF500TLS	RTPF500**Z**T, RTPF500**Z**TL, RTPF500**Z**TS, RTPF500**Z**TLS
Packaging	CG1509, LG1509	Compatible	Compatible
Availability Qualification	Engineering Models	Now	1H 2024
	Mil Std 883 Class B Flight Models	Now	2H 2024
	QML Class Q Flight Models	1H 2023	2H 2024
	QML Class V Flight Models	Not Planned	2025
System Services	JTAG and SPI-Target In-Flight Programming	Supported	Supported
	SPI-Initiator In-Flight Programming	Not Supported	Support Planned *
	System Services on Temporary Exit of System Controller Suspend Mode	Not Supported	Support Planned *

* Pending testing and validation

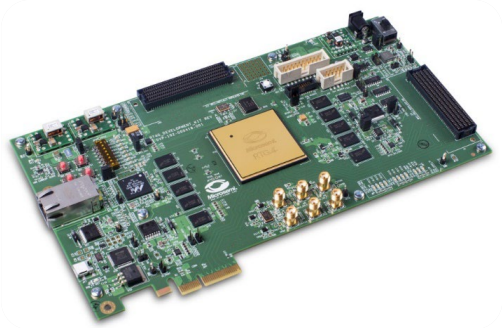
MICROCHIP

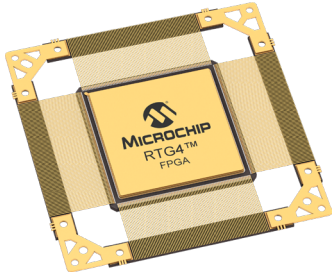
RTG4™ FPGA

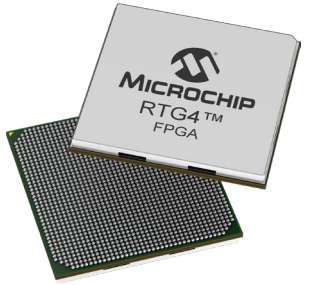
MICROCHIP

RTG4™ FPGA Qualification and Availability

	RT4G150-LG1657	RT4G150-CB1657	RT4G150-CG1657	RT4G150-CQ352	RT4G150-FC1657, FCG1657
Package Type	Ceramic Land Grid 1657	Ceramic Ball Grid 1657	Ceramic Column Grid 1657	Ceramic Quad Flat Pack 352	Plastic Ball Grid 1657
Development Kit	-	Available Today	Available Today	-	-
Daisy Chain	-	-	Available Today	-	Available Today
Mechanical Sample	-	-	-	Available Today	-
PROTO	Available Today	Available Today	Available Today	Available Today	Available Today
Flight Units – QML Q and V	Available Today SMD Published	-	Available Today SMD Published	Available Today SMD Published	-
Flight Units – Sub-QML	Available Today	-	Available Today	Available Today	Available Today







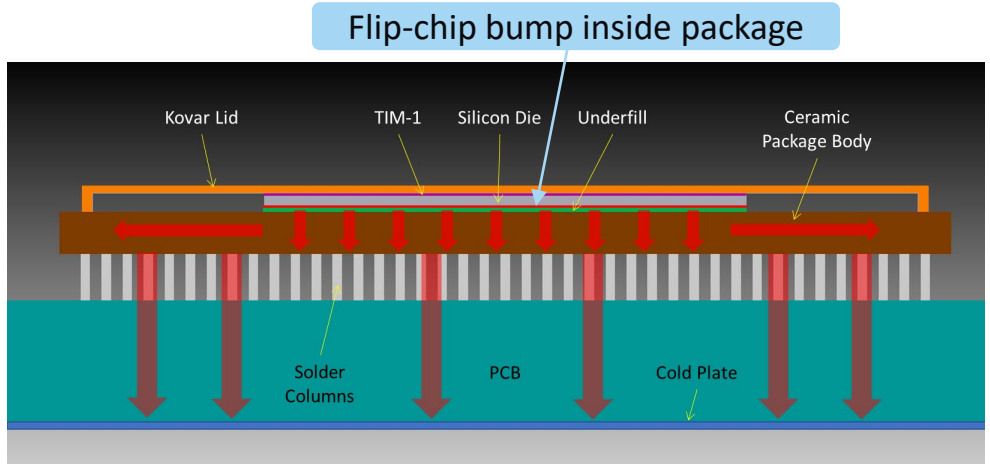
MICROCHIP

RTG4™ FPGA Screening Flows

Flow	Purpose	Package	Qualification	Screening			
				Burn-In	Temp Test	Life Test	DPA
V	NSS, NASA Class1	Hermetic Ceramic	QML-V	Static Dynamic	-55°C – 125°C	Wafer-Lot	Assy Lot
E	Advanced Traditional Space	Hermetic Ceramic	QML-Q	Static Dynamic	-55°C – 125°C	Generic Group C	Optional
B	Entry Level Traditional Space	Hermetic Ceramic	QML-Q	Dynamic	-55°C – 125°C	Generic Group C	None
R	New Space, Strategic Programs	Hermetic Ceramic	MIL-STD-883 Class B	Dynamic	-55°C – 125°C	None	None
Mil Ceramic	New Space, Strategic Programs	Hermetic Ceramic	MIL-STD-883 Class B	None	-55°C – 125°C	None	None
Mil Plastic	New Space, Strategic Programs	Plastic Non-Hermetic	JEDEC	None	-55°C – 125°C	None	None
PROTO	Prototyping	Plastic and Ceramic (Hermeticity not guaranteed)	None	None	-55°C – 125°C	None	None

RTG4™ FPGA Flip-chip Bump Change (1)

- **Background**
  - Leaded flip-chip bump material was discontinued by Microchip vendor
  - Impacting all RTG4 in ceramic packages (CG1657 and CQ352) in all screening flows
    - RTG4 in plastic package and RT PolarFire are NOT impacted. They always use lead-free bump



- **Plans**
  1. Issued RTG4 flip-chip bump customer notification
  2. Qualifying RTG4 lead-free bump parts
     - Mil-Std-883B qualification – expected 2H 2023
     - QML-Q qualification – expected 2H 2023
     - QML-V qualification – expected 1H 2024

RTG4™ FPGA Flip-chip Bump Change (2)

- **Customer notification**
  - Microchip PCN JAON-26GOCS315 released in November 2022
  - GIDEP SC7-C-23-0001 acknowledged

- **Important timelines for leaded-bump RTG4**
  - Last Time Buy (LTB): April 2023
  - Last Time Ship (LTS): April 2024

- **Replacement parts with lead-free bump**
  - All standard RT4G150 parts in CG1657 and CQ352 have equivalent replacement lead-free bump part
    - Ex: RT4G150-CG**G**1657B, RT4G150-CQ**G**352B
    - **G** references lead-free flip-chip bump for RTG4 FPGA family
      - No change to the Six Sigma columns which have lead content

- **No design impact when migrating to replacement parts**
  - No change in board design, reflow profile, board assembly flow or software setting

RTG4™ FPGA Flight Heritage

Mission Extension Vehicle 1 and 2 **Launched 2019, 2020**	**US National Programs** **Launched 2020**	**CAS-500** **Launched 2021**	**Landsat 9 (NASA)** **Launched 2021**	**Lucy (NASA)** **Launched 2021**
AIDA DART (NASA) **Launched 2021**	**Artemis-1 (NASA)** **Launched 2022**	**Worldview Legion** **Launch 2023**	**JUICE (ESA)** **Launch 2023**	**SLIM (JAXA)** **Launch 2023**

MICROCHIP

RT Update Conclusion

- **RT PolarFire® FPGAs**
  - MIL-STD-883B qualification for RTPF500T completed
  - RTPF500ZT has improved radiation performance, added system services and a path to QML-V qualification

- **RTG4™ FPGAs**
  - Leaded bump last-time-buy is April 2023
  - Ongoing lead-free bump qualification, anticipating MIL-STD-883B and QML-Q in 2023

- Microchip Space Forum
  - Free virtual on-demand presentations available now

- Sign up for Microchip Space Brief newsletter to receive quarterly updates

Microchip RISC-V Road Trip or The Road Less Traveled

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

Tim Morin


June 2015
2nd RISC-V Workshop
Berkeley California

The Road Trip

The Opportunity

When you come to a fork in the road take it

The Road Trip

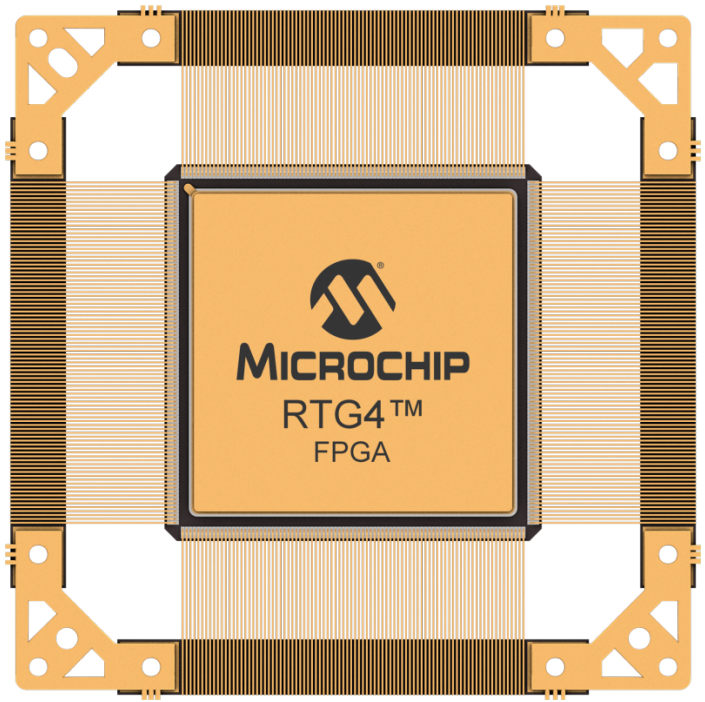
The Decision

What's around the corner?

MICROCHIP

The Opportunity

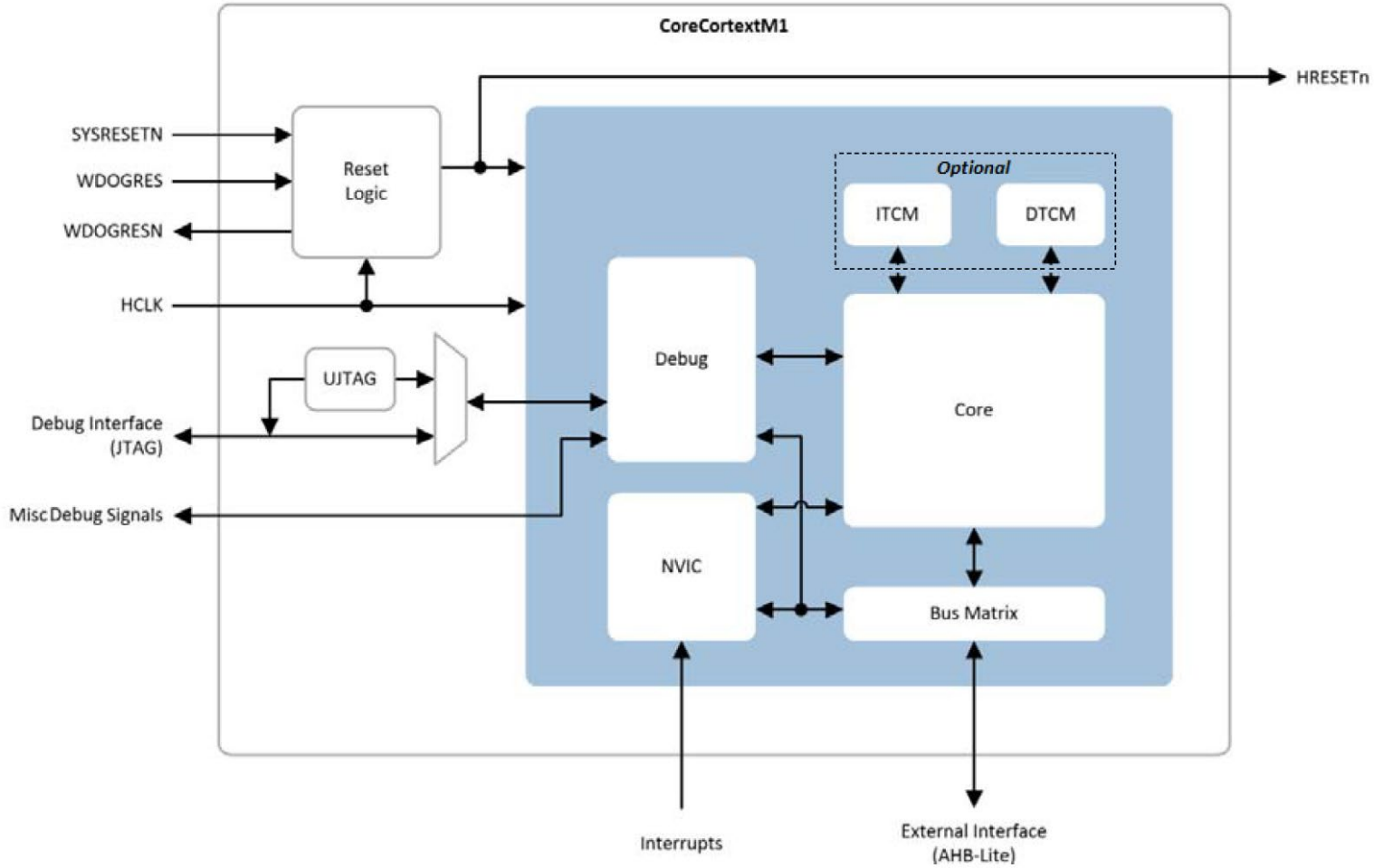
- A&D client building an assembly for a strategic platform
- Needs a soft CPU with Cache



What could go wrong?

ARM Cortex-M1

- **Jointly developed between Actel and ARM in 2006**



Unfortunately, no Cache

We get into the Soft RISC-V Business

- **1-page requirements document**
- **$ was exchanged**
- **3 months later the client was up and running with some basic code**

Soft RISC-V Platform RFI

Microsemi Soc Business unit is requesting a quote for the delivery of the following items.

- RISC-V RV321M core with the following features
  - hardware divide and optional barrel shifter
  - Integrated Cache controller
  - Interrupt controller
  - Debug environment
  - Cacheable and non-cacheable software defined memory regions
    - Software Enable/Disable I cache
    - Enable Software /Disable D Cache
    - Software Flush I cache
    - Software Flush D cache
  - 8Kbyte Instruction and Data Cache
  - >= 1 DMIPS/ MHz
  - AXI bus interface to main memory
  - AHB Bus interface to Peripherals
  - AHB Bus interface to Boot eNVM
  - 32 interrupts, prioritized
  - RISCV Standard Hardware debug
  - RISCV Standard watchpoints
  - 100MHz Operation on an M2S0090TS-FGG484 (Standard Speed Grade)
- A Uart for printf debug support
- A Timer for generating periodic interrupts
- C startup code for booting from internal eNVM in a M2S090TS-FGG484 device
- Test application software
  - Flushes Instruction and Data Caches and then enables them
  - Initializes and starts timers
    - Timer 1: 10 ms countdown, with interrupt on expiration
    - Timer 2: Free running counter
  - Initializes and enables interrupts
  - Test code for cache operation
  - sleep routines using free-running counter
  - Receives and handles 10 ms timeout interrupts
  - Receive interrupts, determine the source and handle it, then return to main routine
  - Exception handling routines
  - eNVM flash read/erase/program
- GCC tool chain V4.7, V4.9 or later
- All Source code under a BSD license
- Documentation

SiFive

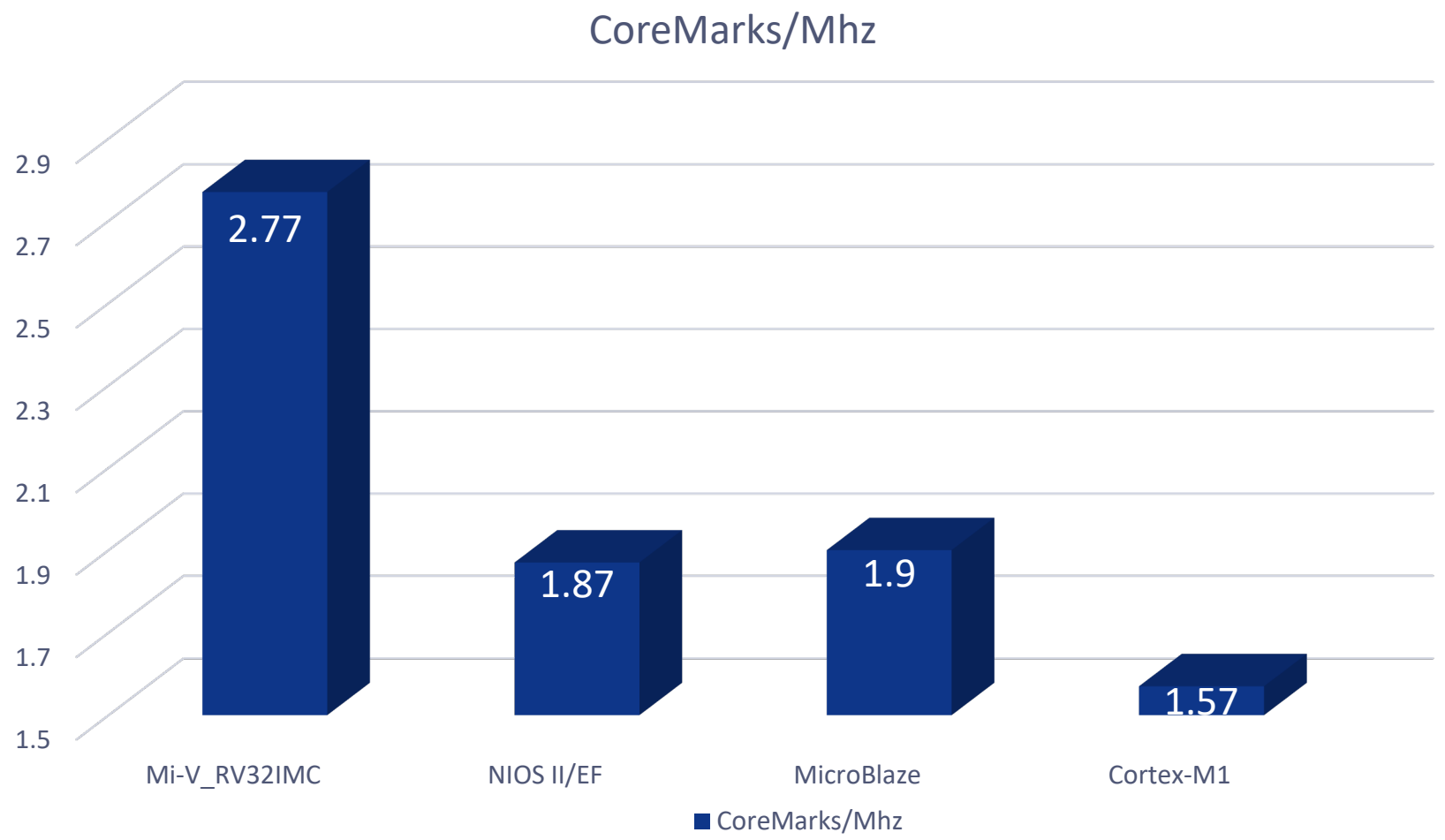
RISC-V is about business innovation

MICROCHIP

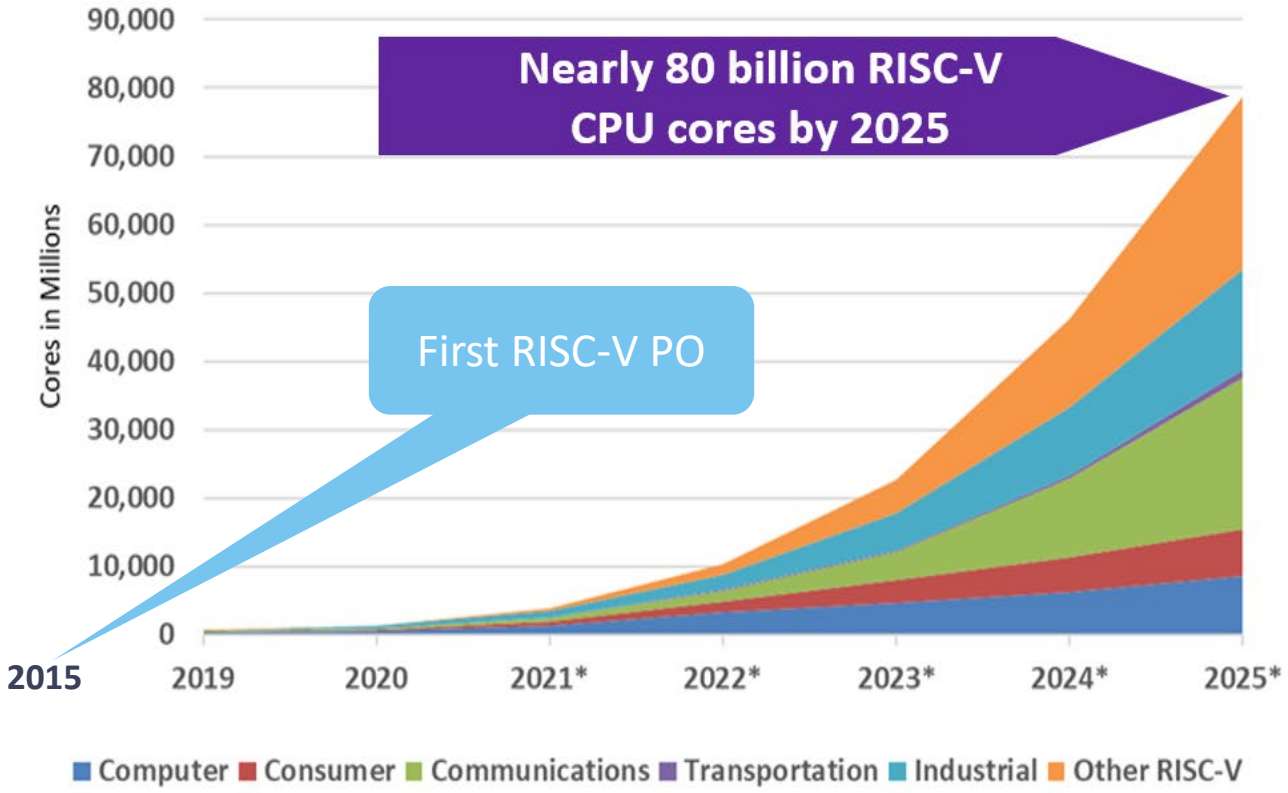
Mi-V RISC-V Soft CPUs

RISC-V Soft CPU	MiV_RV32	Mi-V_RV32IMAF_L1_AHB	Mi-V_RV32IMA_L1_AHB	Mi-V_RV32IMA_L1_AXI
LEs	4k-10k	26k	10k	10k
Coremark Score	0.177-2.77	2.01	2.01	2.01
Cache Size	Libero 2023.01	8KB I/D	8KB I/D	8KB I/D
Tightly Coupled Memory (TCM)	Yes-configurable depth to 256Kb	N/A	N/A	N/A
Compressed	optional	N/A	N/A	N/A
Mul/Div	Optional, MACC, Pipelined-MACC, or 32 cycle fabric (LEs)	Yes	Yes	Yes
Atomics	N/A	Yes	Yes	Yes
Floating Point	Libero 2023.01	Single Precision	N/A	N/A
Interface(s)	APB3/AHB/AXI	AHB	AHB	AXI
Debug	Optional	Yes	Yes	Yes
SECDED	Optional	Optional	Optional	N/A
Availability	Now	Now	Now	Now

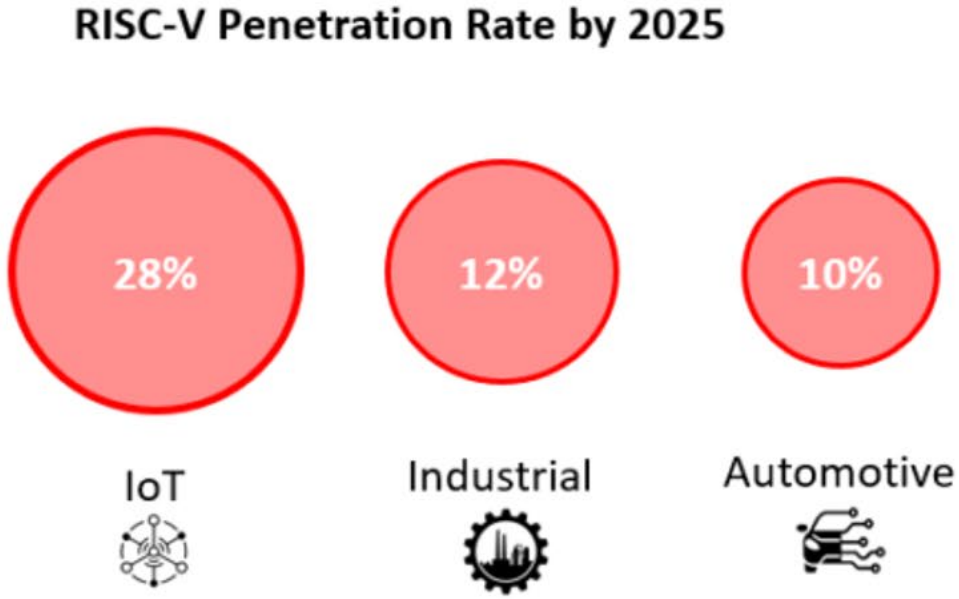
Benchmarks: Soft CPUs



RISC-V CPU core market grows 114.9% CAGR, capturing >14% of all CPU cores by 2025



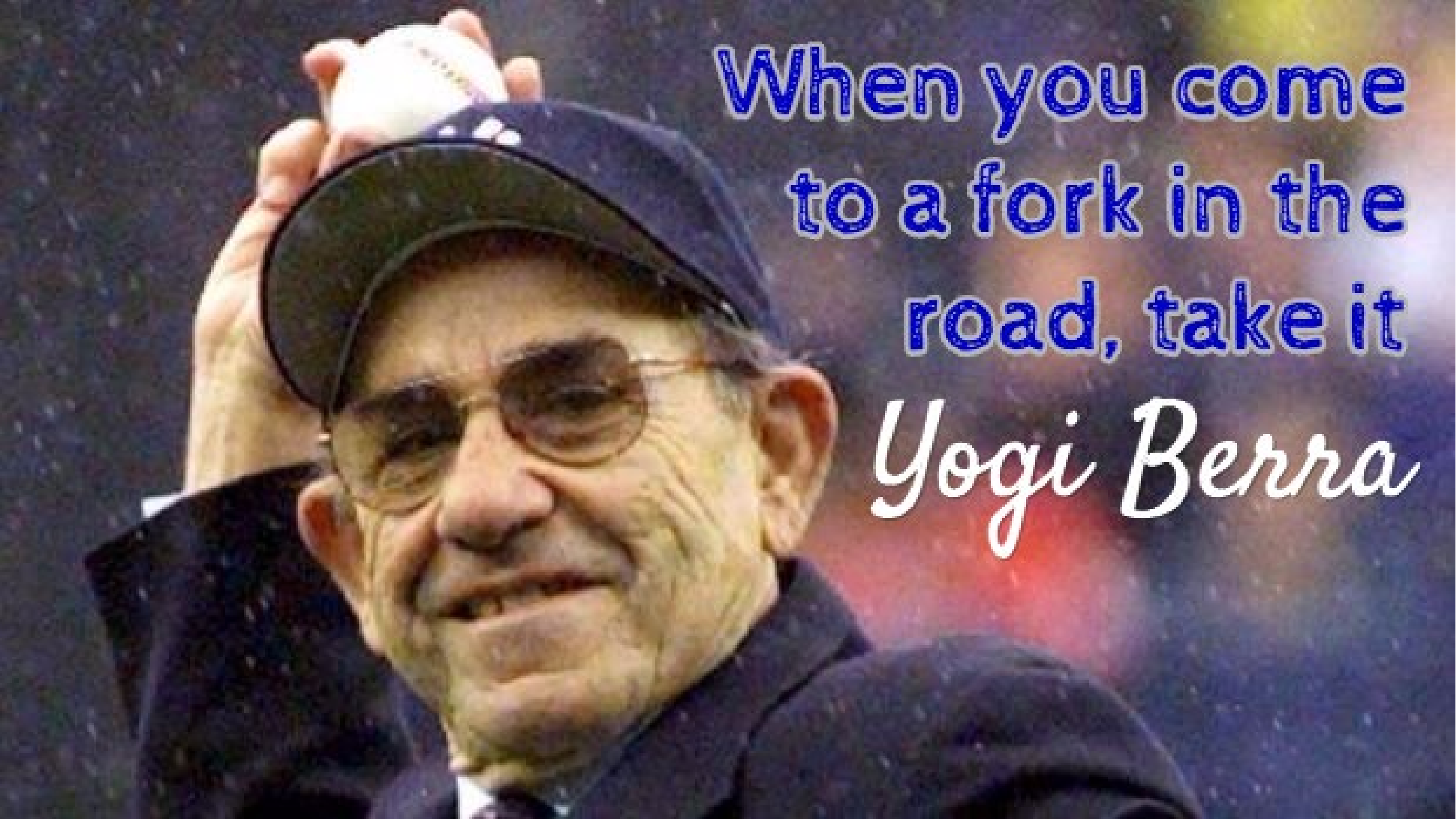
Source: Semico Research Corp, March 2021



"The rise of RISC-V cannot be ignored… RISC-V will shake up the $8.6 Billion semiconductor IP market."

-- William Li, Counterpoint Research

Source: Counterpoint Research, September 2021


When you come to a fork in the road, take it
Yogi Berra

Our next SoC FPGA platform needs to run Linux

ARM

- Mar
- Man
- Mar erlying hard
- Man

MICROCHIP

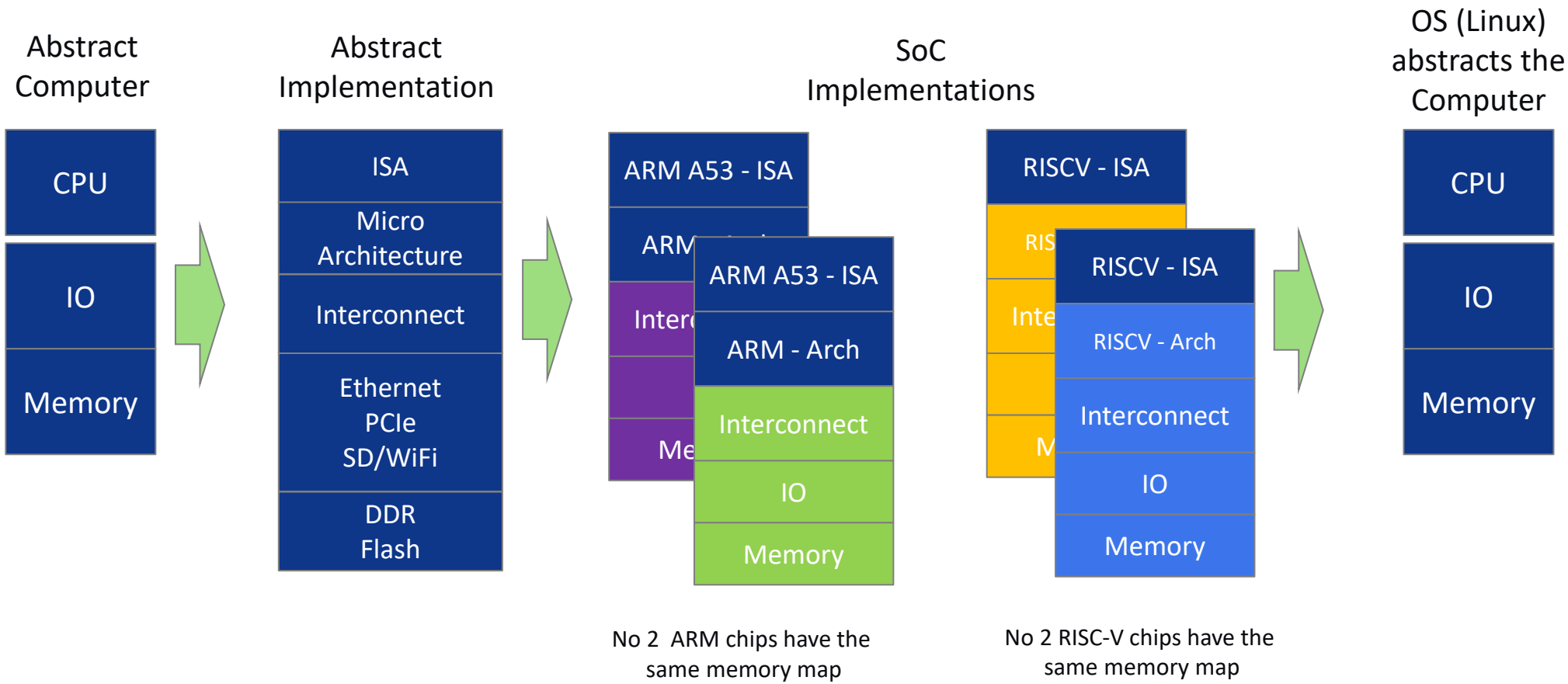
The Road Trip

Mission : bring back client validation to green light the next project

Have you heard of RISC-V?

But we use ARM!

Embedded Linux Adoption



Fragmentation in the ARM ecosystem drove the creation of the Device Tree in Linux
Making Linux even more portable

MICROCHIP

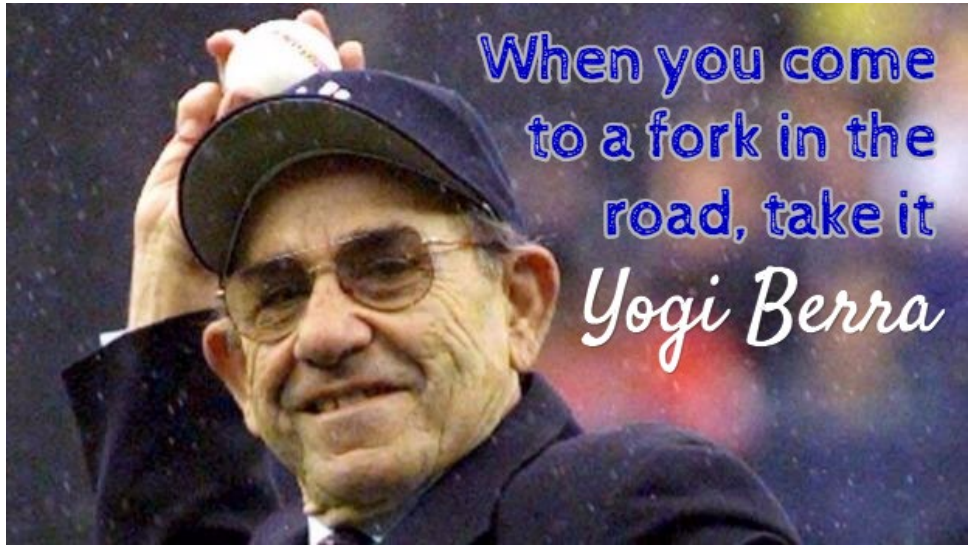
Diversity versus Fragmentation

Fragmentation: Same thing done different ways

Diversity: Solving different problems

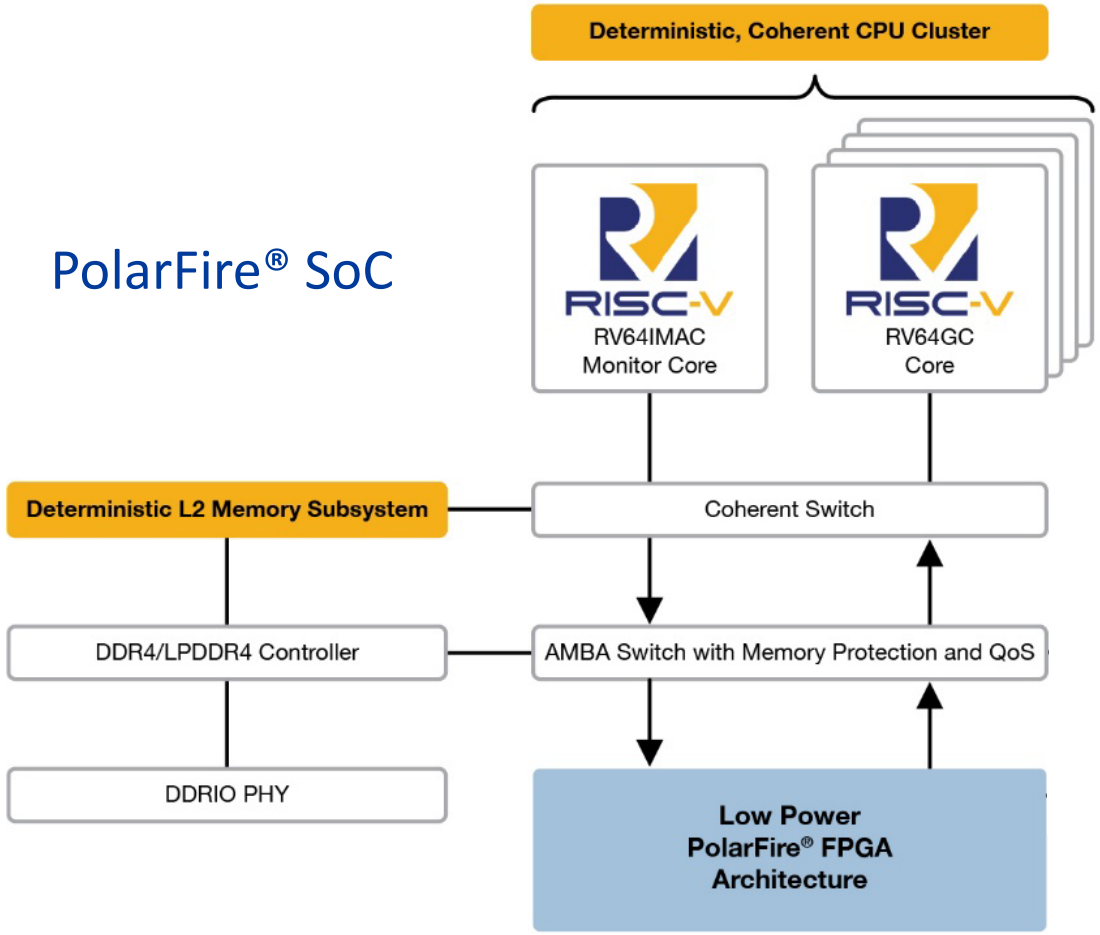
RISC-V®

The Decision



Enjoy Absolute Freedom to Innovate…

PolarFire® SoC



Asymmetric processing with 2X power efficiency

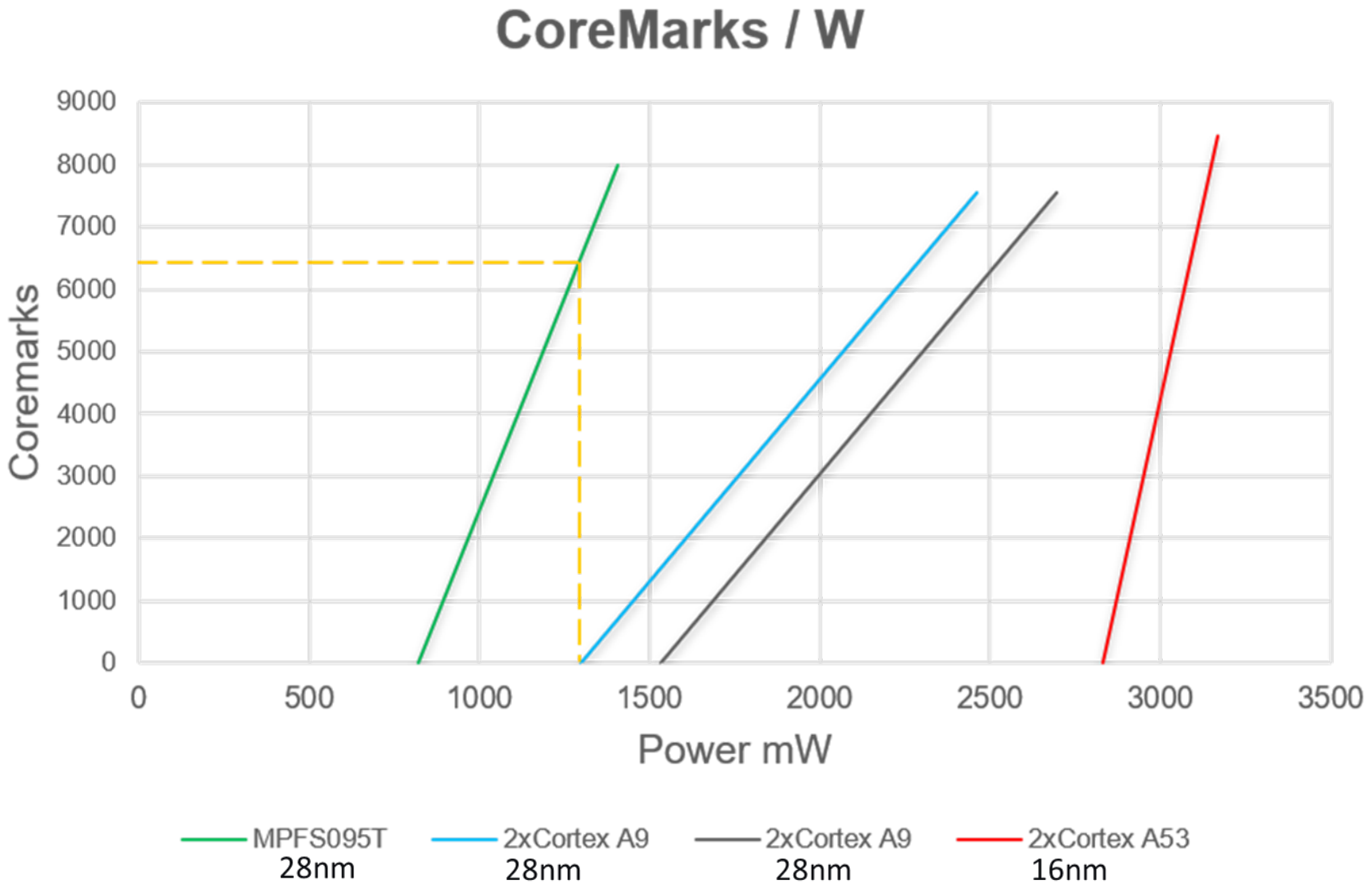
- Quad-core 64-bit RISC-V processors
- Linux® and Real-time operating systems

Highly flexible 2MB L2 cache

With the most comprehensive RISC-V development ecosystem

MICROCHIP

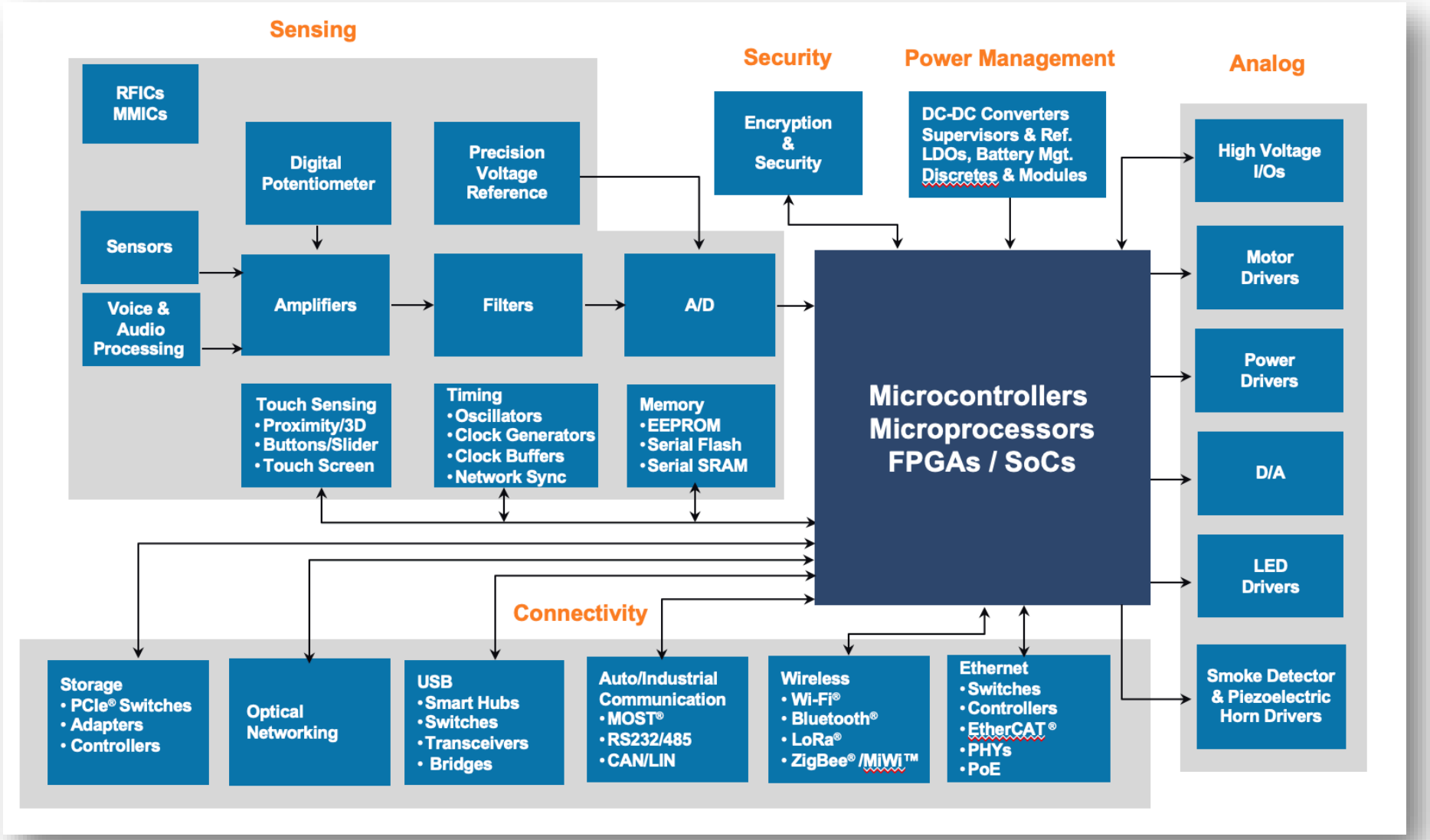
PolarFire SoC has a 6K CoreMark head start!



MICROCHIP

The Most Complete RISC-V Development Ecosystem

Part of Microchip's Commitment to Total System Design



Devices

Firmware

Software

Tools

Support

MICROCHIP

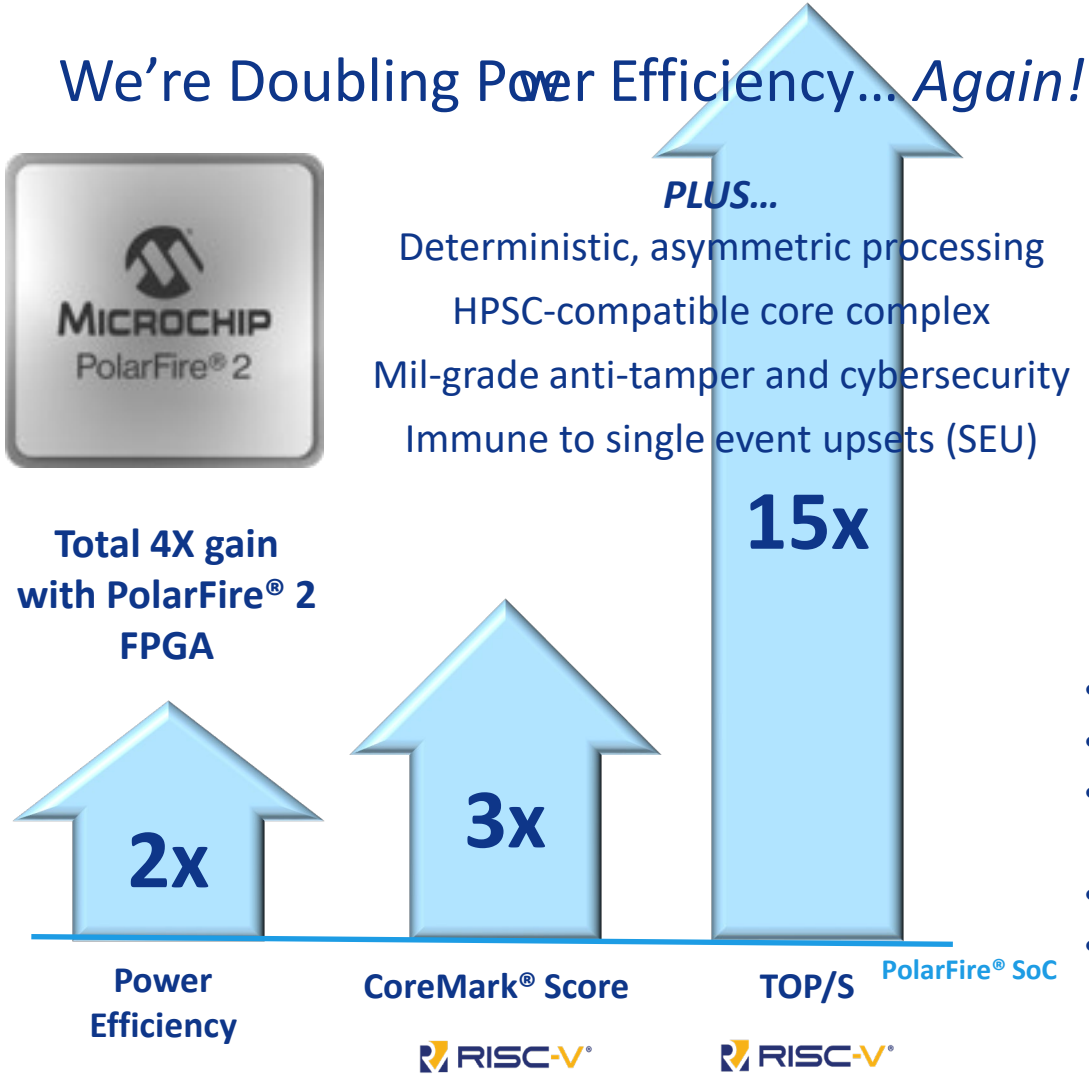
What's around the corner?

Next: The Second Generation of PolarFire® FPGAs

We're Doubling Power Efficiency… *Again!*

MICROCHIP PolarFire® 2

Total 4X gain with PolarFire® 2 FPGA



PLUS…

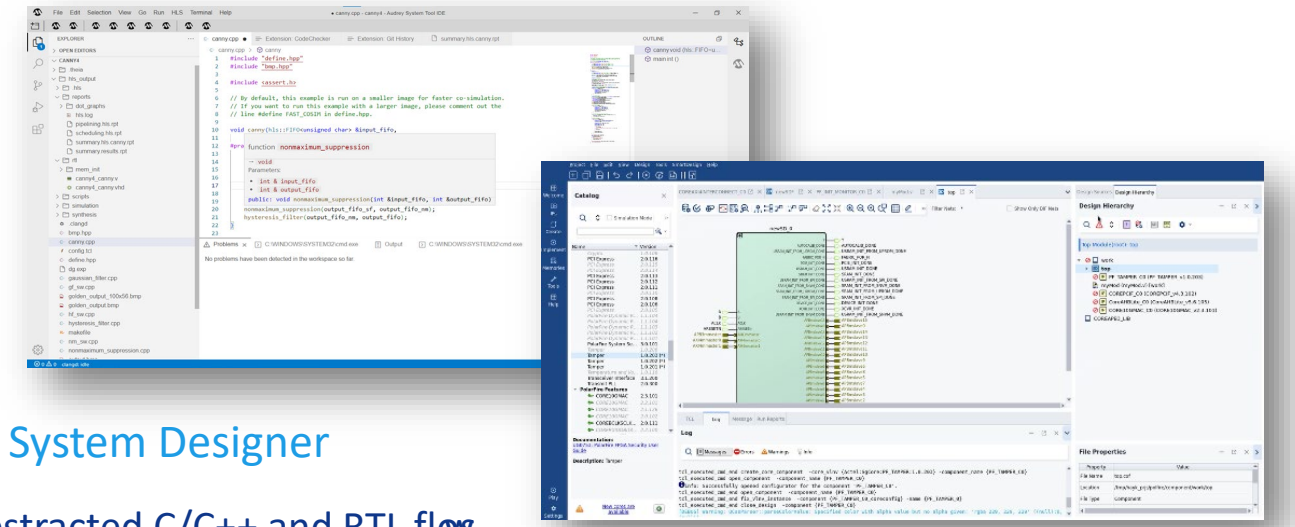
Deterministic, asymmetric processing

HPSC-compatible core complex

Mil-grade anti-tamper and cybersecurity

Immune to single event upsets (SEU)

System-Level Design Gets Its Own Suite



System Designer

- Abstracted C/C++ and RTL flows
- Complete SoC creation with C/C++
- Hardware/software partitioning and co-design
- Full SoC debug to speed bring-up
- Pre-silicon software development

FPGA Designer

- Modern and intuitive UI
- Fast timing closure
- Adaptive design flows
- Better IP handling and delivery
- Faster simulation and expanded debug

MICROCHIP

Tuned for Power-Hungry 100G Edge Technologies

Multiple Concurrent CNNs
Multifold CoreMark Performance Increase

Immune to Single Event Upsets
Resists Next Generation Threats

Up to 8K Video

100G Processing
64x64 MIMO Radio
32G Multiprotocol Transceivers

MICROCHIP

What's around the next corner?

HPSC is Critical for NASA's Strategic Framework

HPSC-based Autonomy is the Key

Go

Rapid and efficient space transportation

Rapid, low cost robotic payloads: Moon, Mars and beyond.
Next generation computing and communications in space.

Land

Expanded access to diverse surface destinations

Precision landings. Avoid unknown local hazards.
Ability to handle unknown environments and situations.

Live

Sustainable Living and Working Farther from Earth

Human and Robotic Lunar Missions > 28 days.
Human Mars Missions > 800 days.

Explore

Transformative missions and discoveries

Robotic systems augmenting human operation.
Remote servicing, assembly and manufacturing.

HPSC Architecture Highlights

Advanced
FinFET Process

Machine Learning

Multi-Core
RISC-V
Space Compute

Time Sensitive
Ethernet
Networking

PCIe

Real-time
Processing

Deterministic
Latency

SWaP Optimized Heterogenous
Fault Tolerant
Architecture

Vector Engines

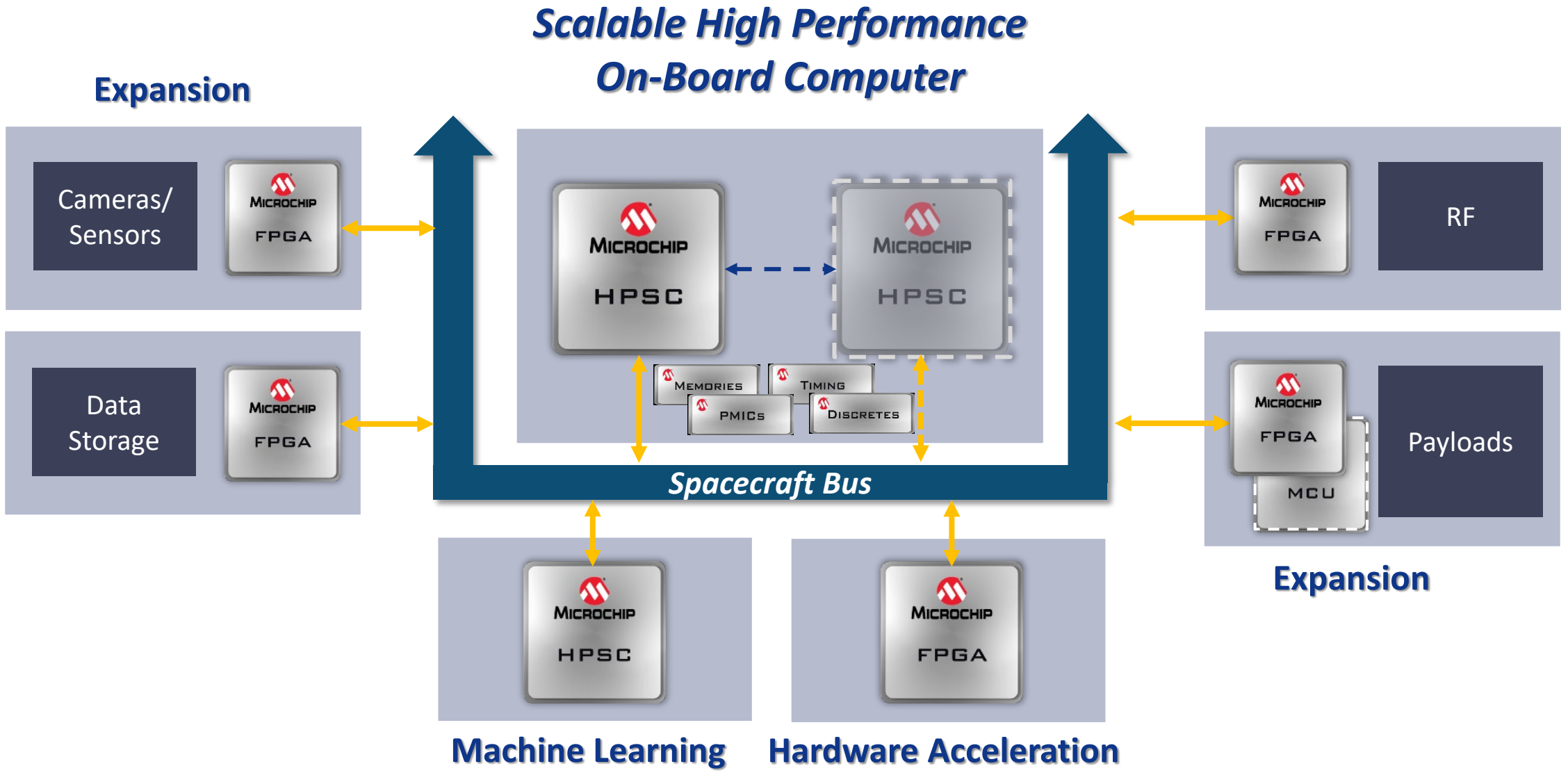
Secure
Enclave

Co-processor
Interfaces

Extensible Power
& Performance

MICROCHIP

Extensible Space System Solution



Enabling HPSC-Based SBC Ecosystem

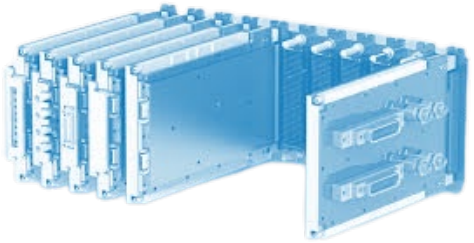
Single Board Computer (SBC) Partners To Fully Address Customer Development Needs

Open/Interoperable

U.S. SpaceVPX™

DoD SOSA™ Sensor Open Systems Architecture

ESA PICMG® cPCI Serial Space™



Build vs. Buy

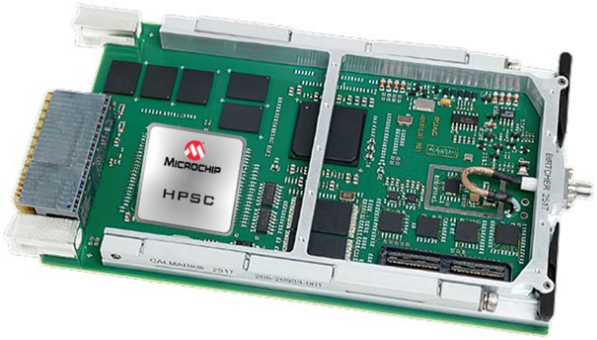
NASA

U.S. Department of Defense

esa

NASA to only buy **SpaceVPX** SBCs, **DoD** will buy **SOSA** compliant SBCs, **ESA** transitioning to **CompactPCI Serial, Defense Primes** increasingly buy off-the-shelf SBCs.

SBC Partners



Target to work with **partners** to develop **flight-capable HPSC-based SBCs** in various form factors for different end-markets (Space, ESA, Defense, etc.)

MICROCHIP

HPSC Timeline

RISC-V Take Aways

- RISC-V breathes new life into the semiconductor industry
- CPU Architectural licenses are free
- Leading to more diverse compute solutions for OEMs
- Microchip has been a pioneer in this effort
- The future is very bright for RISC-V and space-based computing.

Thank You