AMD Xilinx Radiation Tolerant FPGAs

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Agenda

- AMD acquisition of Xilinx
- XQR Kintex™ UltraScale™ update
- XQR Versal™ overview and update
  - Architectural features
  - Product portfolio
  - Packaging, qualification and screening
  - Power and thermal considerations
  - Radiation
  - Ecosystem partners
- Questions and answers

AMD Acquisition

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AMD Acquired Xilinx February 2022

- The combination of AMD and Xilinx is a leading high performance computing company
- Aerospace & Defense customers can now leverage a combined portfolio of CPUs, GPUs, FPGAs, Adaptive SoCs and Unified SW Platforms
  - World-class 2.5 / 3D die integration and packaging technology
  - Commercially-proven chiplet & C2C interconnect technology
  - Leading-edge AI engines and domain specific architectures
- Xilinx becomes part of the AMD Adaptive Embedded Computing Group (AECG)
- AECG continues the 30+ year legacy of Xilinx in support for the Aerospace & Defense industry with the supply of state-of-the-art microelectronics

AMD AECG Leadership Team
Adaptive Embedded Computing Group

Victor Peng
President, Adaptive and Embedded Computing Group

Salil Raje
SVP and General Manager, Data Center and Communications Group

Mark Wadlington
SVP and General Manager, Core Markets Group

Vamsi Boppana
SVP, Central Products Group

Ivo Bolsens
SVP and Chief Technology Officer

Vincent Tong
SVP, Global Operations and Quality, Adaptive and Embedded Computing Group

Rajneesh Gaur
CVP and General Manager, Embedded Solutions

Aman Singh
Sr Director, Chief of Staff

XQR Kintex™ UltraScale™ Update

XQR Kintex™ UltraScale™ Qualification - *Completed!*

- The XQRKU060 qualification was completed on schedule
- 3 qualification lots tested and meet requirements per MIL-PRF-38535
- Qualification report available
  - Group A (TM5005)
  - Group B (MIL-STD-883)
  - Group C (TM1005 – 2000 Hours) + Group C (TM1005 – **Aug. 2021 Surpassed 10K hours** for New Product Introduction)
  - HTS (TM 1008); HAST (JESD22-A110); Temp Cycle (TM1010 Cond C)
  - Group D (Sub Groups 1,3,4,5)
  - Group E (TM 1019, Sub Group2)
- QML-Y Certification Plans for XQRKU060
  - AMD to pursue certification once DLA COVID-19 restrictions are over
  - 9-12 month effort once initiated
- Additional Reliability Monitors
  - Board Level Reliability completed
  - 1000 Temp cycles (-55°C to 100°C, 10°C/min, 15min dwell time) PASSED

XQRKU060 Xilinx Class B, Class Y **PASSED** Qualification,
Shipments since *Sept 2020*

XQR Versal™ ACAP for Space 2.0 Applications

AMD AECG – A Leading Provider for Aerospace and Defense

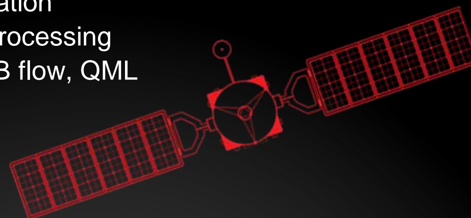
30+ Years Heritage

Commercial & Military Avionics

- DO-254 and DO-178
- Certifiable Solutions
- SEU Mitigation
- Advanced Tool Flows

Space & MilSatCom

- Space-grade Portfolio
- SEU Mitigation
- Payload Processing
- Y, V, and B flow, QML
- TMRTool



Missiles & Munitions

- Defense-grade Portfolio
- Anti-Tamper IP
- Bare Die

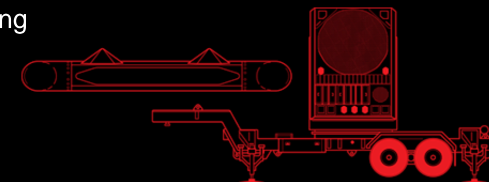
Intelligence, Surveillance & Reconnaissance (ISR)

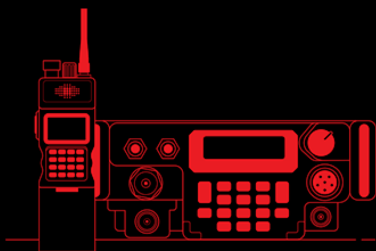
- Signal Processing
- Vivado™, Vitis™
- Connectivity
- Anti-Tamper IP

AMD Covers *Ground-Air-Space* Applications

Electronic Warfare (EW)

- Signal Processing
- Vivado / Vitis
- Connectivity
- Anti-Tamper IP



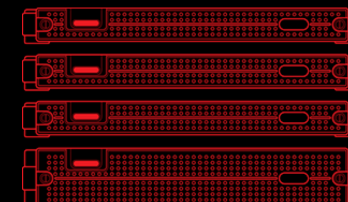


MILCOM & Public Safety

- Signal Processing
- Low Power Solutions
- Waveform IP & Analysis
- LTE UE with P2P
- Secure Information Assurance
- Anti-Tamper IP

Homeland Security

- Vivado / Vitis
- SEU Mitigation
- Partial Reconfiguration



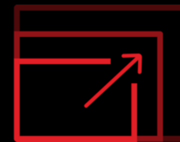
Space Industry Market Challenges & Requirements

- Downlink Bandwidth is limited
- Fast time to market
  - Platform Concept for reuse on multiple missions

- Low Latency and High Bandwidth
  - Seamless and reliable connectivity for broadband communications

- Machine Learning in orbit

- Need for capability to process on board a satellite vs ground station
  - Reduce Development Time to launch
  - Process hundreds of Gbps data streams in real time



- Flexible System Architecture
  - Change algorithms “on the fly”
- Reliable components for long mission life, extreme environments

- SWaP (Size, Weight and Power) Tradeoffs

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Target Markets and Applications

Communications Constellations

- Broadband Internet
- High Speed Networks

Earth Observation Payloads

- Hyperspectral Cameras
- Synthetic Aperture Radar

Navigation/ Technology

- GPS
- Entry/Descent/ Landing
- Instruments
- Avionics

Signal Processing, HW/SW Reconfigurable, Robust Package,Space Grade Tested, On Orbit Flexibility

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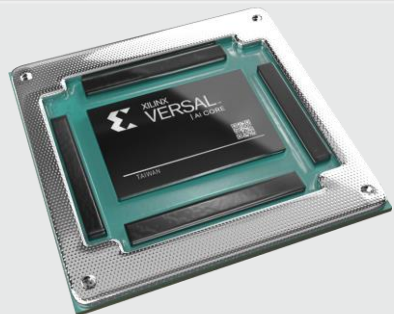
XQR Versal™ ACAP for Space 2.0 Applications

First 7nm Adaptable SoC for Space Applications

- AI Core and AI Edge family members with Scalar, Intelligent and Adaptable Engines (ARM® CPUs, AI Engines & Prog. Logic)
- Innovative silicon design for SEU mitigation (> 50 patents)
- True on-orbit reconfiguration with unlimited programming cycles



Ruggedized Organic BGA

- AI Core 45mm x 45mm, AI Edge TBD
- Lidless with stiffener ring for added thermal mitigation capabilities
- Footprint compatible with commercial packages

Production Space Test Flow

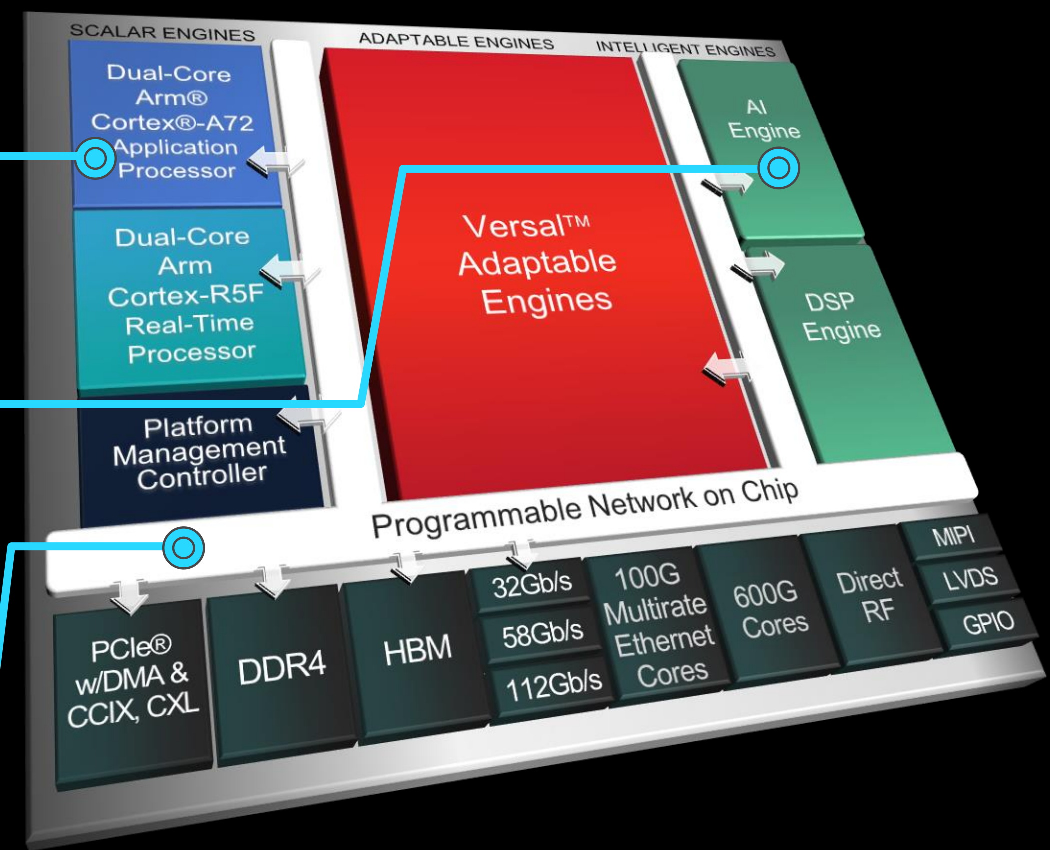
- Screened to MIL-PRF-38535 Class B, modified for organic packages
- Designed for Space 2.0 Applications
- 5 to 7 Year Mission Duration

Novel Features for Space in Versal™ ACAPs

Processor System

AI Engines

Network on Chip



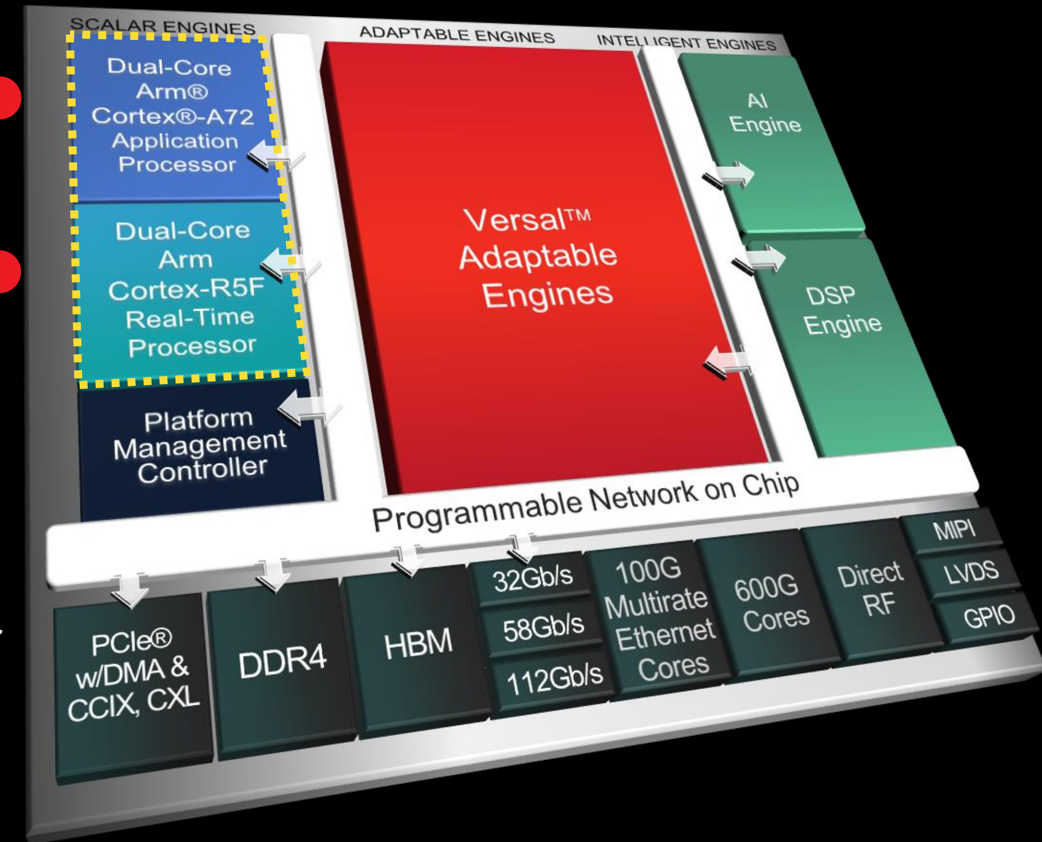
ARM® Cortex® Processors

APU

- Dual-core Arm Cortex-A72 application processor

RPU

- Dual-core Arm Cortex-R5F real-time processor



Processing system (PS) is part of a group of architectural elements that include:

- Platform management controller (PMC) - New central device manager
- Processing system manager (PSM) - PS-specific device manager
- Boot peripherals located in the PMC and shared with the PS
- Shared multiplexed I/O (MIO) pins between the PMC and PS
- CCIX and PCIe® module (also known as the CPM)
- Network on chip (NoC)
- Tightly coupled, integrated memory controllers capable of operating independently

PS supports the low-power and full-power domains (LPD and FPD)

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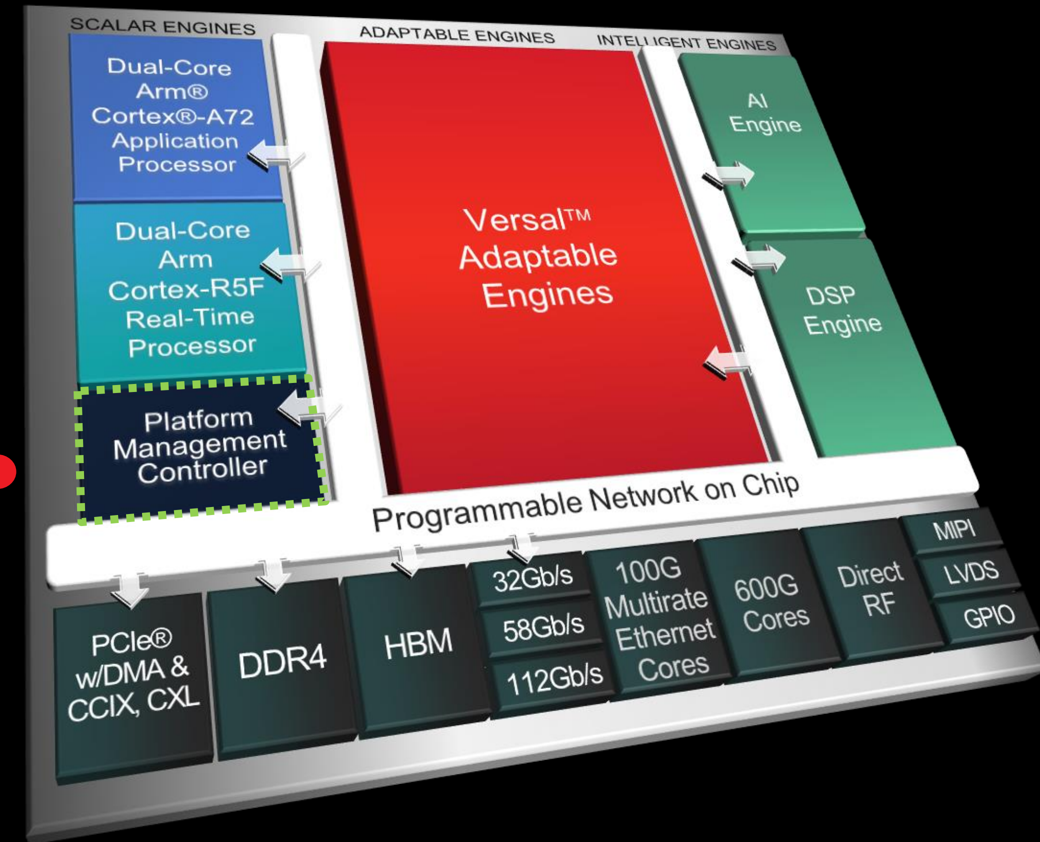
PMC – Platform Management Controller

PMC

- Two hardwired triple-redundant MicroBlaze™ processors

- Central to all Versal™ devices
- Power domain is independent from other processors and logic fabric
- Contains the boot peripherals for initialization that become available to the PS after boot
- Handles power management and reset for all blocks, error management, security, configuration, and analog measurements
- Hosts XilSEM – Xilinx Soft Error Manager
  - Runs as C code on PMC
  - PMC is a critical part of SEU mitigation infrastructure



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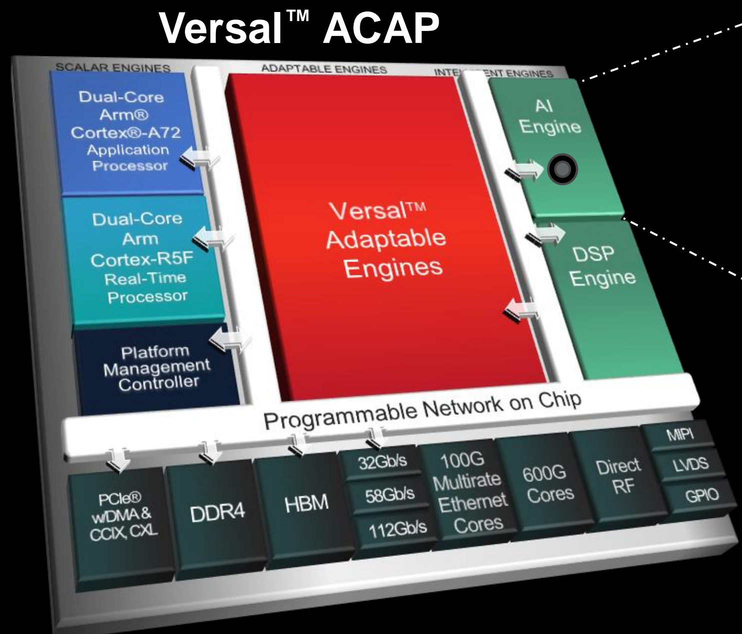
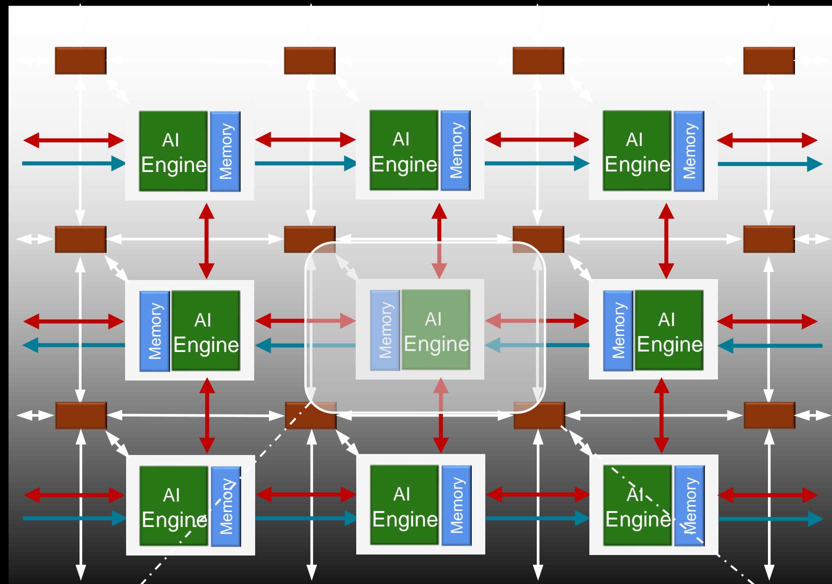
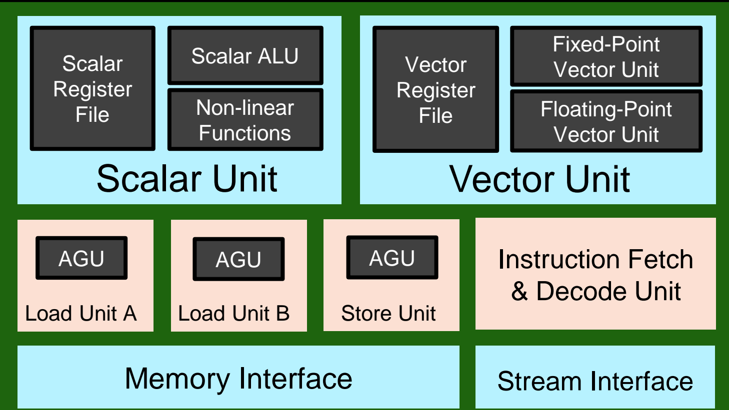
AI Engine

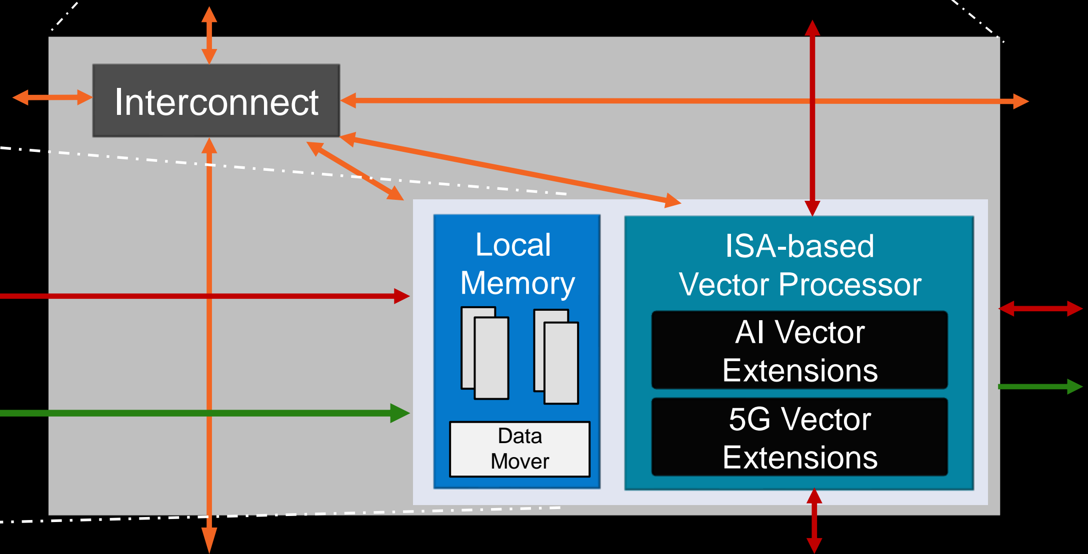




AI Engine Array



AI Engine



Memory Interface
Stream Interface
Cascade Interface

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AI Engine Summary

- The AI Engine consists of
  - 512-bit SIMD (single instruction, multiple data) vector units, both fixed-point and floating-point
  - 16 KB program memory
  - 32-bit scalar RISC processor
  - 256-bit load (x2) and store units with individual address generation units (AGUs)

- The AI Engine supports multiple levels of parallelism
  - Instruction-level parallelism (ILP)
  - Data-level parallelism (DLP)

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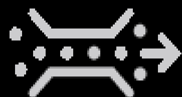
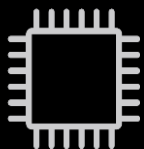
Benefits of a Network on Chip

It's fast!
High bandwidth for huge data movement



NoC <-> DDRMC
DDR interleaving
Bottleneck management



Silicon implementation
- Meets timing
- Low power
- No PL routing resources

Scalar Engines
Adaptable Engines
Intelligent Engines

Arm® Dual-core Cortex-A72
Application Processor

Arm Dual-core Cortex-R5
Real-time Processor

Platform Management Controller

Versal™ Adaptable Engines

Block RAM
UltraRAM
Accelerator RAM

AI Engines

DSP Engines

Huge data in/out quickly

Huge data in/out quickly

Huge data in/out quickly

Huge data in/out quickly

Programmable Network on Chip

PCIe® and CCIX (w/DMA)
DDR
HBM
112G
58G
Multirate Ethernet
600G Cores
MIPI
LVDS
GPIO
Direct RF

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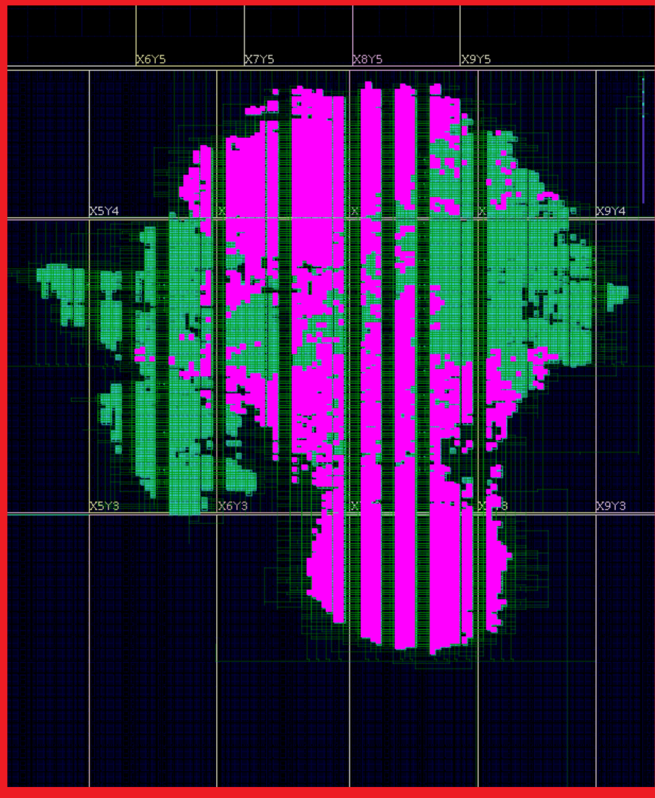
Versal™ ACAP NoC Features and Performance Example

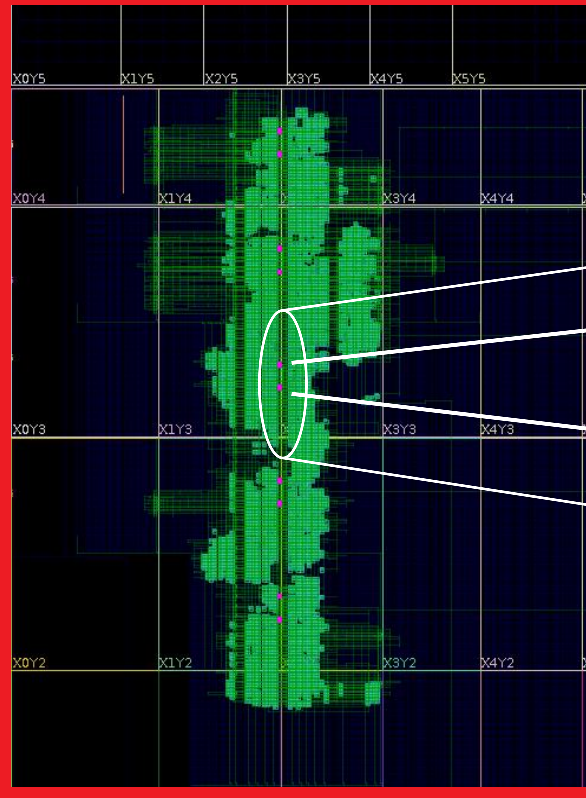
Design without NoC



Total Resources*: 70K LUTs + 70K FFs

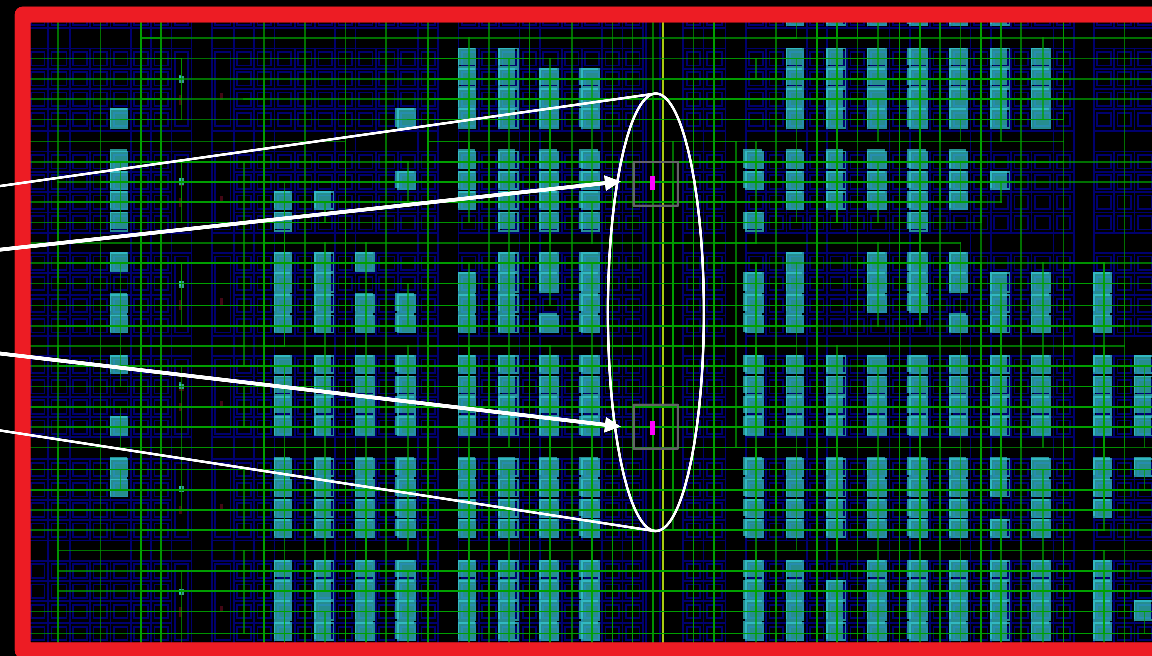
Interconnect*: 37K LUTs + 42K FFs

Design with NoC



Total Resources*: 36K LUTs + 28K FFs

Interconnect*: 0 Resources, NoC Only



Approximately 50% Fewer PL Resources

*AMD internal data

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NoC Summary

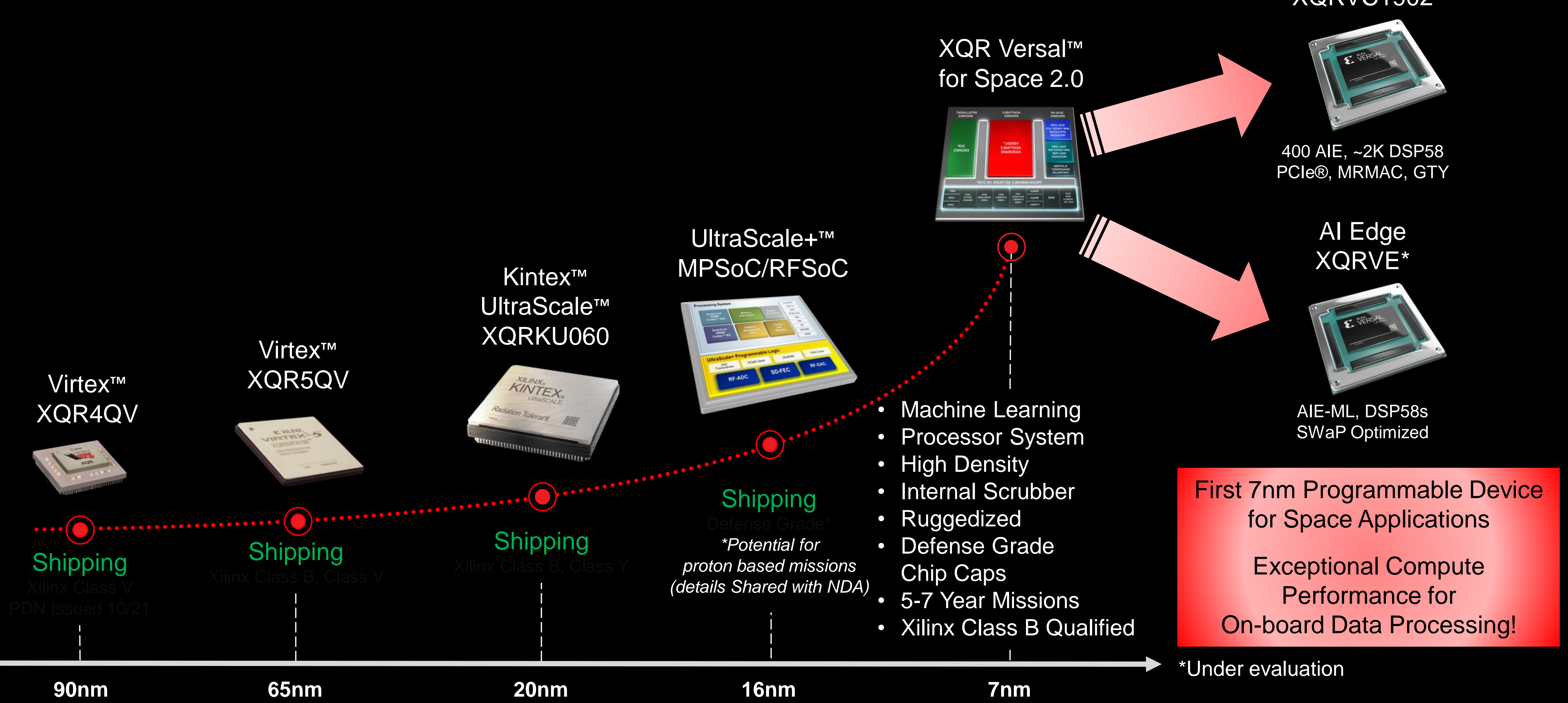
- Network on chip moves data within the device and is also tightly coupled with the DDR memory

- Key NoC components
  - NoC master unit: Brings data into the NoC subsystem
  - NoC slave unit: Takes data out of the NoC subsystem
  - NoC packet switch: Buffers and arbitrates flits
  - NoC routing resources: Vertical and horizontal routes carrying the flits

- Increased system integration
  - Provides high-bandwidth connections among all major blocks within the Versal™ ACAP device
    - Includes tight coupling with the DDR memory controllers

XQR Versal™ Product Portfolio

AMD Space Grade Products



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XQR Versal™ ACAP for Space 2.0 Product Table

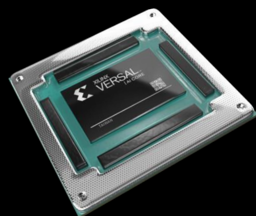
		XQRVC1902-1MSBVSRA2197 (AI Core)
Intelligent Engines	AI Engine Tiles	400 (AIE)
	AI Engine Data Memory (Mb)	100
	AI-ML Shared Memory (Mb)	-
	DSP Engines	1,968
Adaptable Engines	System Logic Cells (K)	1,968
	LUTs	899,840
	NoC Master/NoC Slave Ports	28
	Distributed RAM (Mb)	27
Memory	Total Block RAM (Mb)	34
	UltraRAM (Mb)	130
	Accelerator RAM (Mb)	-
	Total PL Memory (Mb)	191
	DDR Memory Controllers	4
	DDR Bus Width	256
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48KB/32KB L1 Cache w/ECC 1 MB L2 Cache w/ECC
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC
	Memory	256KB On-Chip Memory w/ECC
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2) USB 2.0 (x1); SPI (x2); I2C (x2)
Serial Transceivers	GTx Transceivers	44 GTY (26.5625 Gb/s)
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	1 x Gen4x8, CCIX
	PCI Express	4 x Gen4x8
	Multirate Ethernet MAC	4
	Platform Management Controller	Boot, Security, Safety, Monitoring, High-Speed Debug, SEU Mitigation (XilSEM)
Package	Ruggedized Organic BGA	VSRA2197, 45mm x 45mm, 0.92mm pitch
I/O		648 XPIO, 44 HDIO, 78 MIO, 44 GTY
Radiation Single Event Effects (SEE)	Proton and Heavy-Ion Testing Ongoing in 2023	NO SEL, 100% Correctable SEUs, Ultra-low SEFI

XQRVC1902 B qual completed 6/2022

XQR Versal™ ACAP for Space 2.0 Timeline

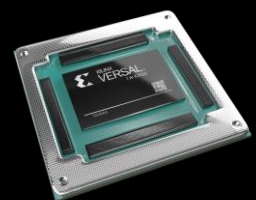
Subject to Change

AI Core



XQRVC1902

AI Edge



XQRVE TBA

* Use XC Equivalent

XQR Versal™ ACAP
Packaging, Qualification and Screening

Paul Lynch
Customer Quality Engineer

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AMD Aerospace and Defense

- AMD/Xilinx has a long history of producing space and organic devices
- We are leveraging this learning to now release class B organic devices
- This has leveraged our silicon experience with space devices - XQR5V, XQRKU060, and space 2.0
- Packaging with organics has demonstrated robustness including flight heritage for LEO
- AMD is now expanding our portfolio formally to offer broader organic options specifically designed for space
  - Class B device based upon commercial device with enhanced screening and applicable MIL-PRF-38535 qualification
  - Class Y device being considered, and would have enhanced materials for extended/more rigorous missions

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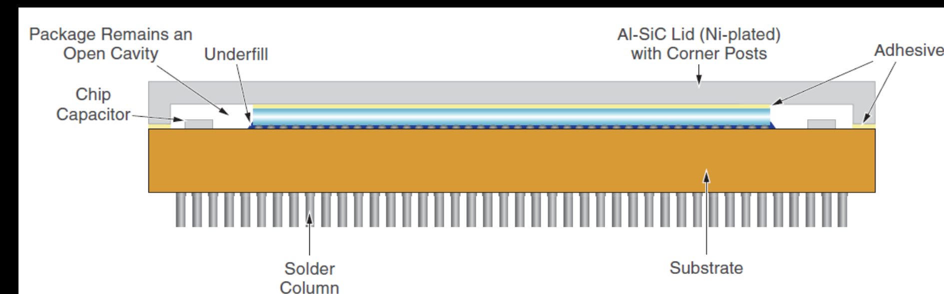
AMD Space Grade Flows

Flow	QML "Class V"	AMD "Class V"	QML "Class Y"	AMD "Class Y"	QML "Class B"	AMD Ceramic "Class B"	AMD Organic "Class B"
Wafer Sort	√	√	√	√	√	√	√
Bumping	N/A	√	N/A	√	N/A	√	√
Assembly (per MIL-STD-883)	√	√	√	√	√	√	Commercial
Bond Pull (Extended Pull Test)	√	N/A for flip chip	√	N/A for flip chip	N/A	N/A	N/A
Die Shear (1unit/lot)	√	√	√	√	√	√	√
Die Visual Inspection	Cond A	Cond A	Cond A	Cond A	Cond B	Cond B	Commercial
Serialization	√	√	√	√	√	√	√
Temperature Cycling (cycles)	10	100	10	100	10	100	10
Constant Acceleration	√	N/A for flip chip	√	N/A for flip chip	√	N/A for flip chip	N/A for flip chip
PIND	√	N/A for flip chip	√	N/A for flip chip	N/A	N/A	N/A
Seal (Fine/Gross Leak Test)	√	N/A	N/A	N/A	√	N/A	N/A
X-Ray and/or SAM	√	√	√	√	N/A	N/A	N/A
Pre Burn-in Electrical Test	@25C	@25C, 125C, -55C	@25C	@25C, 125C, -55C	@25C	@25C, 125C, -55C	@25C, 125C, -55C
Dynamic Burn-in @125C	240 hrs	240 hrs	240 hrs	240 hrs	160 hrs	160 hrs	160 hrs
Post Burn-in Test @25C with Read & Record	√	√	√	√	N/A	N/A	N/A
Static Burn-in (144 hours @125C)	√	√	√	√	N/A	N/A	N/A
Group A Post Burn-in Test @25C with Read & Record	√	√	√	√	√	√	√
Group A Final Test @-55C with Read & Record	√	√	√	√	√	√	√
Group A Final Test @125C with Read & Record	√	√	√	√	√	√	√
Column Attach	√	√	√	√	√	√	N/A (BGA Pkg)
100% QA Electrical @25C	√	√	√	√	√	√	N/A
Visual Inspection	√	√	√	√	√	√	√
Group B Lot Specific	√	√	√	√	√	√	√
Group C Sample to 44k device hours	√	√	√	√	√	√	√
Group D	√	√	√	√	√	√	√
Group E Total Ionizing Dose	√	√	√	√	N/A	N/A	N/A
DPA Sample/Ion Milling	N/A	√	N/A	√	N/A	N/A	N/A

- AMD Flows derived from MIL-PRF-38535 for high lead count, flip chip devices
- AMD exceeds the QML requirements in:
  - Temp cycles
  - Pre Burn-in electrical testing
  - DPA with column attach stress

AMD XQR Construction Comparison (Ceramic Devices)

Feature	Attribute	XQR5VFX130-CN1752	XQRKU060-CNA1509
Qualification Level	Class	B and Y	B and Y
Package	Package Type	Ceramic Column Grid Array	
	Body Size	45x45 mm sq.	40x40 mm sq.
	Height	8.29 mm	8.53 mm
	Pitch	1.0 mm	
	Array	42x42	39x39
	Corner Depopulation	3	
C4 Bump	*Supplier*	SPIL	
	C4 Material	Eutectic, 63Sn37Pb	
	Pitch	217 um	180 um
Substrate	*Material*	Ceramic (Alumina)	
	Thickness	4.11 mm	4.35 mm
	Substrate Metal Layers	28 layers	37 layers
	I/O, Vcc, Vss Trace Metallization	Tungsten (W)	
	Via Metallization	Molybdenum (Mo)	
	C4 Pads	E-Less Ni/Au	
	Substrate LGA Pads	E-Less Ni/Au	
Assembly	*Supplier*	Kyocera	
	Chip Capacitors	Mil screened	
	Heatspreader Design	4 corner	
	Heatspreader Material	Ni plated AlSiC	
	Underfill	Underfill A	Underfill B
	Thermal Interface Material (TIM)	TIM A	
Column/BGA Ball	*Supplier*	6 Sigma	
	Material	80Pb/20Sn	
	Height	2.20 mm	
	Diameter	0.51 mm	



- Almost identical BOM used for both older ceramic packages
  - The material set was fixed with the release of the XQR5VFX130 device in 2011
- This BOM has proven itself to be very reliable, but the ceramic substrate has limitations with regard to routing density and performance

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AMD XQR Construction Comparison (Ceramic vs. Organic)

Feature	Attribute	XQRKU060-CNA1509	XQRVC1902-VSRA2197
Qualification Level	Class	B and Y	B
Package	Package Type	Ceramic Column Grid Array	Organic Ball Grid Array
	Body Size	40x40 mm sq.	45x45mm
	Height	8.53 mm	3.8mm
	Pitch	1.0 mm	0.92mm
	Array	39x39	47x47
	Corner Depopulation	3	
C4 Bump	*Supplier*	SPIL	
	C4 Material	Eutectic, 63Sn37Pb	Copper pillar with SnAg solder
	Pitch	180 um	130um
Substrate	*Material*	Ceramic (Alumina)	Organic
	Thickness	4.35 mm	1.45mm
	Substrate Metal Layers	37 layers	16 layers
	I/O, Vcc, Vss Trace Metallization	Tungsten (W)	Copper
	Via Metallization	Molybdenum (Mo)	Copper
	C4 Pads	E-Less Ni/Au	Sn/Cu SOP
	Substrate LGA Pads	E-Less Ni/Au	SAC305 SOP
Assembly	*Supplier*	Kyocera	SPIL
	Chip Capacitors	Mil screened	Commercial
	Heatspreader Design	4 corner	Stiffener
	Heatspreader Material	Ni plated AlSiC	Stainless Steel
	Underfill	Underfill B	
	Thermal Interface Material (TIM)	TIM A	
Column/BGA Ball	*Supplier*	6 Sigma	SPIL
	Material	80Pb/20Sn	63Sn/37Pb
	Height	2.20 mm	0.5mm
	Diameter	0.51 mm	0.64mm

- Organic substrate has higher density routing to allow more complex devices
  - Allows high speed performance
- Organic substrate is lighter and thinner than ceramic substrates
- Organic substrate is aligned with future device enhancements and stacked silicon packaging
- BGA format allows for lower overall package height than column grid array
  - Still Sn/Pb compatible with existing board assembly and addresses whisker concerns

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AMD A&D Qualification

- Industry and military requirements differ by intended product

Stress Test	MIL-STD-883 JEDEC reference	Conditions	XC Commercial	XQR Class B	XQR Class Y
Prod. Burn-in	TM 1015	Tj = 125°C Vccmax		Dynamic: 160 hrs.	Dynamic: 240 hrs., Static: 144 hrs.
Group A	TM 5005	Functional, AC and DC Parameters	Test at 110°C	Test at -55°C, 25°C and 125°C	Test at -55°C, 25°C and 125°C
Group B	Mil Std 883	Organic: Commercial Assembly Monitors Ceramic: Mil Std Assembly Monitors	Commercial monitors	Commercial or Mil Std 883	Mil Std 883
Group C	TM 1005 JESD22-A108	Tj = 125°C, Vccmax	1000 hrs, 3 lots, 135 units total	1000 hrs, 3 lots, 135 units total	1000 hrs, 2 lots, 90 units total 4000 hrs, 1 lot, 45 units total
HTS	TM 1008 JESD22-A103	Ta = 150°C	1000 hrs, 3 lots, 75 units total	1000 hrs, 3 lots, 75 units total	1000 hrs, 3 lots, 75 units total
THB or HAST	JESD22-A101 JESD22-A110	Organic: THB 85°C / 85%RH, Vccmax Ceramic: HAST 130°C / 85%RH, Vccmax	THB - 1000 hrs, 3 lots, 75 units total	THB - 1000 hrs or HAST - 500 hrs 3 lots, 75 units total	HAST - 500 hrs 3 lots, 75 units total
Temp Cycle	TM 1010 JESD22-A104	Organic: Cond. B: -55°C / 125°C Ceramic: Cond. C: -65°C / 150°C	1000 cyc, Condition B 3 lots, 75 units total	1000 cyc, Cond. B or C 3 lots, 75 units total	1000 cyc, Cond. C 3 lots, 75 units total
Group D	TM 5005	Sub-Groups 1,3,4,5		15 units / subgroup	15 units / subgroup
Group E	TID: TM1019	> 100krads, Cond. A			5 units

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AMD Reliability Qualification for Commercial Grade Versal™

- Versal Organic Class B qualification was built upon the previously completed commercial qualification

- AMD Versal Commercial Qualification Results
  - Due to similarity in package and device design and fabrication, commercial reliability data does give some indication on XQR reliability

Test	Stress Conditions	Test Vehicles	Lot Quantity	Sample Size	Number of Failures	Cumulative Device Hours/ Cycles
High Temperature Operating Life	T_J = 125°C, > V_{CCMAX} V_{CC_CORE} = 0.938V	XCVC1902-VSVA2197	8	291	0	291000
		XCVP1202-VSVA2785	2	96	0	96,000
High Temperature Storage (1)	T_A = 150°C	XCVC1902-VSVA2197	6	150	0	150,000
Temperature Cycling (1)	Cond. B (-55°C / 125°C)	XCVM1802-VFVC1760	3	75	0	300000
		XCVC1902-VSVA2197	8	150	0	150,000
		XCVC1902-VSVD1760	3	75	0	75,000
		XCVC1702-VSVA1596	6	96	0	96,000
		XCVM1402-NBVB1024	6	82	0	82,000
		XCVM1402-NSVF1396	4	58	0	58,000
		XCVP1202-VSVA2785	6	136	0	136,000
Temperature Humidity Biased Test (1)	85°C, 85% RH biased	XCVC1902-VSVA2197	6	150	0	150,000

(1) Units submitted to MSL-4 preconditioning prior to stressing

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XQR Versal™ ACAP for Space 2.0 Qualification & Screening

- Xilinx Class B qualification completed
  - Derived from MIL-PRF-38535
  - Groups A – D
  - Burn-in
  - High-temp storage and operating life
  - Temp cycling
- All devices will be screened to Xilinx Class B for organic packages
  - Derived from MIL-PRF-38535
  - Offered for mission duration up to 7 years
- For complete qualification details & results, please contact Xilinx Customer Quality team

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AMD Reliability Qualification for Versal™ XQR (Class B)

- AMD has successfully completed our Class B qualification for the Versal XQRVC1902 device

Stress Test	MIL-STD-883 JEDEC reference	Conditions	Duration / Sample Size	Results
Prod. Burn-in	TM 1015	Dynamic, Tj = 125°C Vccmax	160 hrs.	Passed
Group A	TM 5005	Functional, AC and DC Parameters Test at -55°C, 25°C and 125°C	Test at -55°C, 25°C and 125°C	Passed
Group B	Various JEDEC	Assembly Monitors	✓	Passed
Group C	TM 1005	Tj = 125°C, Vccmax	1000 hours 3 lot, 135 units total	Passed
HTS[1]	TM 1008	Ta = 150°C	1000 hours 3 lots, 75 units total	Passed
THB[1]	JESD22-A101	85°C / 85% RH, Vccmax	1000 hours 3 lots, 75 units total	Passed
Temp Cycle[1]	TM 1010	B: -55°C / 125°C	1000 cycles 3 lots, 75 units total	Passed
Group D[1]	TM 5005	Sub-Groups 1,3,4,5	3 lots, 15 units / subgroup	Passed

(1) Units submitted to MSL-4 preconditioning prior to stressing

Note: 4000 hour Group C Qualification Versal™ family data required for meeting QML class Y flight requirements (under class S) pending completion

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AMD Aerospace and Defense

- The release of AMD Versal™ ACAP for Space 2.0, organic based XQRVC1902 device is the next step for AMD to support space customers
- Silicon and organic packaging has demonstrated the necessary reliability to enable the use of high-performance devices in a lighter and smaller package
- AMD Class B qualified and screened units give customers added risk mitigation over other organic devices

Power and Thermal Considerations

Ken O’Neill
Space Systems Architect

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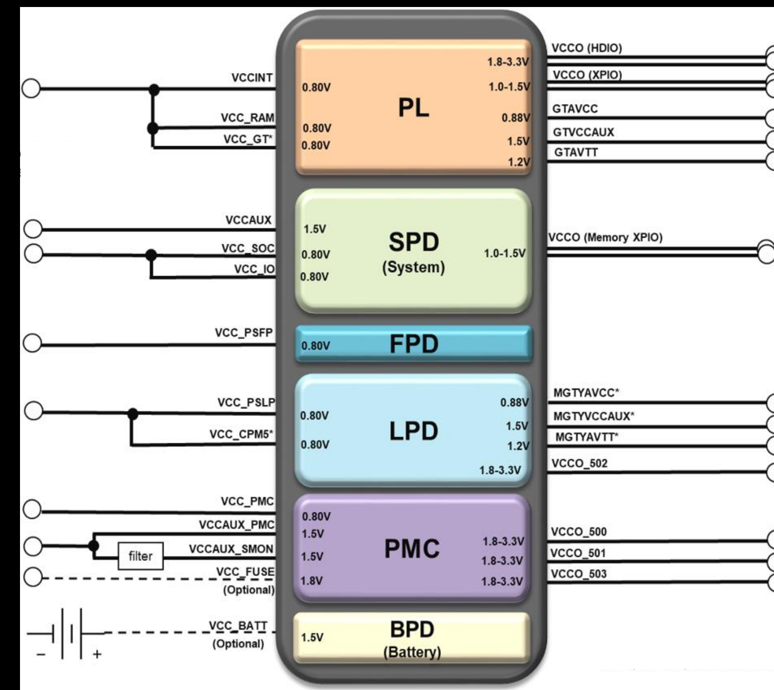
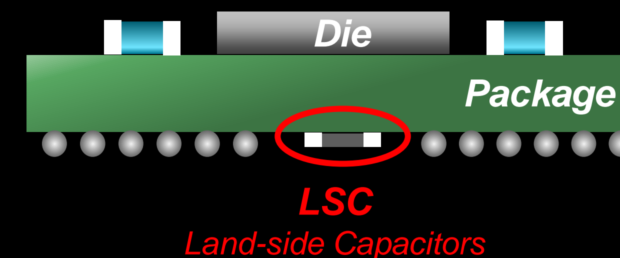
XQR Versal™ ACAP Power

- Power Distribution Network (PDN)
  - Land-side capacitors (LSC): short distance to die; low package induction
  - Optimal mix of SMT, LSC and on-die caps helps ensure noise mitigation across wide frequency range
- Xilinx Power Design Manager (PDM) – available now
  - Stand-alone power estimator based on Java™
  - Enhanced stability, user interface, IP wizards, XDC constraints
- Power Delivery
  - Strategic partnerships for optimized, reliable, radiation tolerant power delivery
  - Monitoring, protections and flexible features to reduce BOM count and improve performance
- Power and Thermal Dissipation go hand-in-hand
  - Greater power density on Versal demands proper thermal mitigation
  - Must do complete thermal simulation
    - Siemens Simcenter Flowtherm
    - Ansys® IcePak
  - XQR Versal thermal models will be available on Space Lounge



www.xilinx.com/power



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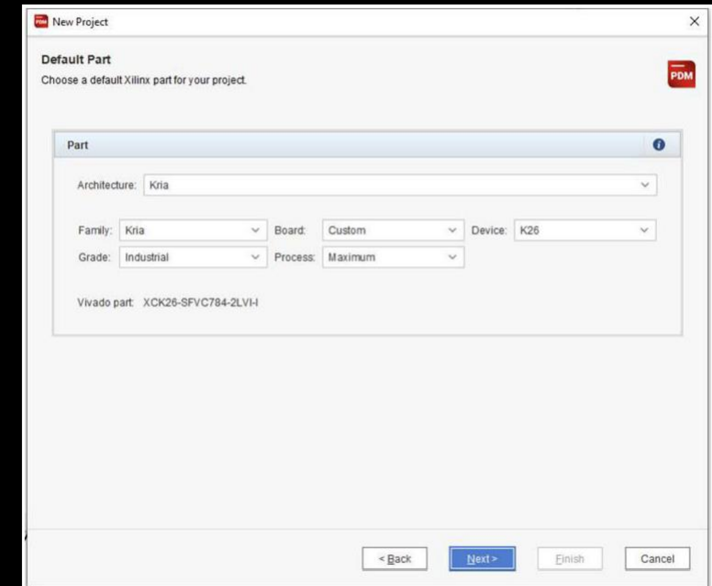
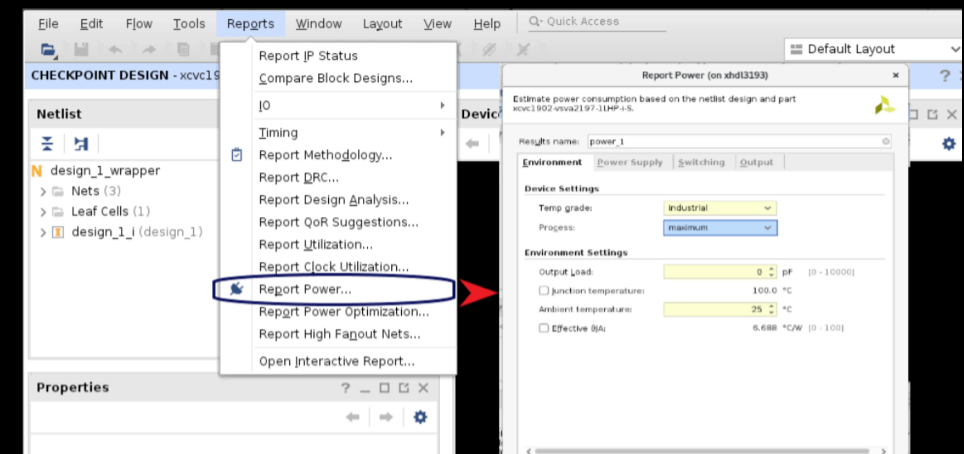
Power Design Manager Supports Two Major Design Flows

- **Manual Estimation Flow**
  - Completely manual entries for power estimation
  - Start with device selection, followed by thermal specifications and configuring the PMC (platform management controller)



- **Import Flow**
  - You can import the XPE file generated from Vivado™ power into PDM while creating a new project
  - You can also use existing estimations from XPE and import into PDM for Versal™ and Kria™ devices



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Addressing Thermal Design Challenges

- AMD highly recommends the use of thermal simulation via CFD software
- AMD has improved the thermal simulation models
  - Predict the thermal performance of the device
  - Quickly iterate through different heat sinks, board placement, airflow directions and countless other scenarios
  - Swiftly and confidently arrive at optimal thermal solution
- Thermal design decisions must take place prior to board layout
- Choosing a material with high thermal conductive properties to help ensure:
  - Complete coverage (>95%)
  - High reliability
- AMD is improving thermal performance by:
  - Refining and improving current processes
  - Introducing and embracing new packaging designs
- Low power screened XQRVC1902
  - 20% static power reduction in I_{CC}
  - Ready for quote now using SCD – append “5355” to ordering code

XQR Versal™ ACAP
Radiation Effects

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Versal™ ACAP Radiation Effects Summary

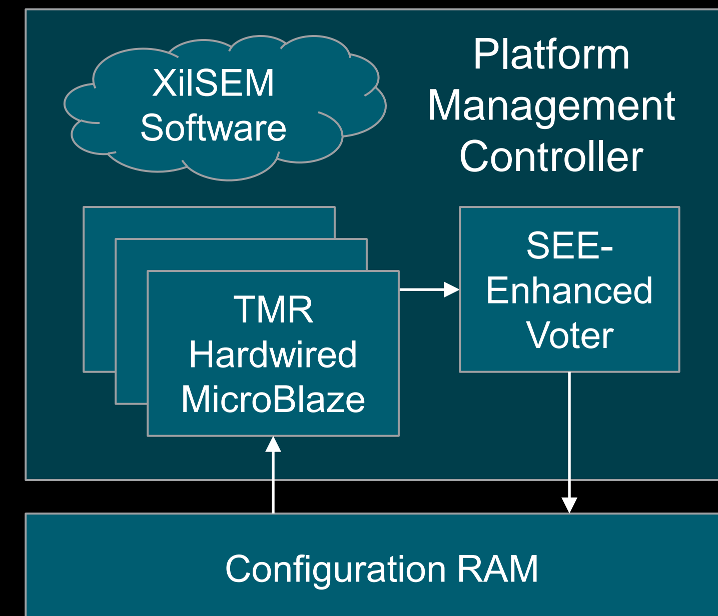
	Protons (2 – 105 MeV) Low Earth Orbit, 500 km, 20° inclination			Heavy-ions (1 - 80 MeV·cm²/mg) Geosynchronous Earth Orbit			TID (gamma)
	CRAM SEU (upset/bit/day)	SEL	SEFI (events/device/year)	CRAM SEU (upset/bit/day)	SEL	SEFI (events/device/year)	
Observed Rates	3.5×10^{-9}	**ZERO** events observed	PS: **1.3** XilSEM: **ZERO** AIE, GT Planned CY2023	6.5×10^{-12}	**ZERO** events observed	PS: 0.16 and XilSEM: 4.9×10^{-3} AIE, GT Planned CY2023	**PASS 120 KRad(Si)**
Comments	Proton energy: 64-400MeV Environment: 1×10^{12} p/cm² at 125°C			Ion Energy: 1-80 MeV·cm²/mg Environment: 1×10^{7} per ion/cm² at 125°C			<18 Krad/min

Estimates based on CREME96 AP8-Max; 500km and GEO models

- DUTs: Versal 7nm VC1902, 20 parts from 5 wafer lots to account for lot-to-lot variation
- ZERO SEL events in maximum V_{CC} and junction temperature conditions at LET up to 80 MeV·cm²/mg
- ZERO uncorrectable Configuration RAM (CRAM) events in LEO and GEO
  - Configuration RAM protected by EDAC and interleaving
- Robust XilSEM internal scrubber SEFI rate may eliminate need for on-board scrubber in space flight
  - Reference Xilinx user guides UG643 and PG352 for XilSEM scrubbing operation and cycle time
- Xilinx has published Versal SEE results at SEE/MAPLD 2022, NSREC 2022, and RADECS 2022
  - Versal 7nm SEL and SEU (terrestrial neutron) paper published & presented at NSREC 2021

XilSEM – CRAM Soft Error Mitigation in XQR Versal™ ACAP

- XQR Versal uses a novel approach to mitigate SEUs in configuration RAM (CRAM)
  - Previous generations of Xilinx FPGAs use SEM (Soft Error Manager) IP residing in the programmable logic fabric
  - XilSEM uses the hardwired TMR MicroBlaze™ processors in the Platform Management Controller (PMC) as a fault-tolerant platform to mitigate upsets in the configuration RAM
  - Approx 30 times greater protection than previous techniques



	Kintex™ UltraScale™ XQRKU060	Versal XQRVC1902	Comments
Configuration Memory (Mb)	193 Mb	363 Mb	VC1902 has ~ 80% more CRAM than KU060
SEFI Rate per Device* (with mitigation, GEO solar min)	1 in 6 years Using SEM	1 in 200 years Using XilSEM	30X Improvement

* AMD internal radiation test data

AMD

AMD Ecosystem Partners

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Ecosystem Partners

- Configuration Memory
  - 3D-Plus
  - Avalanche
  - DDC
  - Infineon
  - Mercury Systems
- Power Distribution
  - Frontgrade (CAES)
  - Infineon
  - Renesas
  - Texas Instruments

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