New Generation of Rad-Hard SoC FPGA

SEFUW 2023

NanoXplore

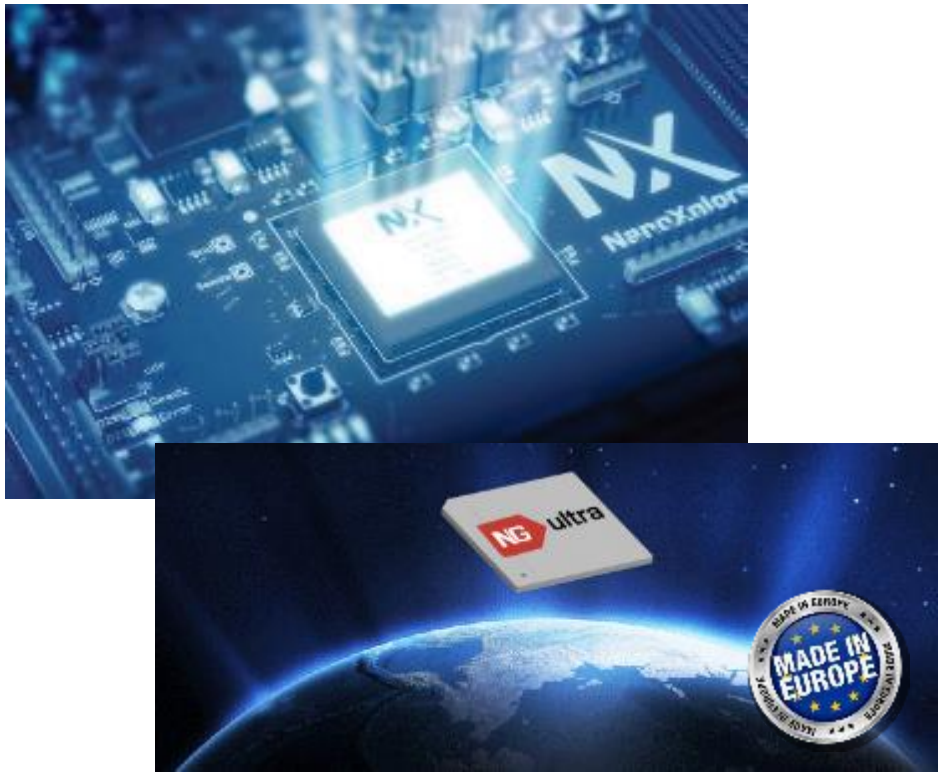
Company Strategy

- The company is focusing on developing SoC FPGA for Hi-Rel markets
- Become quickly a clear leader on Space, Defense and Avionic market
- Focus on key market differentiators like radiation hardening, very high reliability, ITAR free etc
- Slowly moving to more commercial markets with low and mid range FPGA offering
- Fabless strategy based on STM sovereign supply chain
- Full hardware and software in-house development leveraging open source approach when relevant

NX value proposition

FPGA designed for Space

- NX FPGAs are Rad Hard by design -> **no mitigation techniques required**
- All FPGA designed to reach class 1 qualification requirements (ESCC9000 / 9000P)
- Full radiation and aging characterization to meet the most aggressive mission profiles
- Flexible approach to offer same die in various screening flow to address class 1 down to new space requirements
- No export control

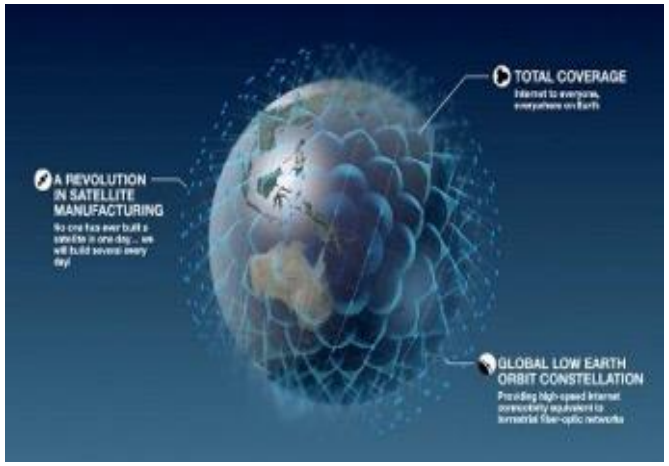


NX value proposition

From Class 1 to « new space »

QA Flows, addressing:

Class 1 Space



New Space

NG-MEDIUM

ESCC9000 qualified (CQ352 & CLGA625)

esa

European Space Agency
Agence spatiale européenne

Certificate of Qualification No. 382

This is to certify that NanoXplore, Sèvres , France has been qualified by ESA for the supply of Integrated Circuits, Silicon, Monolithic, 35KLUT Radiation-Hardened FPGA (NG-Medium) , for use in ESA space programmes, according to ESCC Generic Specification 9000 and associated Detail Specification 9304/010 as recommended by the Space Components Steering Board.

This certificate is valid until August 2024.

Head of the Product Assurance
and Safety Department

Date
31 August 2022

NG-MEDIUM

MP screening flow

- Dedicated screening flow to address low cost mission
- BGA organic package
- Radiation hardening by design
  - Full radiation characterization based on ESCC9000 qualification datapack
- Temp range : -40°c +105°c
- No export control
- Low to High volume
- <1 month leadtime

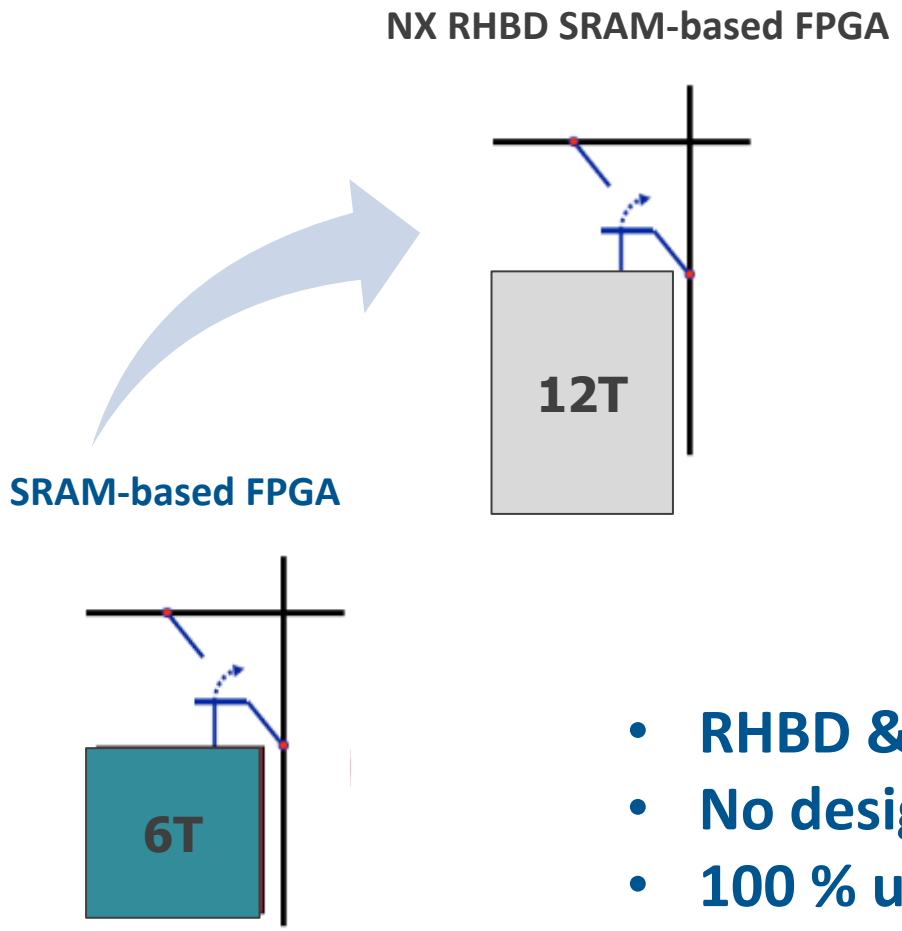
Organic	MP
WLAT	✘
TID / Report	✘
SLDC	✘
T/C	10cy
IVI	2010B SPL
CSAM	✘
Serialization	✘
Burn-In	48h
PDA	✘
Electrical Test	+25°C then -40°C & +105°C
LAT	✘
EVI	100%
CoC	✘

NG-ULTRA

28 nm FDSOI

NG-ULTRA Overview

28 nm Radiation Hardening



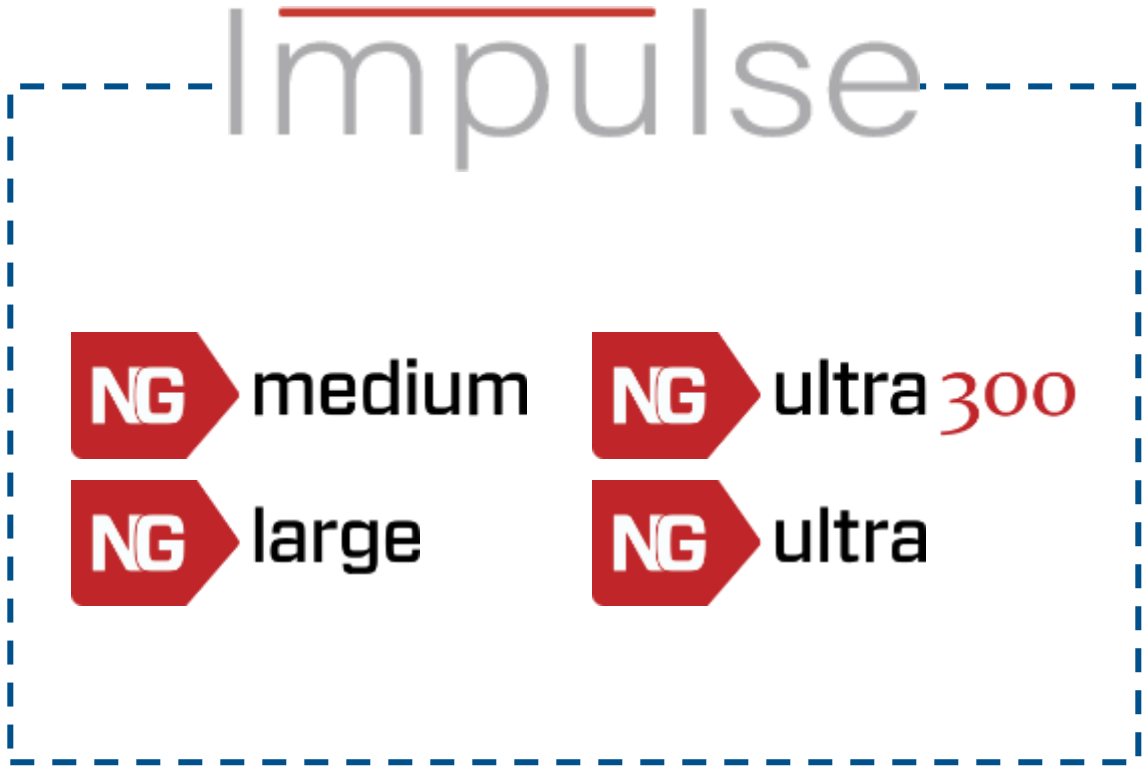
- Rad-hard SoC FPGA manufactured on STM 28nmFDSOI Space process
  - Digital IPs (Standard Cells)
  - Analog Ips
- PL resources are hardened by design (RHBD)
  - SRAM config DICE (Dual Interlocked Cells)
  - DFF, PLL, IO buffer …
- Embedded EDAC for user memory

- **RHBD & SOI = SEE immune**
- **No design mitigation techniques required by the user**
- **100 % usable ressources**

Rad-hard FPGA Offering

Complete rad-hard FPGA offering and associated tools

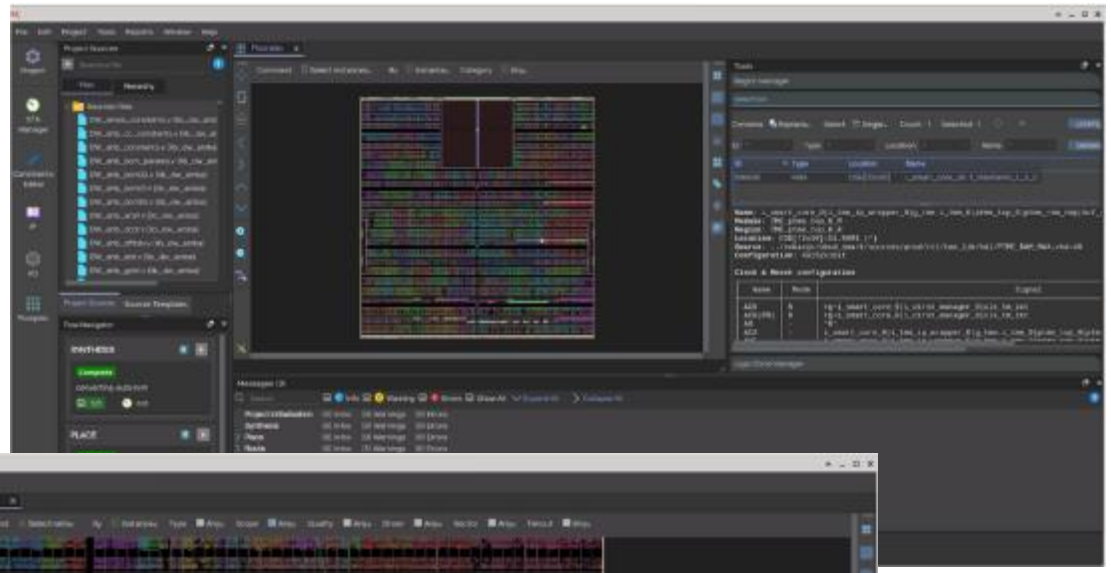
- NX offers a complete rad-hard FPGA offering with all associated tools
- IMPULSE is the programming tools that generate any VHDL into bistream generation
- All required tools ecosystem and IPs to develop simple to complex design

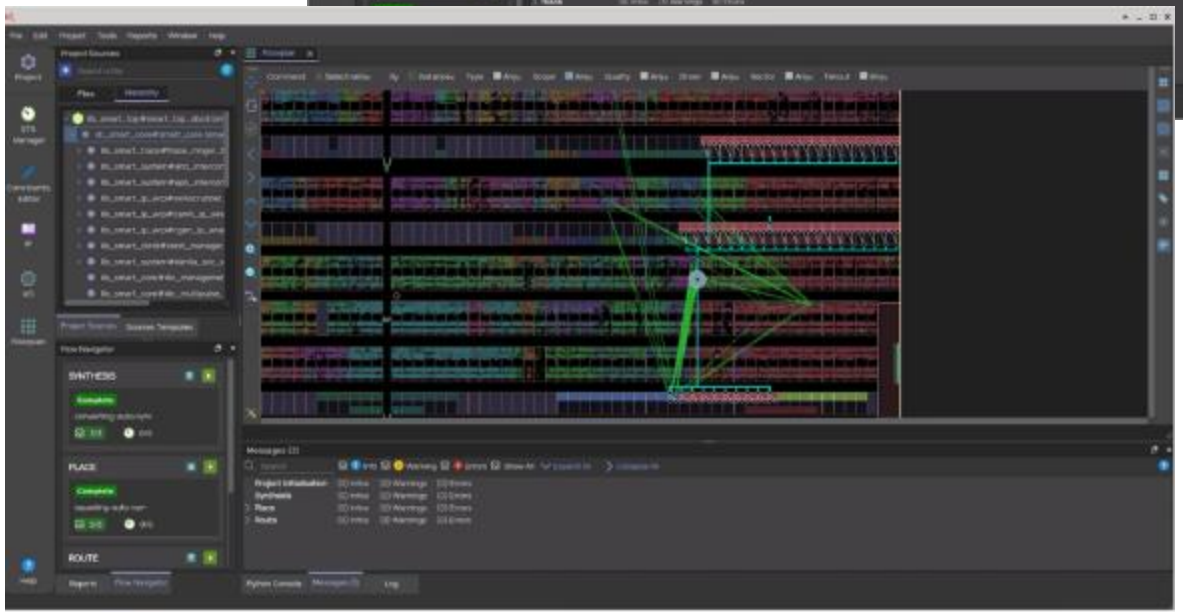


What is Impulse ?

Impulse

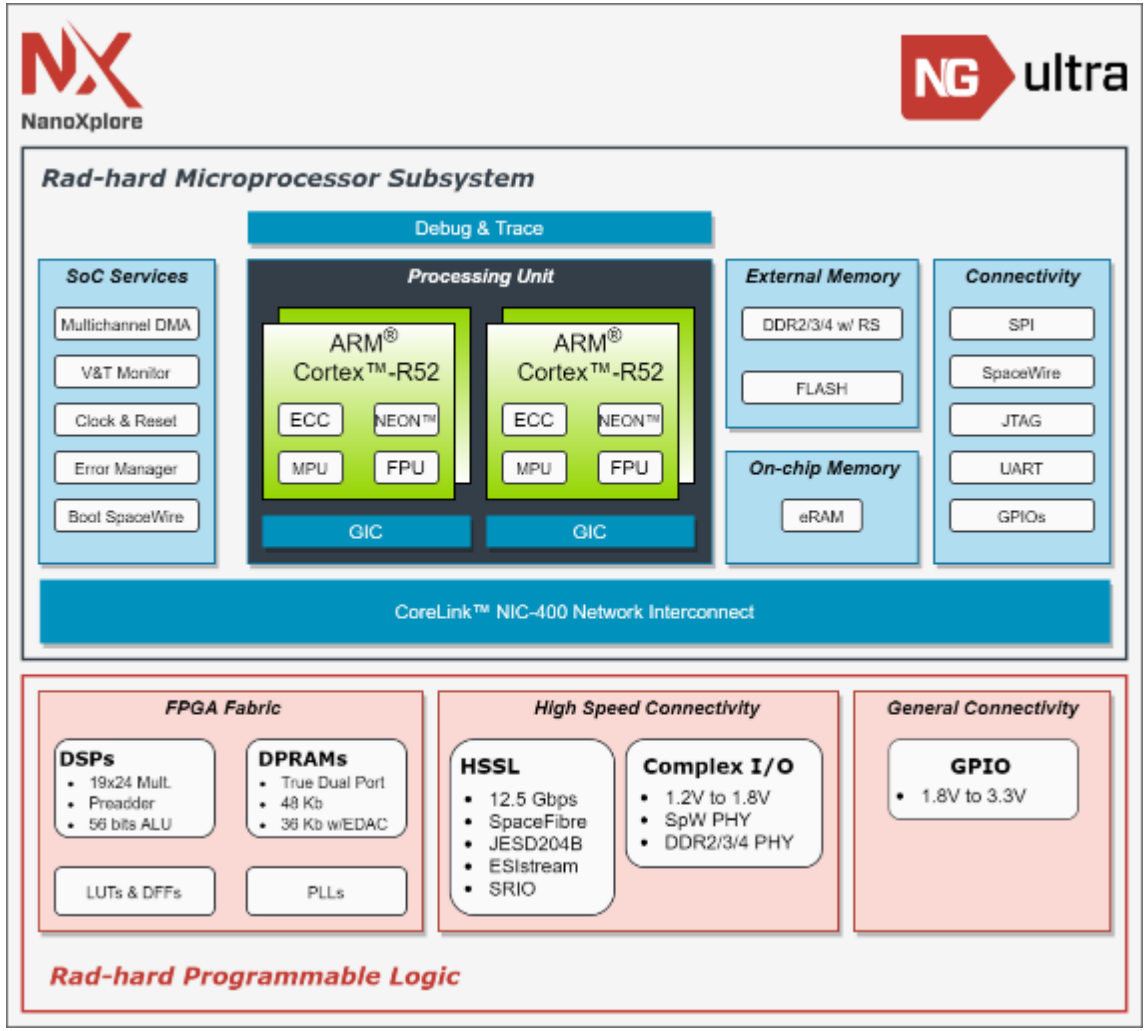
- ✓ More user friendly
- ✓ Better performance
- ✓ More features
- ✓ New GUI





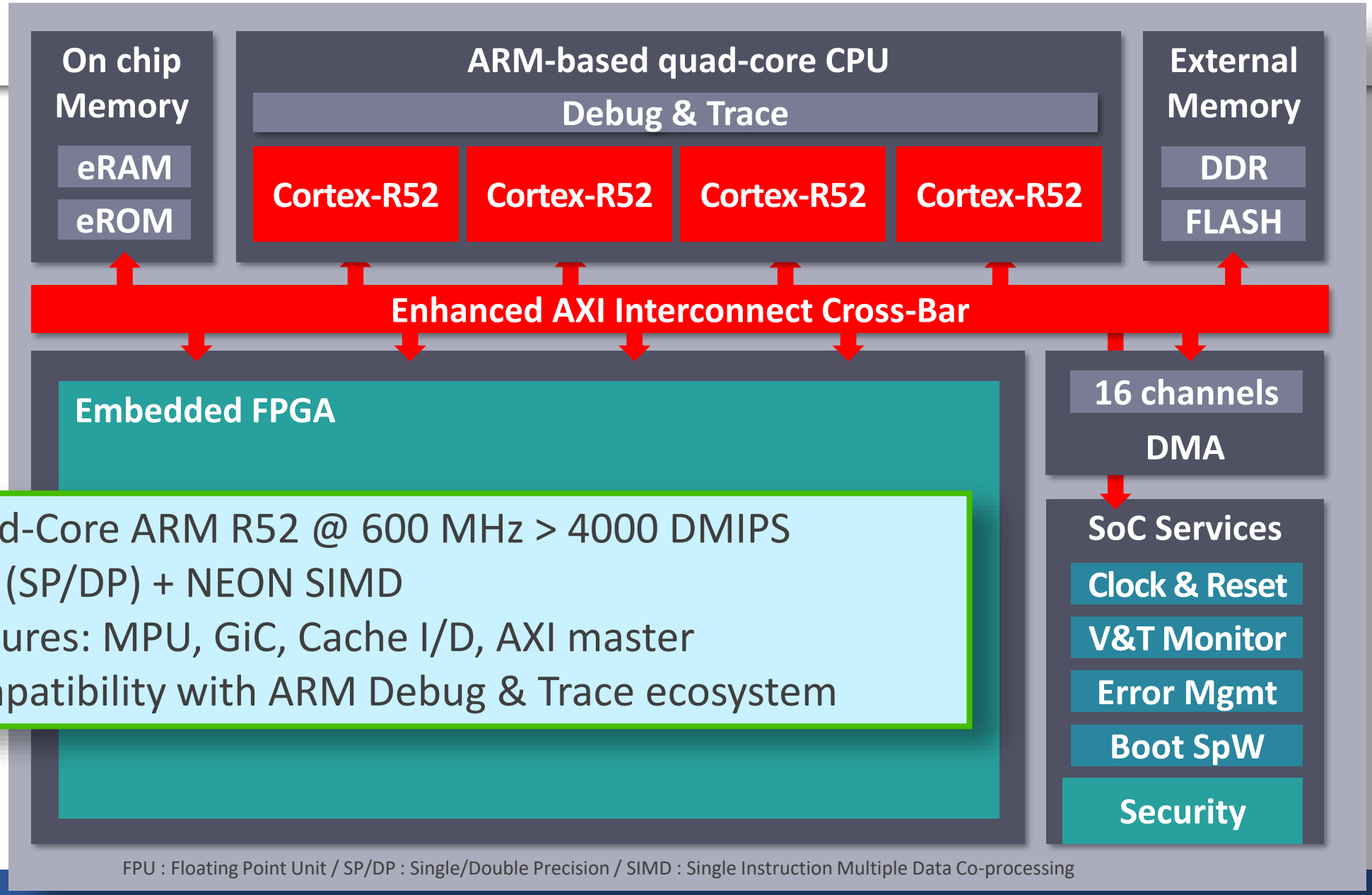
NG-ULTRA

Overview



- Quadcore ARM R52 @ 600MHz each
- 500KLUT density
- SpW & DDR 3&4 PHY hard-coded
- 32 HSSL @ 12.5 Gbps
- Radiation performances
  - TID 50krads(Si)
  - SEL and SEE immune

New Generation of Rad-Hard SoC



- → Quad-Core ARM R52 @ 600 MHz > 4000 DMIPS
- → FPU (SP/DP) + NEON SIMD
- → Features: MPU, GiC, Cache I/D, AXI master
- → Compatibility with ARM Debug & Trace ecosystem

FPU : Floating Point Unit / SP/DP : Single/Double Precision / SIMD : Single Instruction Multiple Data Co-processing

NG-ULTRA SdK

Board Support Package

- Generic build system for embedded software
  - Including Makefiles and generation instructions
  - Generic linker script
- Ready to use drivers
  - Flash, Clock & Reset, DMA, DDR, UART, eRAM, GIC…
  - ARM R52 init (crt0, handler, MPUs, stack…)
  - HAL and Helpers
- Example applications & demo

➢ Easy to use

NX Embedded Tools

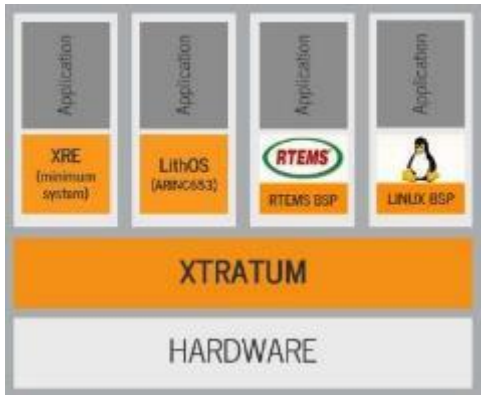
For NG-ULTRA

- ✓ Debugging facilities:
  - Lauterbach (debug & trace)
  - OpenOCD support
- ✓ Flash programmer
- ✓ Bitstream loader
- ✓ Memory dumper using DAP (debug access port)
- ✓ BL1 signer
- ✓ Read temperature sensor

➢ More on the way...

OS Supports

For NG-ULTRA



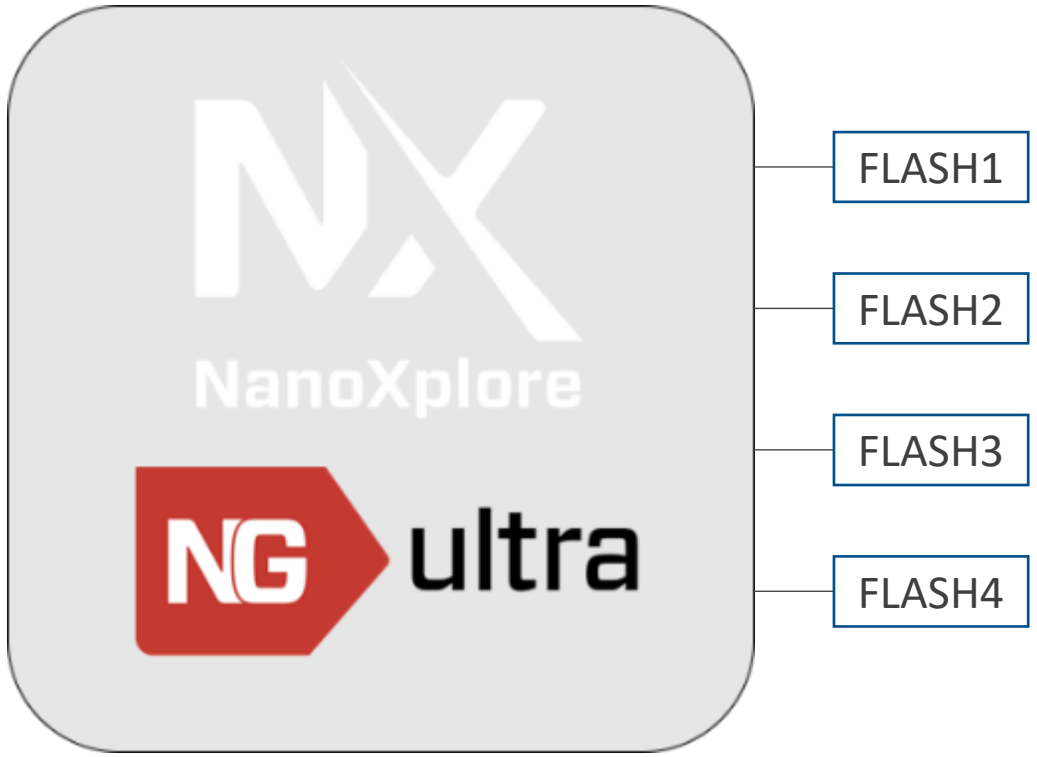
NG-ULTRA Configuration

Configuration Security

- BL1 authentication signature
- BL1 integrity verification
- Bitstream encryption
- Anti-rollback protection
- Lifecycle management
- Security information stored in OTP

NG-ULTRA Configuration

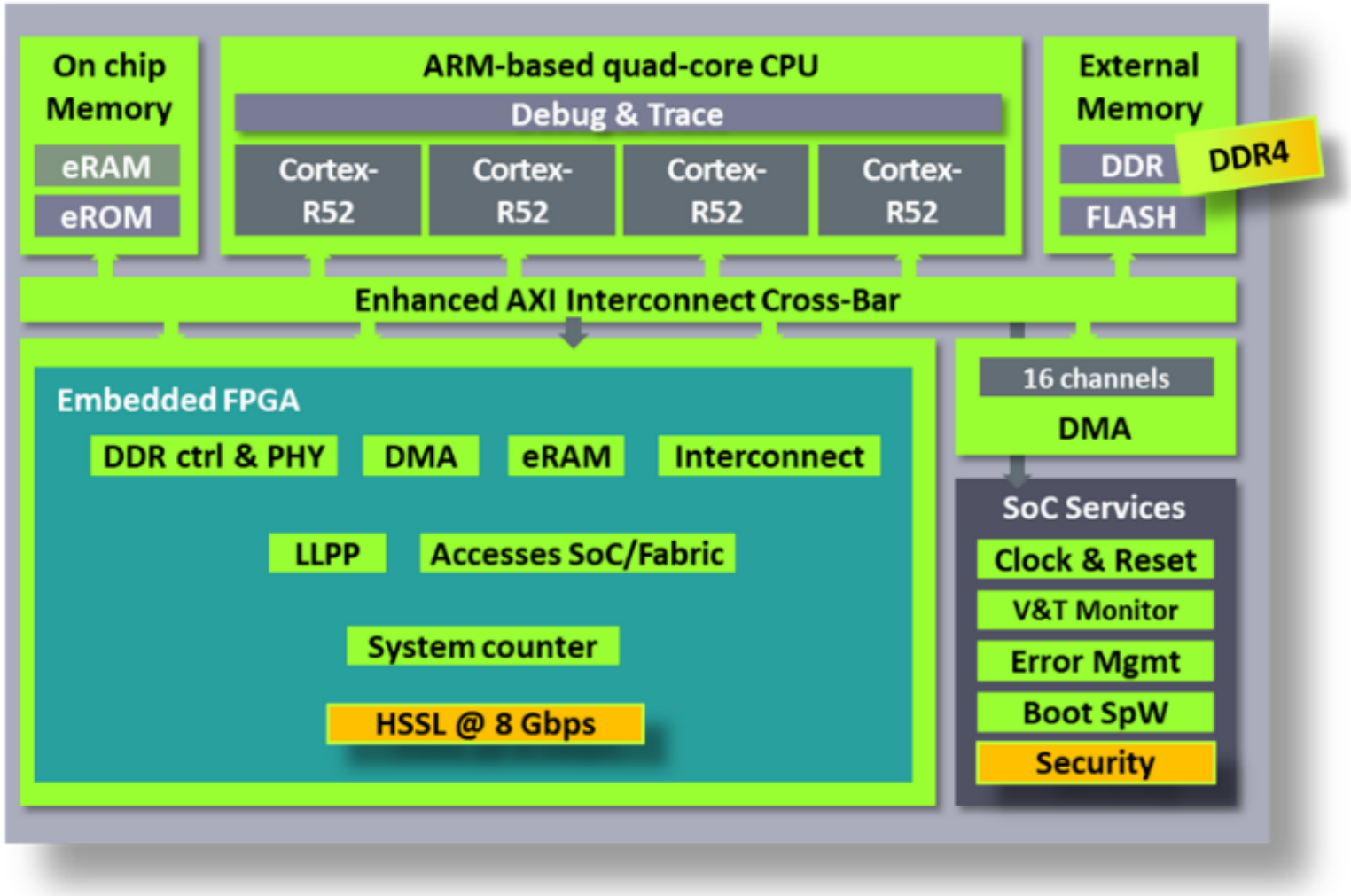
FLASH Loading



- 4 parallel SPI interfaces controlled by the boot loader
- FLASH mode:
  - SEQUENTIAL
  - TMR
    - Parallel read
    - NG-ULTRA performs the majority-voting
    - The last memory can be used for an application purpose

NG-Ultra HW

Maturity status



Functions

Validated

Functions

Ongoing validation

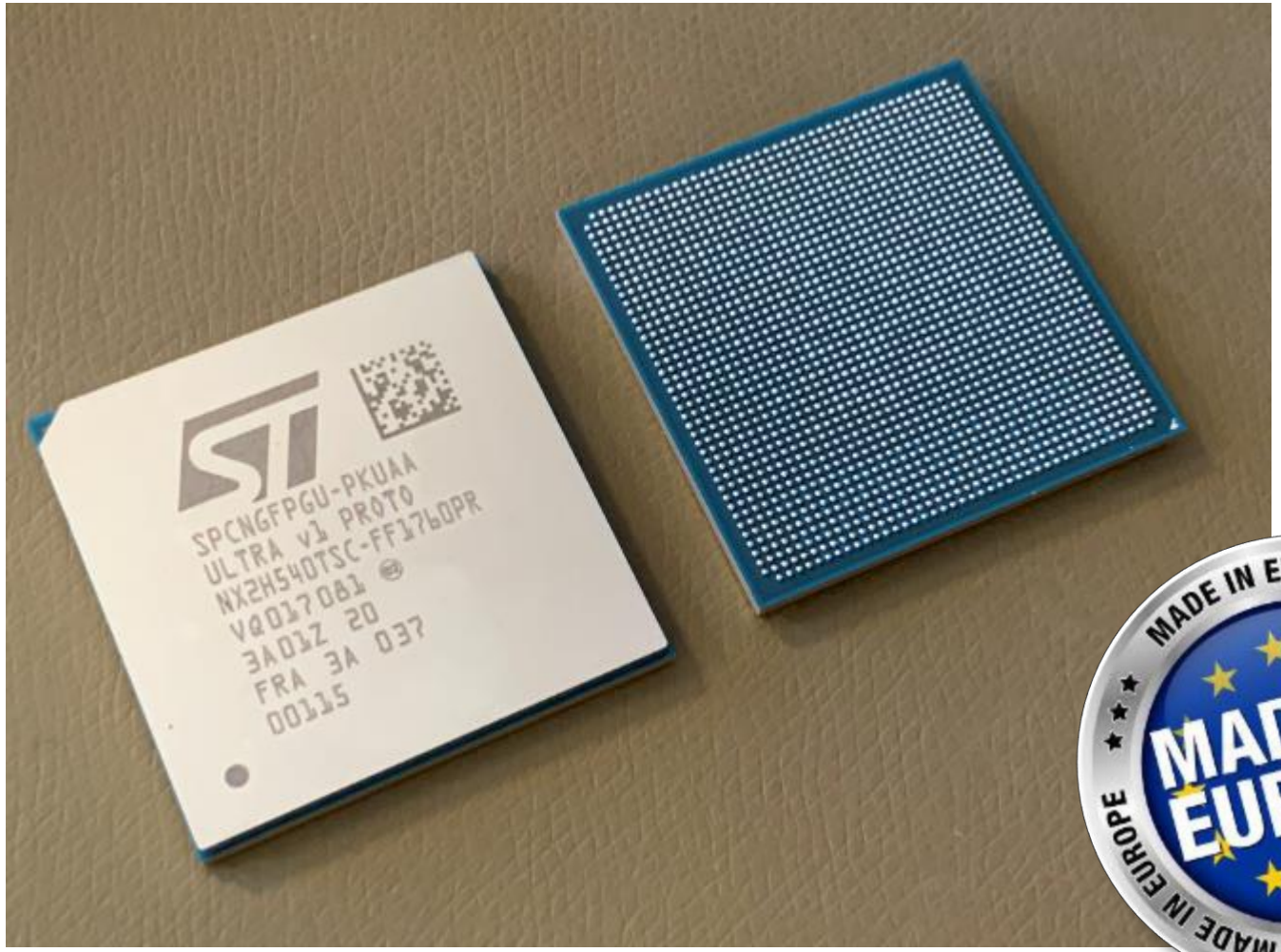
Radiation tests

Status and activities

- UCL / HIF campaign done in Dec 2020 and in June 2021 on NG-Ultra v1 Bring-up board
- Configuration memory
  - No errors detected up to 62MeV/g/cm3
- DFF
  - No errors detected up to 62MeV/g/cm3
- PLL
  - Good radiation performance for the PLL
  - No SEFI
- 3 new heavy ions campaigns planned in 2023
- **Latchup free, SEU Immune**

Having a European FPGA + SoC
Is not a dream anymore !

V1 samples tested since Q4 2020



V2 prototypes and evaluation kit available

NG-ULTRA Ecosystem

Fast Growing Ecosytem

NG-ULTRA

Status

Part Number	Designation	Status
NG-ULTRA DAISY CHAIN ORGANIC PACKAGE		
NX2H540TSC-FF1760DC	NX2H540 FF1760 Daisy Chain package	now
NG-ULTRA ORGANIC PACKAGE FF1760		
NX2H540ATSC-FF1760PR	NX2H540 FF1760 Prototype	now
NX2H540ATSC-FF1760M	NX2H540 FF1760 Military Part	Q2’23
NX2H540ATSC-FF1760E	NX2H540 FF1760 eq. ESCC9000P (-40 -> +125°c)	Q3’23
NG-ULTRA EVAL KIT		
NX2H540ATSC-EK	NX2H540TSC Evaluation Kit	now

What's Next?

28 nm FDSOI

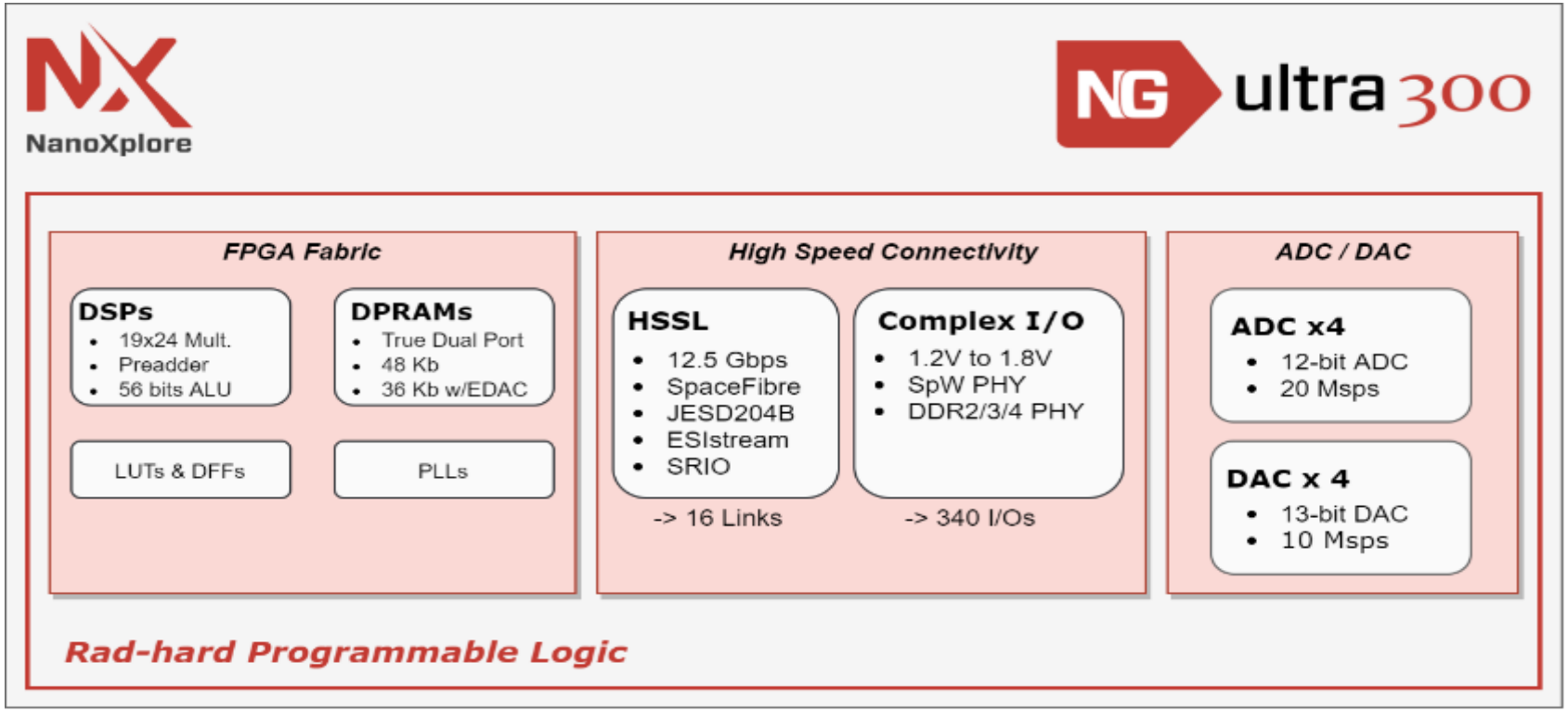
- Most cost-effective rad-hard FPGA
- 10x bigger than NG-MEDIUM
- 2x faster than 65nm
- Embedded ADC and DAC
- Small form factor in BGA 484
- Immune to SEE
- …

ULTRA 300 Overview

FPGA overview

- Small Form factor ➔ FCBGA-484
- High pin count ➔ FCBGA-1152 and CLGA/CCGA-1152
- 300KLUT & DFF, 22Mb RAM and 900DSP blocks
- Embedded ADCs & DACs

Radiation immune



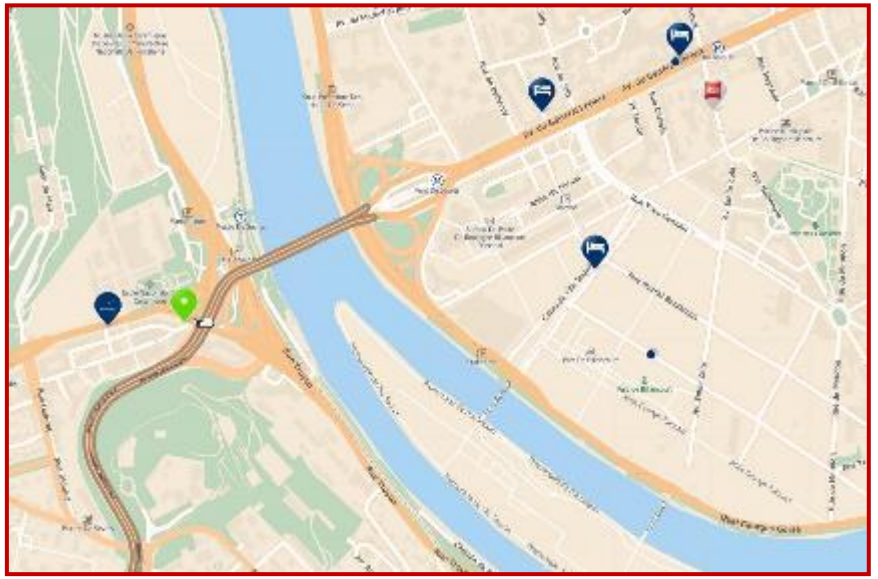
ULTRA 300 Overview

Most cost effective rad-hard FPGA solution

- Same architecture as NG-ULTRA
- Very easy design portage between the two FPGA
- Target ESCC 9000P qualification
- Key milestones
  - Prototypes Q3 2023
  - Eval kit Q3 2023
  - EQM Q2 2024

Device		Details	NX2H300TSA
Capacity - ASIC Gates	Rad Hard FPGA		**4 000 000**
Logic Modules		11x Tiles + 7CGBs	
Register		384DFF on 11rows	**273 408**
LUT-4		408LUT on 11rows	**290 496**
Carry		96CY on 11rows	**68 352**
Embedded RAM			**22Mb**
DPRAM		448BRAM * 48Kb	**21 504**
Core Register File		On 11 rows	**1 424**
Core Register File Bits		32*18bits	**807K Hardened**
Clocks / PLL			**50 / 6**
Additional Features	Rad Hard SOC		
SpaceWire PHY (8 IOBs)		2x/Complex IOBank	**20**
DDR3/4 PHY (11IOBs)		2x/Complex IOBank	**20**
DSP Blocks		From 7 rows	**896**
SpaceWire link I/F 430Mbps		CODEC	**1**
SERDES Tx/Rx 12,5Gbps (supporting several protocols such as Space Fibre)		4 Quad HSSL 12,5Gbps	**16**
Hard IP Processor core / SoC			**NO**
ADC		12-bit ADC, 10Msps	**1**
DAC		13-bit DAC, 10Msps	**1**
Design Security			**YES**
Inputs / Outputs	I/O		**547 I/Os**
Complex I/O bank		VIO 1,2 – 1,5 – 1,8V	**10 x 34 I/Os**
Simple I/O bank		VIO 1,8 – 2,5 – 3,3V	**6 x 24 I/Os + 1 x 16 I/Os**
Packages - User I/Os	PKG		
FF484 organic		27*27 mm / 1 mm	**239 I/Os (TBC)**
FF1152 organic		35*35 mm / 1 mm	**547 I/Os (TBC)**

Thank you



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