

# NG-Ultra, the European rad-hard SoC + FPGA suitable for future space applications

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**AIRBUS**

## Key Messages Summary

NG-Ultra is unique in the landscape of available Rad Hard components

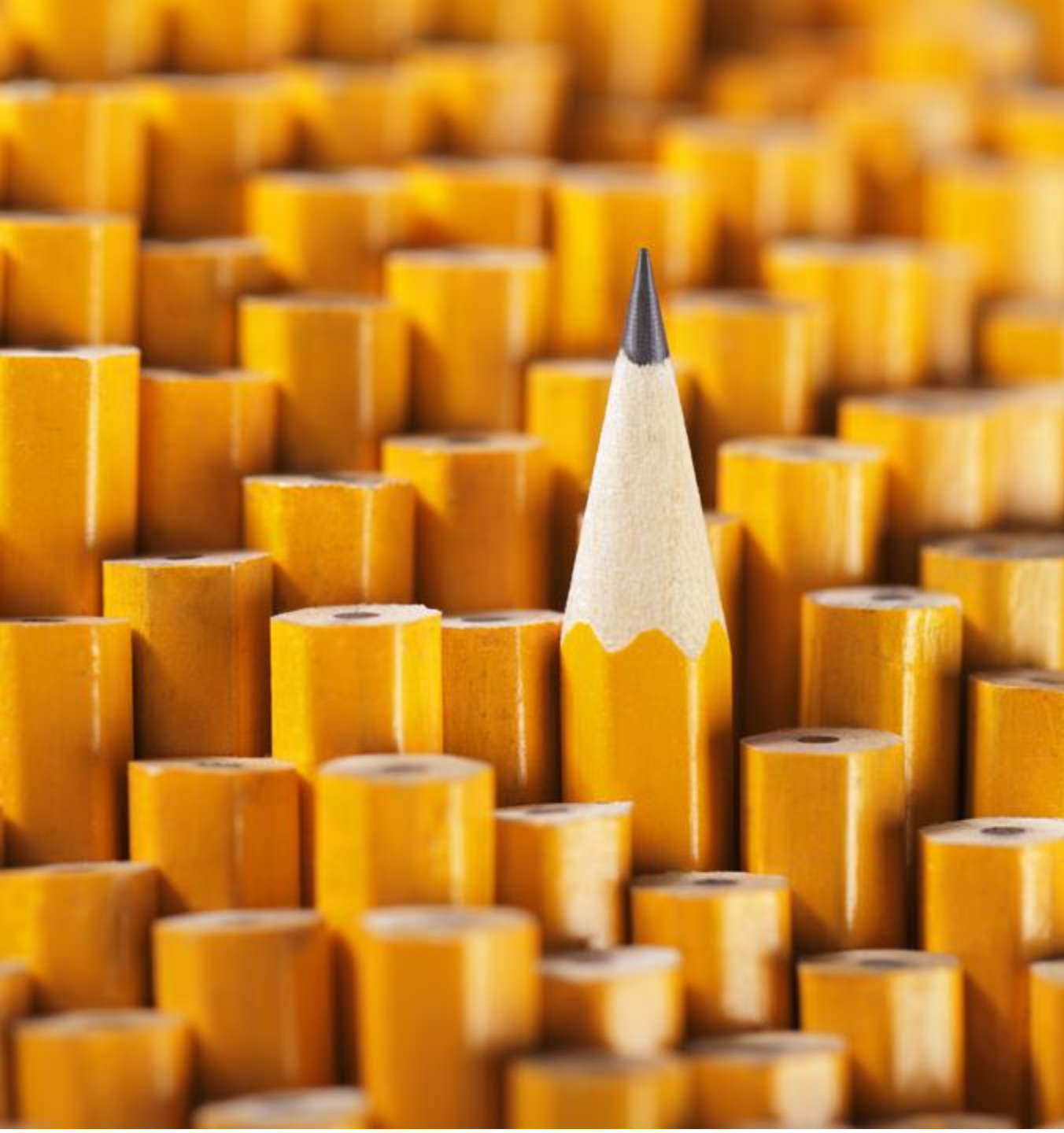
It is the only European FPGA solution with a SoC

It offers performances & robustness breakthroughs with Huge FPGA + High performance processing

Tools are (now) at good maturity level and continue to improve

NG-Ultra selected as technical baseline on several Airbus D&S on-going projects





# Why NG-Ultra is unique in the landscape of available Rad Hard components?

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Introduction

Performances Status

Ecosystem Status

Use Cases

Conclusion

Initiated by **CNES**, collaboration between **Airbus** and **TAS** to develop a **European chip** supported by H2020  
**NanoXplore** is the company owning and commercialising the **NG-Ultra** manufactured by **STMicro** in 28FDSOI

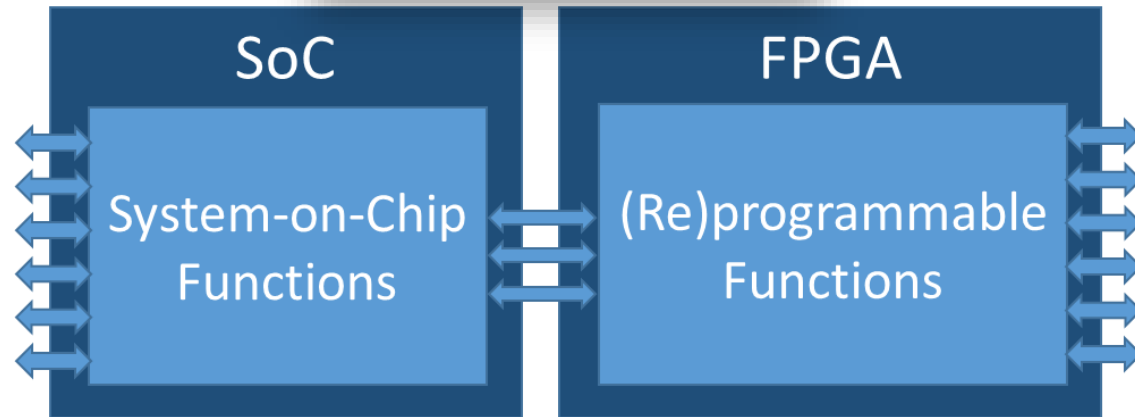
**NG-Ultra = SoC + FPGA**



Horizon 2020 was the EU's research and innovation funding programme from 2014-2020

# To integrated SoCs and beyond

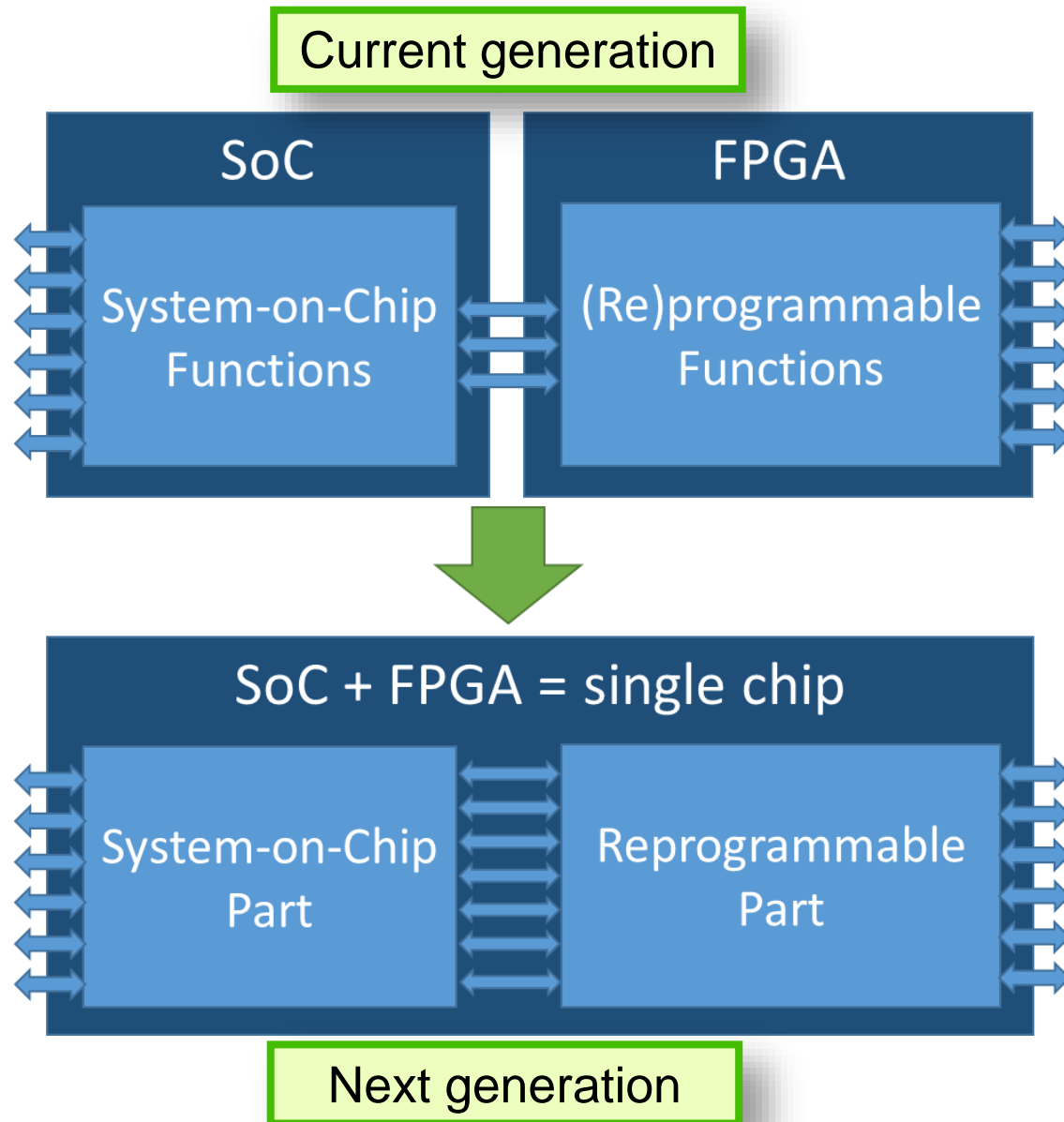
Current generation



Integrated SoC+FPGA

- ‡ Consistent with the design of processing boards
- ‡ Optimized interfaces SOC & FPGA
- ‡ Key enabler for more integrated designs & cost reduction

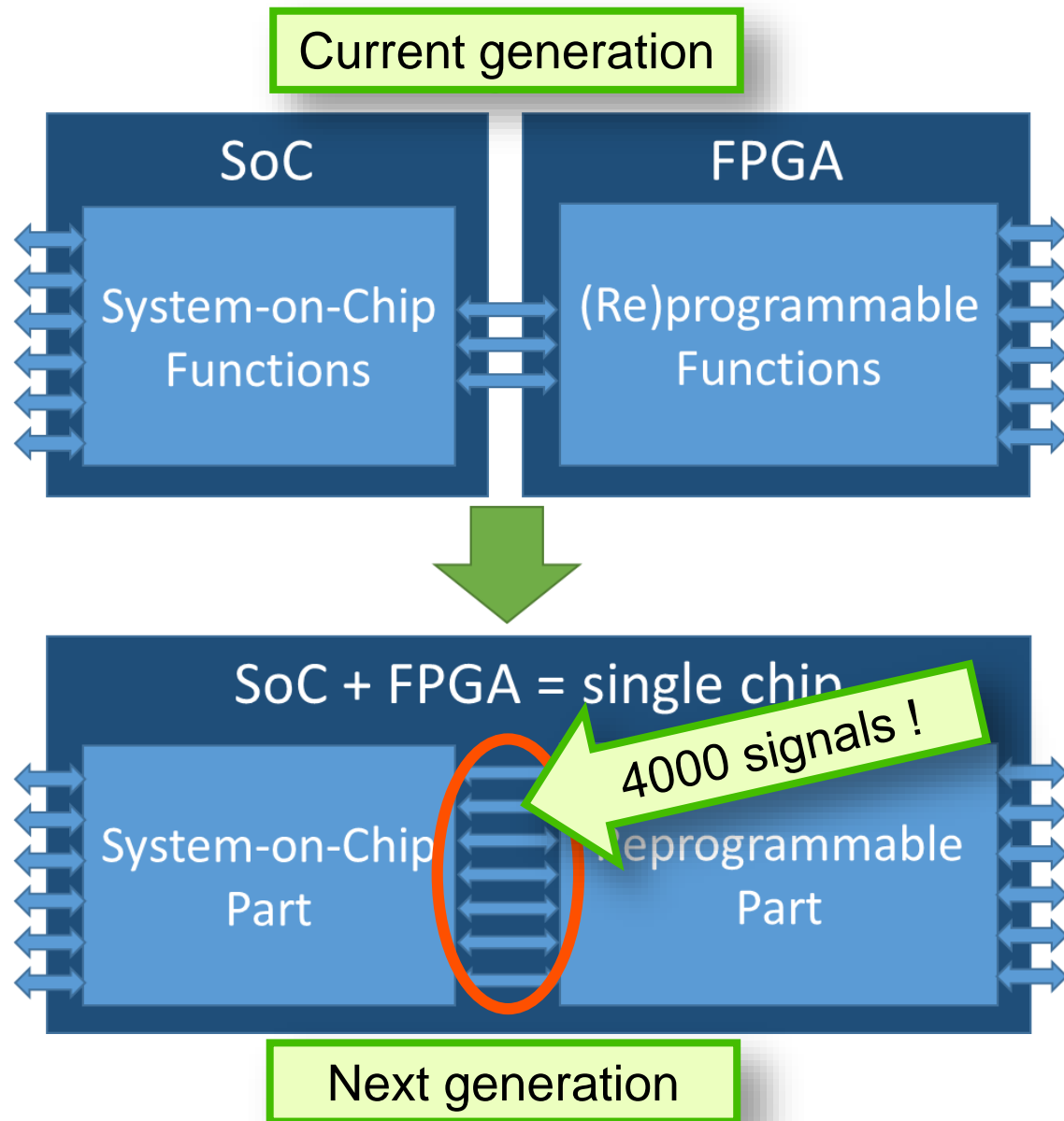
# To integrated SoCs and beyond



## Integrated SoC+FPGA

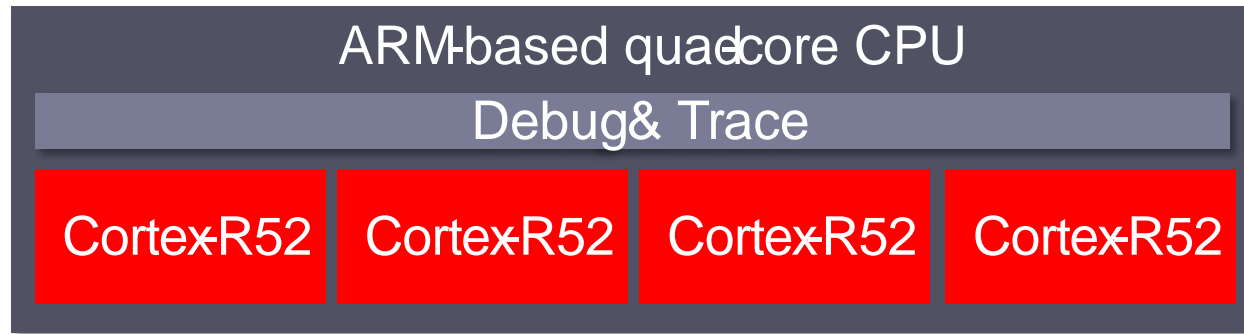
- ‡ Consistent with the design of processing boards
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# To integrated SoCs and beyond



## Integrated SoC+FPGA

- ‡ Consistent with the design of processing boards
- ‡ Optimized interfaces SOC ↔ FPGA
- ‡ Key enabler for more integrated designs & cost reduction



ÆQuad-Core ARM R52 @ 600 MHz > 4000 DMIPS  
ÆFPU (SP/DP) + NEON SIMD  
ÆCompatibility with ARM Debug & Trace ecosystem



# Features ±Memories

On chip  
Memory

eRAM

eROM

External  
Memory

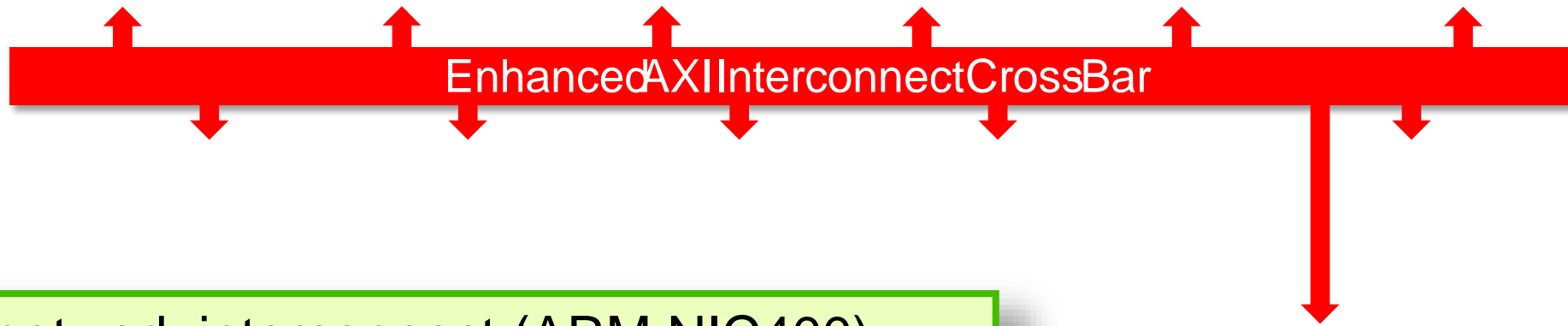
DDR

FLASH

16 channels

DMA

ÆBoot eROM + 2 MBytes eRAM w/ ECC  
ÆMemory interface (volatile) ÆDDR2/DDR3/DDR4  
ÆMemory interface (non volatile) ÆBoot NOR Flash  
Æ16 channels DMA to support memory transfers



ÆAXI network interconnect (ARM NIC400)  
ÆQuality of Service (QoS)

## Embedded FPGA

- Æ More than 500 K LUTs programmable matrix
- Æ HSSL in the FPGA
- Æ Additional on-chip services
- Æ Security features (e.g. bitstream encryption)

## SoC Services

Clock & Reset

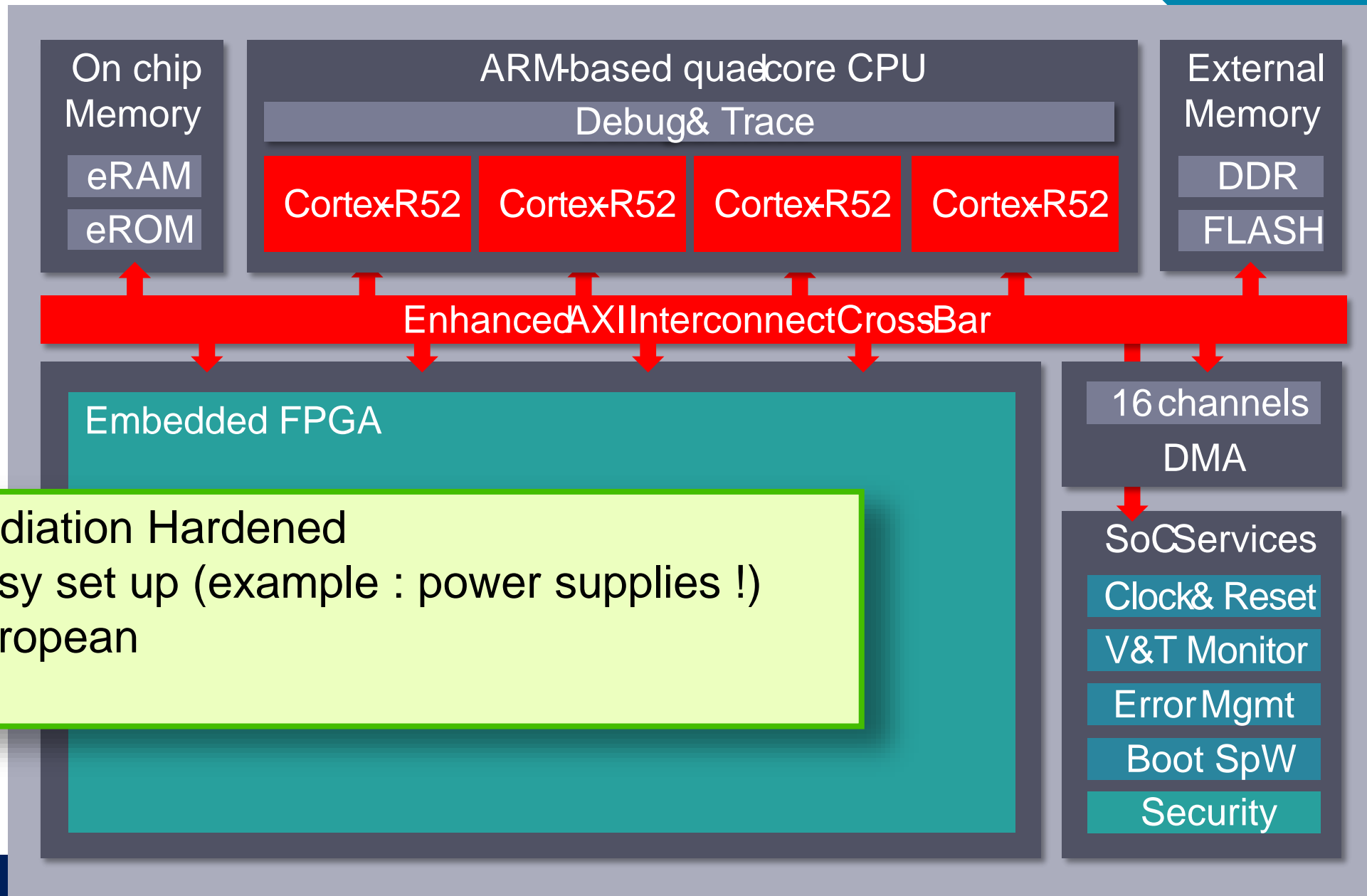
V&T Monitor

Error Mgmt

Boot SpW

Security

# Features ±What else ?



- Æ Radiation Hardened
- Æ Easy set up (example : power supplies !)
- Æ European
- Æ «

How I see my design



How the others see it



What are the breakthroughs (\*) of NG-Ultra architecture and detailed performances ?

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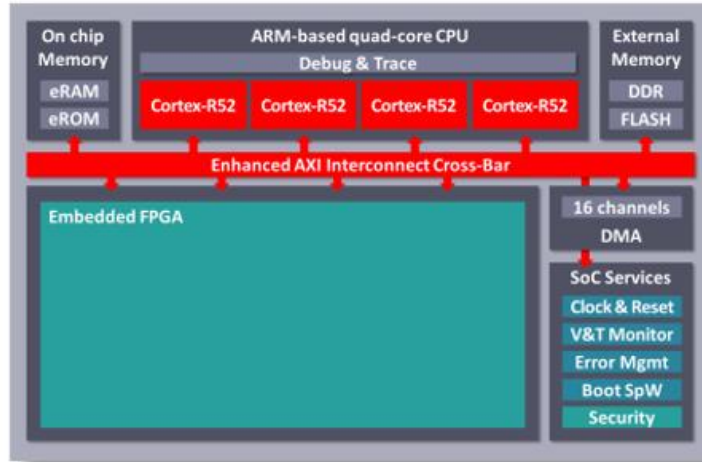
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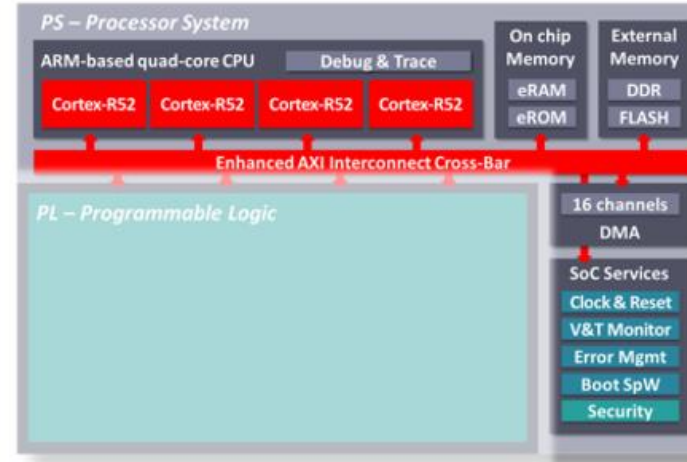
(\*) for a rad-hard component

# High level performances comparison

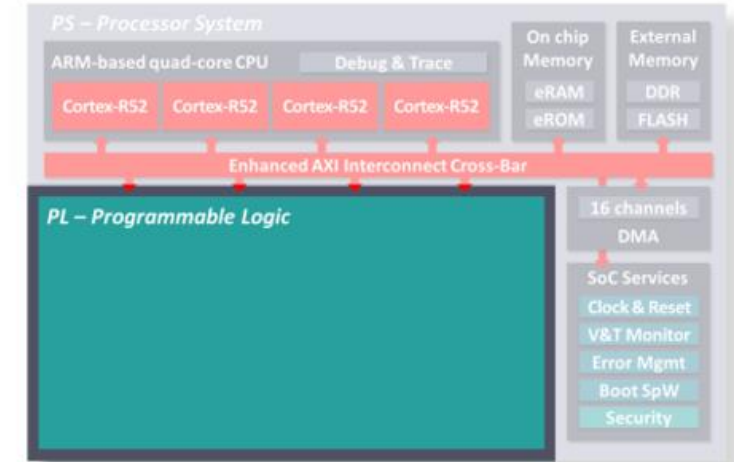
## SoC + FPGA



## SoC only



## FPGA only



### NG-Ultra processing perfo

1 818 CoreMark / core

1 250 DMIPS / core

### NG-Ultra FPGA capacity

~530 KLUT

### CPU Performance

Æ40 x SCOC3

Æ2 x GR740

### FPGA Capacity

Æ2 x RTG4 (\*)

Æ25 x RTAX2000 (\*)

(\*) estimation of realistically useable FPGA size at Q1/2023 date, twice more to be expected considering theoretical LUTs resources and the strong momentum deployed on tools improvement

# High level performances comparison

Table: Power Supply Ramp Time

Symbol	Description	Min	Max	Units
T <sub>VCCINT</sub>	Ramp time from GND to 95% of V <sub>VCCINT</sub>	0.2	40	ms
T <sub>VCCINT_IO</sub>	Ramp time from GND to 95% of V <sub>VCCINT_IO</sub>	0.2	40	ms
T <sub>VCCINT_VCU</sub>	Ramp time from GND to 95% of V <sub>VCCINT_VCU</sub>	0.2	40	ms
T <sub>VCCO</sub>	Ramp time from GND to 95% of V <sub>VCCO</sub>	0.2	40	ms
T <sub>VCCAUX</sub>	Ramp time from GND to 95% of V <sub>VCCAUX</sub>	0.2	40	ms
T <sub>VCCBRAM</sub>	Ramp time from GND to 95% of V <sub>VCCBRAM</sub>	0.2	40	ms
T <sub>MGTA VCC</sub>	Ramp time from GND to 95% of V <sub>MGTA VCC</sub>	0.2	40	ms
T <sub>MGTA VTT</sub>	Ramp time from GND to 95% of V <sub>MGTA VTT</sub>	0.2	40	ms
T <sub>MGTVCCAUX</sub>	Ramp time from GND to 95% of V <sub>MGTVCCAUX</sub>	0.2	40	ms
T <sub>VCC_PSINTFP</sub>	Ramp time from GND to 95% of V <sub>VCC_PSINTFP</sub>	0.2	40	ms
T <sub>VCC_PSINTLP</sub>	Ramp time from GND to 95% of V <sub>VCC_PSINTLP</sub>	0.2	40	ms
T <sub>VCC_PSAUX</sub>	Ramp time from GND to 95% of V <sub>VCC_PSAUX</sub>	0.2	40	ms
T <sub>VCC_PSINTFP_DDR</sub>	Ramp time from GND to 95% of V <sub>VCC_PSINTFP_DDR</sub>	0.2	40	ms
T <sub>VCC_PSADC</sub>	Ramp time from GND to 95% of V <sub>VCC_PSADC</sub>	0.2	40	ms
T <sub>VCC_PSPLL</sub>	Ramp time from GND to 95% of V <sub>VCC_PSPLL</sub>	0.2	40	ms
T <sub>PS_MGTRAVCC</sub>	Ramp time from GND to 95% of V <sub>PS_MGTRAVCC</sub>	0.2	40	ms
T <sub>PS_MGTRAVTT</sub>	Ramp time from GND to 95% of V <sub>PS_MGTRAVTT</sub>	0.2	40	ms
T <sub>VCCO_PSDDR</sub>	Ramp time from GND to 95% of V <sub>VCCO_PSDDR</sub>	0.2	40	ms
T <sub>VCC_PSDDR_PLL</sub>	Ramp time from GND to 95% of V <sub>VCC_PSDDR_PLL</sub>	0.2	40	ms
T <sub>VCCO_PSDDR_PLL</sub>	Ramp time from GND to 95% of V <sub>VCCO_PSDDR_PLL</sub>	0.2	40	ms

FPGA only

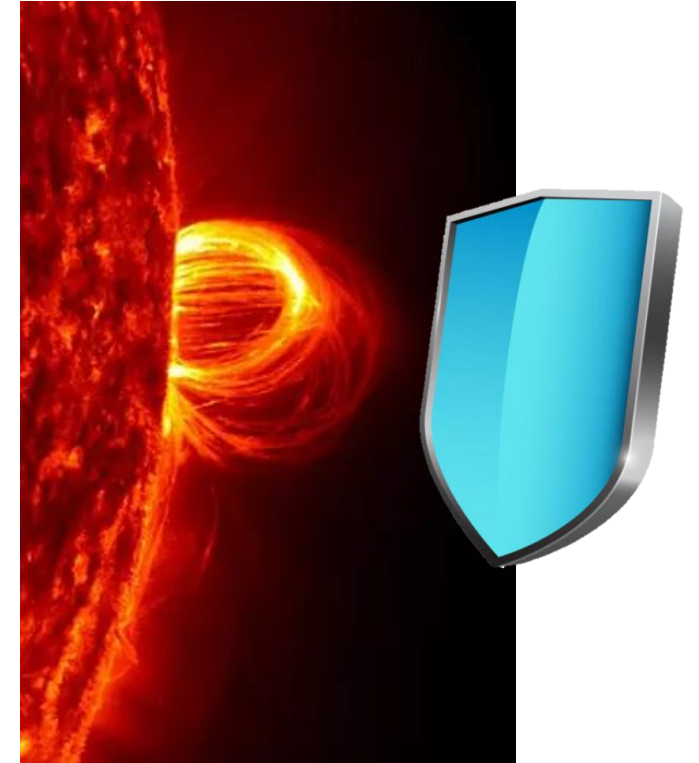
Comparing performances is important but not enough. Many other criteria shall be considered such as package, radiation hardening, cost, hardware setup (memories, power supply « K D U GaZd U H software ecosystem, U L V N P L W L J D W L R Q R I H [ S R U W F R Q W U R O O L P L W D

## NG-80WUD UDGLDWLRQ UREXVWC

- ‡28FDSOI technology intrinsically latch-up immune Æno SEL
- ‡NG-Ultra tested during 2 radiation campaigns Æno SEFI
- ‡Robustness confirmed (no SEU, no SEFI) on v1, v2 launched

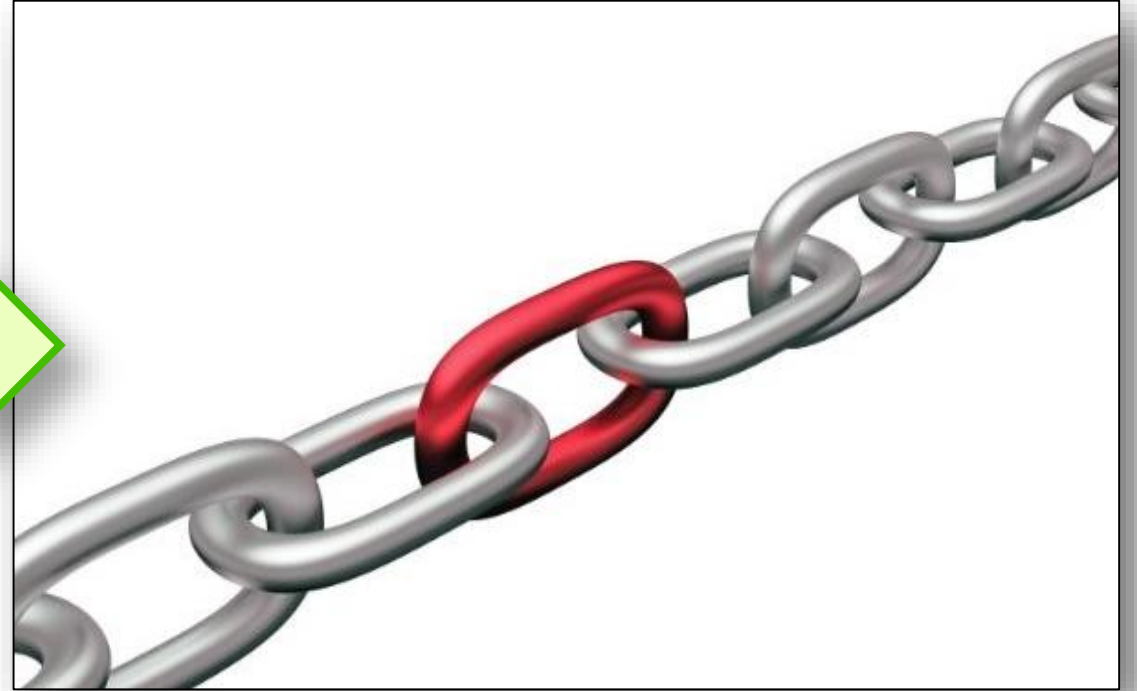
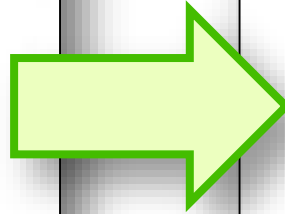
## DDR memory protection Æa game changer

- ‡Supporting DDR2, DDR3 and DDR4 / 8-bits & 16-bits devices
- ‡Reed-Solomon for SEU high level of memory protection
- ‡Robustness against SEFI up to the loss of two 16-bits devices





# NG-Ultra architecture approach ±No « weakest link »



Having a high performance and very robust component is not enough, because if it is associated to sensitive components (such as peripheral memories), the overall system performance is degraded. As an example, if you need to reboot each time you have an upset in a memory, this will drive the way you design the system.

NG-Ultra solves this issue, since (1) it offers a robust Radiation Hardened By Design (RHBD) chip and (2) it provides unprecedented protection mechanisms for all of its peripheral components (Flash, DDR) allowing to achieve high reliability.



# What about the ecosystem to develop with NG-Ultra ?

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Horizon 2020 was the EU's research and innovation funding programme from 2014-2020

OPERA project objectives were to assess the performances that can be achieved by some designs in NG-ULTRA technology and compare it with performances achieved in reference technologies.

Several designs from low to higher complexity synthesized on both NG-Ultra and RTG4 targets

## ±Synthesis

9Synthesis time Æsimilar performance on both technologies

9Clock frequency Æsimilar performance ~100MHz, Libero/RTG4 slightly better handles complex design

9Resource utilization Æperformance in favor of NG -Ultra factor of 1.5 in nb of LUT, factor 2 improvement on large memories due to NG-Ultra larger BRAM, larger DSP width +++ for algo

## ±Place and Route

9Not easy to obtain a good layout in one run whatever the target Æsimilar performance

**NG-Ultra relevance confirmed for ADS future projects !**



# What about first use cases targeted by Airbus with NG-Ultra ?

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# NG-Ultra already on ADS Projects - Platform OBC-Ultra

## NG-Ultra present in both platform & payload ADS roadmaps

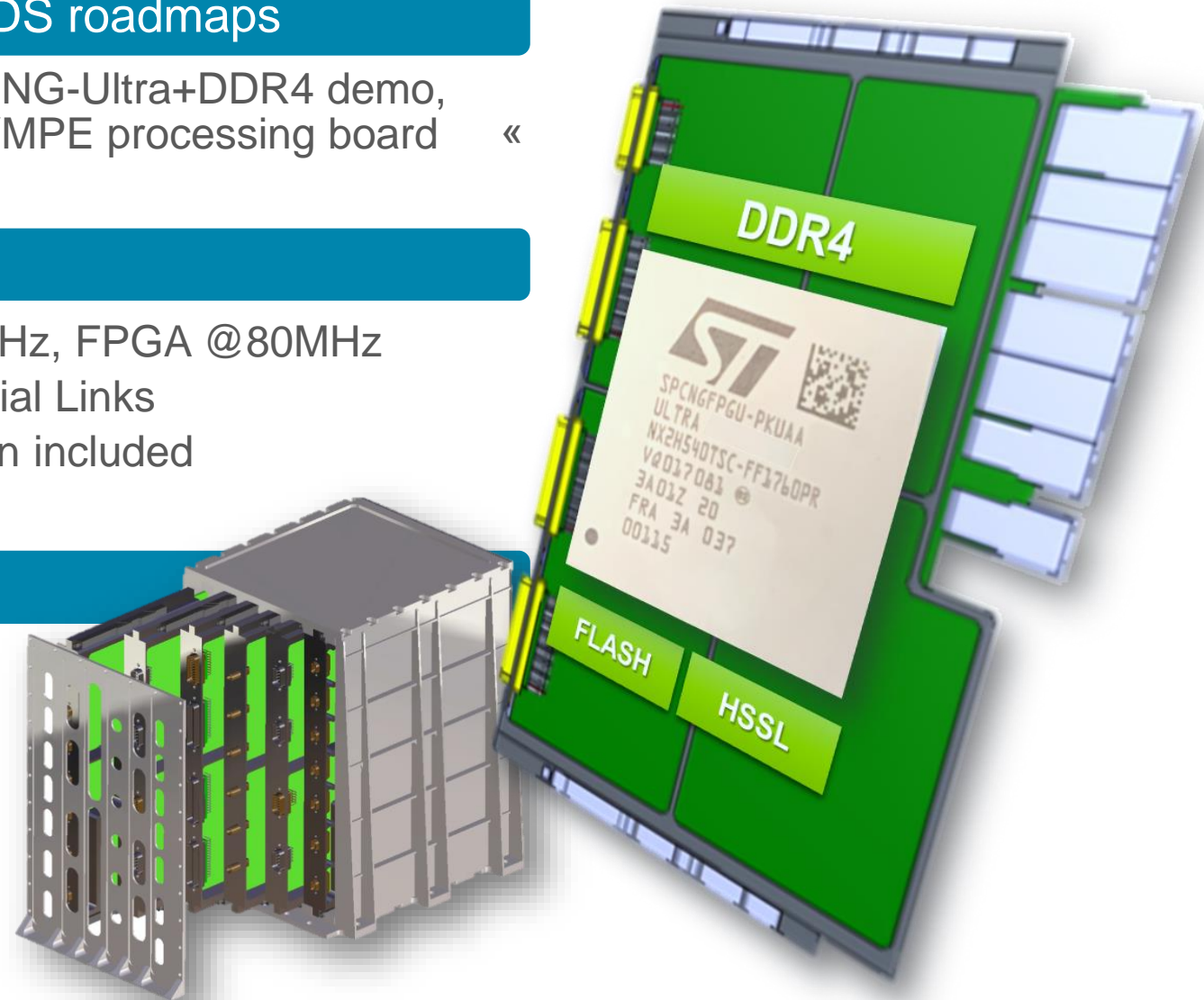
- ‡Several boards under development **AEQ2 2023** / NG-Ultra+DDR4 demo, **Q3 2023** / OBC use case demonstrated with OLYMPE processing board
- ‡One main component = simplified board design

## NG-Ultra-based OBC

- ‡High performances multicore processing @600MHz, FPGA @80MHz
- ‡NAND Flash + **DDR4 Memory** + High Speed Serial Links
- ‡Enhanced Security features / Bitstream encryption included
- ‡ADHA-compatible format

## Highly integrated OBC-Ultra

- ‡Gain in performances confirmed through studies
- ‡More than **500kLUT** compared to ~20kLUT for previous generation with RTAX2000
- ‡More embedded functionalities
- ‡**Very compact product**



# NG-Ultra on ADS Projects - Payload Missions

Payload missions requirements analysis

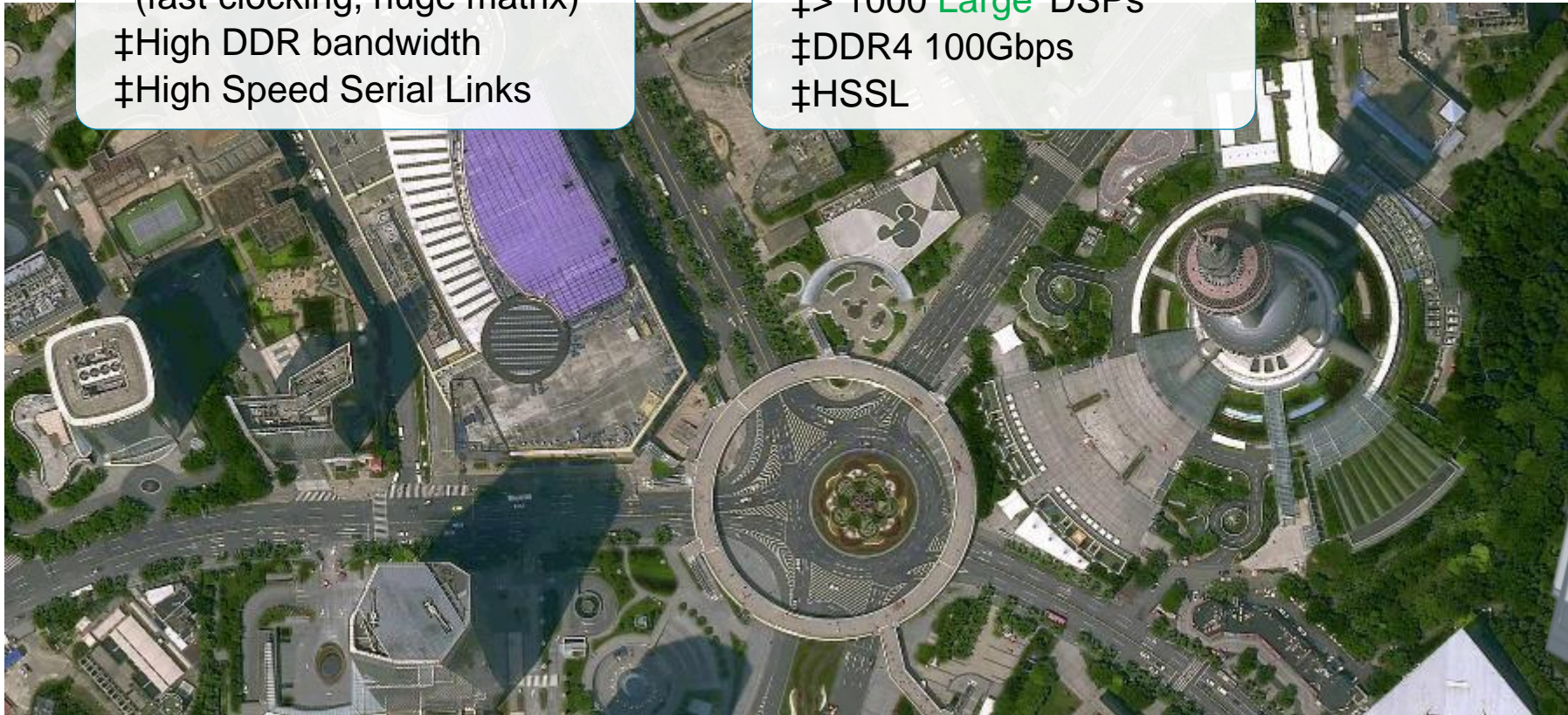
- ‡Very performant FPGA (fast clocking, huge matrix)
- ‡High DDR bandwidth
- ‡High Speed Serial Links

NG-Ultra suitability ?  
Confirmed !

- ‡Huge 500k LUT matrix
- ‡> 1000 Large DSPs
- ‡DDR4 100Gbps
- ‡HSSL

NG-Ultra-based board for payload processing under development at Airbus

- ‡Ground demonstrator ready for Q4 2023



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How the others see it



What can be concluded considering the overall picture and status on NG-Ultra ?

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NG-Ultra is unique in the landscape of available Rad Hard components

It is the only European FPGA solution with a SoC

It offers performances & robustness breakthroughs with Huge FPGA + High performance processing

Confidence in tools capacity to meet performances for complex designs use cases (cf OPERA)

NG-Ultra selected as technical baseline on several Airbus D&S on-going projects

Questions??