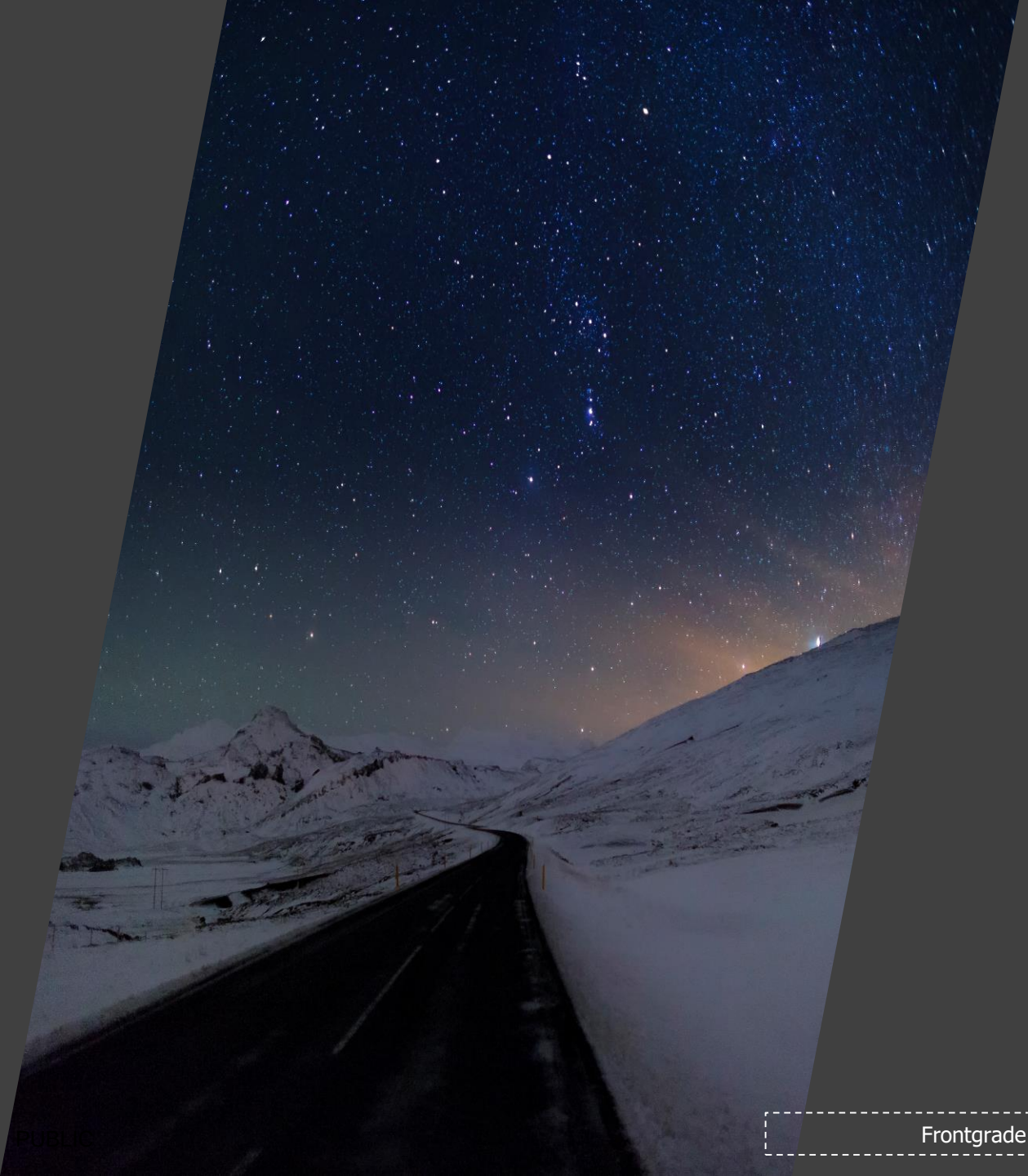


FRONTGRADE

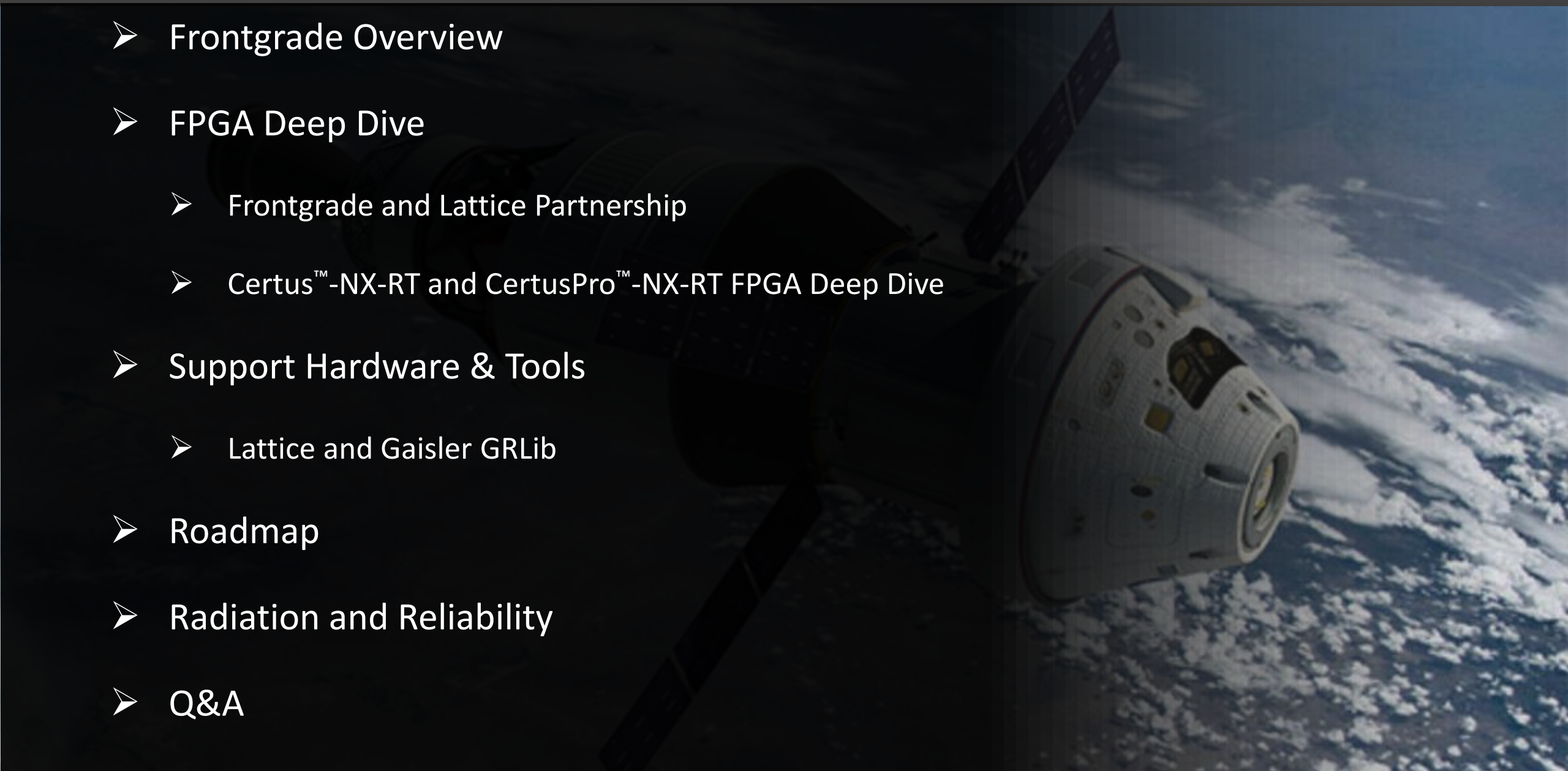
Innovating At The Speed Of Technology

Next-Gen FPGAs For Space

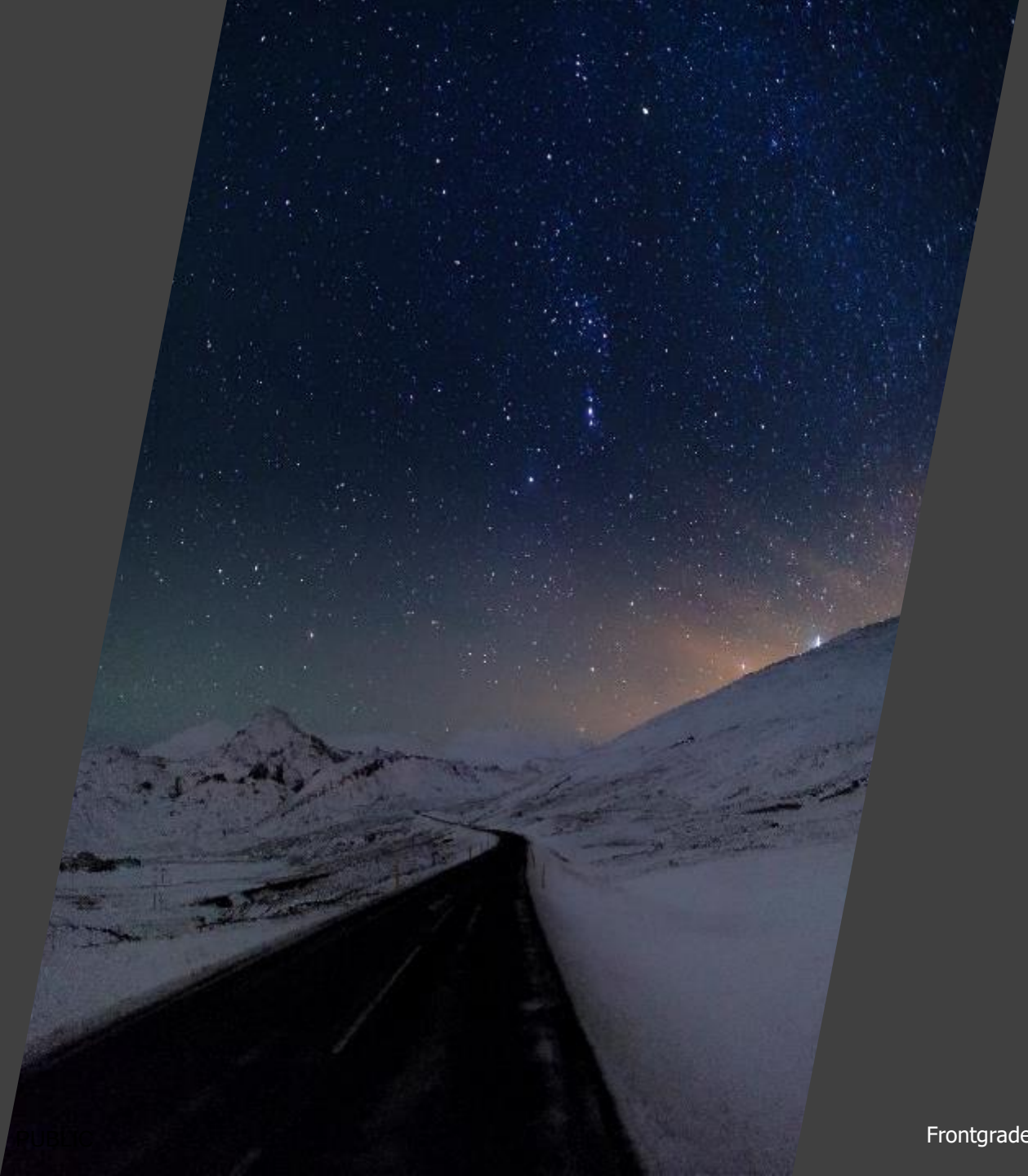
March, 2023

David Meyouhas – Sr Director of Standard Products
Brian Baranski – Systems Architect

Agenda



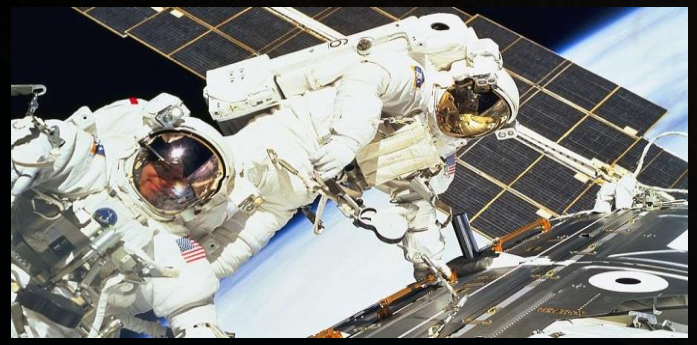
- Frontgrade Overview
- FPGA Deep Dive
  - Frontgrade and Lattice Partnership
  - Certus™-NX-RT and CertusPro™-NX-RT FPGA Deep Dive
- Support Hardware & Tools
  - Lattice and Gaisler GRLib
- Roadmap
- Radiation and Reliability
- Q&A



FRONTGRADE

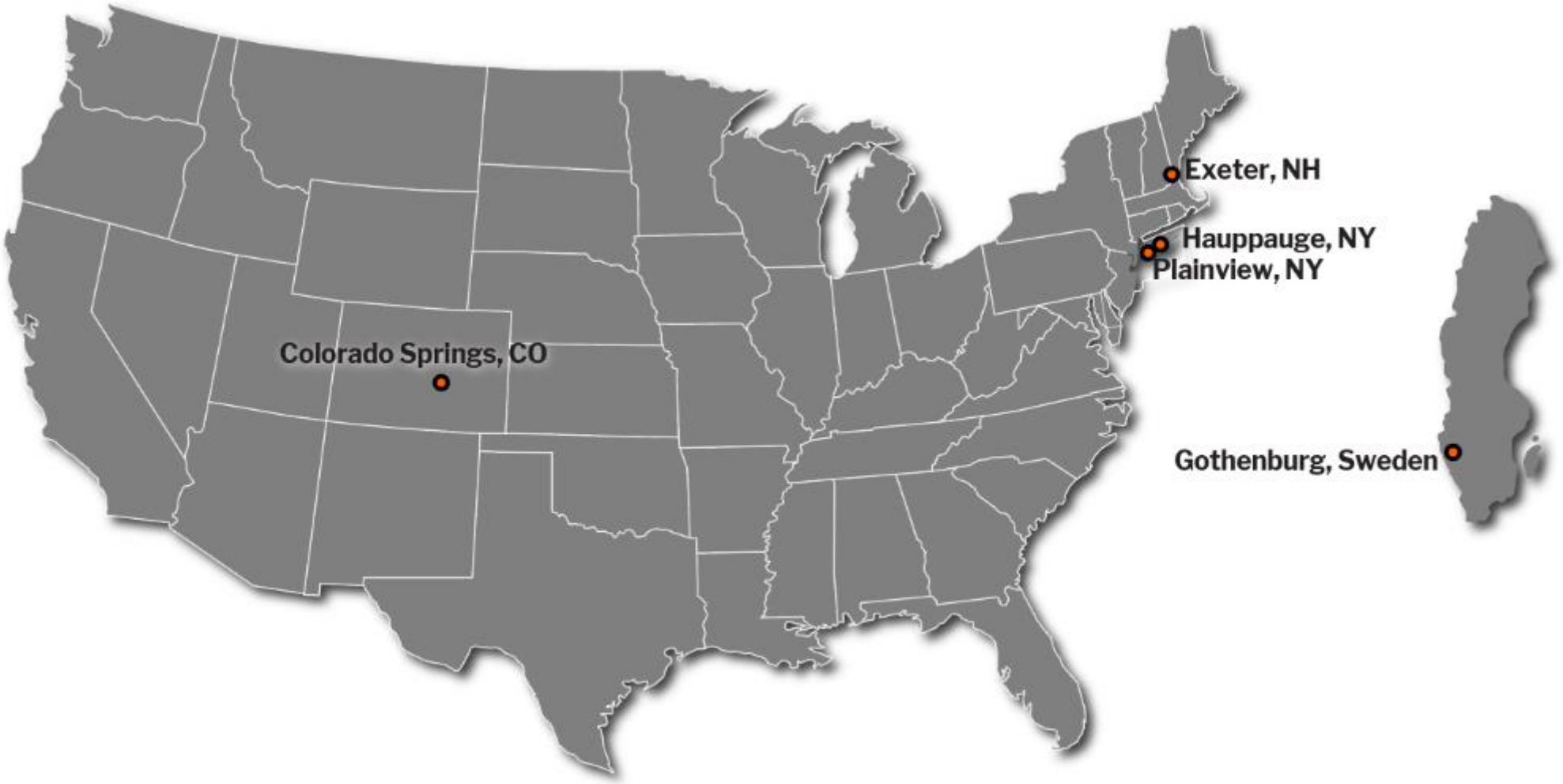
Frontgrade Overview

Overview



- Frontgrade is a stand-alone Company serving Space, Defense and Commercial customers with advanced electronic solutions
- Frontgrade pioneers new technology leveraging decades of heritage in the harshest domains
- Veritas Capital acquired the Space Systems Division of CAES from Advent International in January 2023
- Over 1,100 employees across the US and Europe
- Frontgrade is headquartered in Colorado Springs USA, and is comprised of five sites

Locations



Frontgrade – Microelectronics History

1980

1980
United Technologies Microelectronics Center (UTMC) founded

1998

1998
UTMC acquired by Aeroflex

2008

2008
Aeroflex acquires Gaisler Research

2014

2014
Aeroflex acquired by Cobham

2020-2021

2020
Acquired by Advent International and rebranded as CAES

2023

2023
Acquired by Veritas Capital and rebranded as Frontgrade

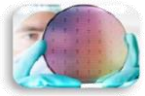
Operating Business Units

Microelectronics


Microprocessors


Microcontrollers


Logic / FPGA


ASIC Design


Packaging & Test


Single Board Computer

Rad-Hard Components:
- FPGA
- Microprocessors
- Microcontrollers
- Memory
- Interconnects

Custom ASICs:
- ASIC design
- Packaging & test

Mission Processing:
- Single board computer
- Box design & assembly
- Manufacturing

Major Sites:
- Colorado Springs, CO (two facilities)
- Gothenburg, Sweden

Electro-Mechanical Systems


Waveguides


Cables


Rotary Joints


Steerable


Non-Steerable


Motion Control


Slotted Flat Panel

RF Transmission:
- Waveguides
- Cables
- Rotary joints

Antennas:
- Steerable antennas
- Non-steerable antennas
- Slotted flat panel

Motion Control:
- Motion control products
- Satellite solar panel actuation
- Mars Rover arm actuation
- Optical steering

Major Sites:
- Exeter, NH
- Hauppauge, NY

Power Solutions


Converters


Battery Electronics


Synthesisers

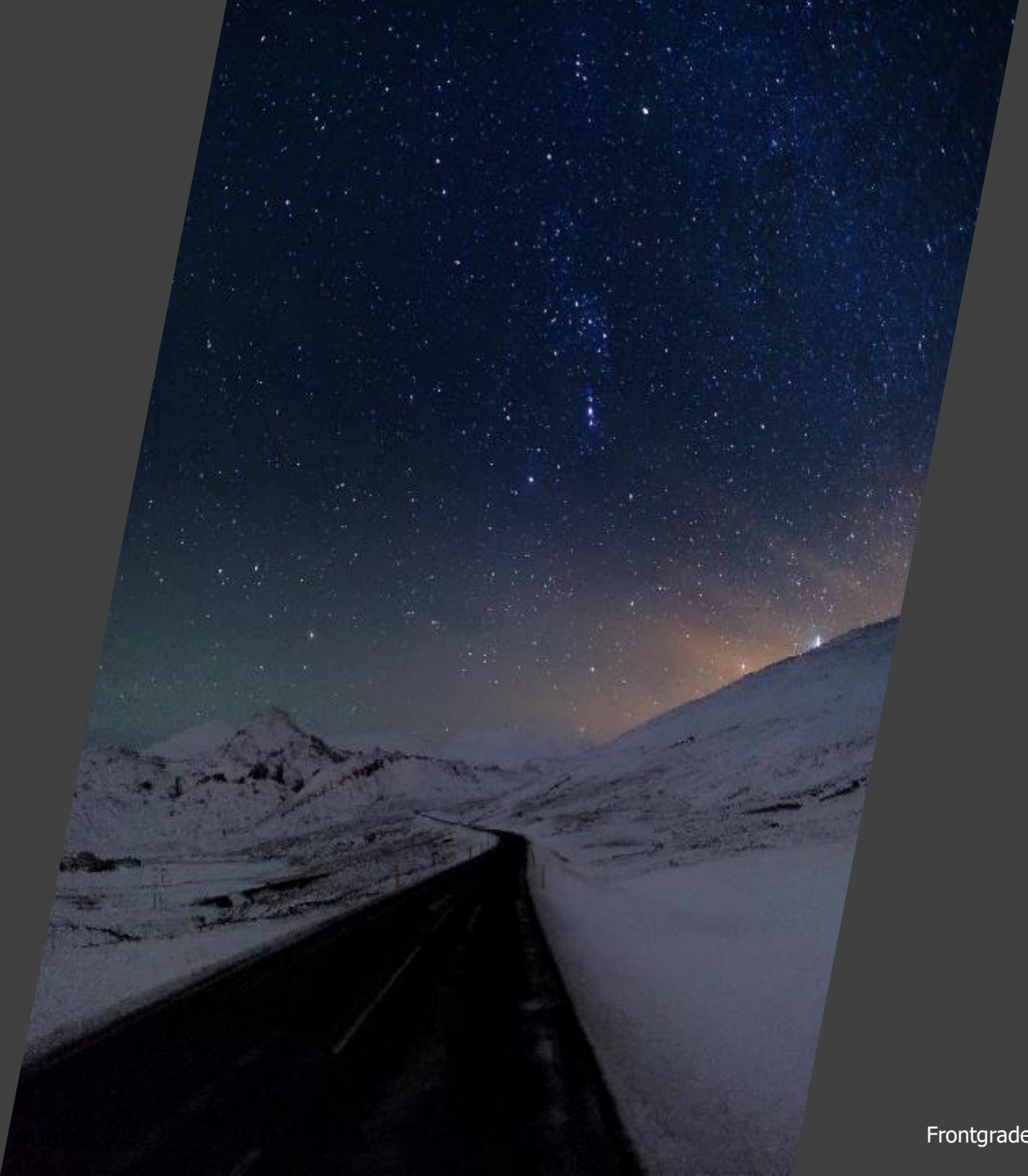

Hybrids


Modules

Power Management:
- Converters
- Modules
- Battery electronics
- Hybrids

RF Generation:
- Synthesizers

Major Sites:
- Plainview, NY



FRONTGRADE

FPGA Deep Dive

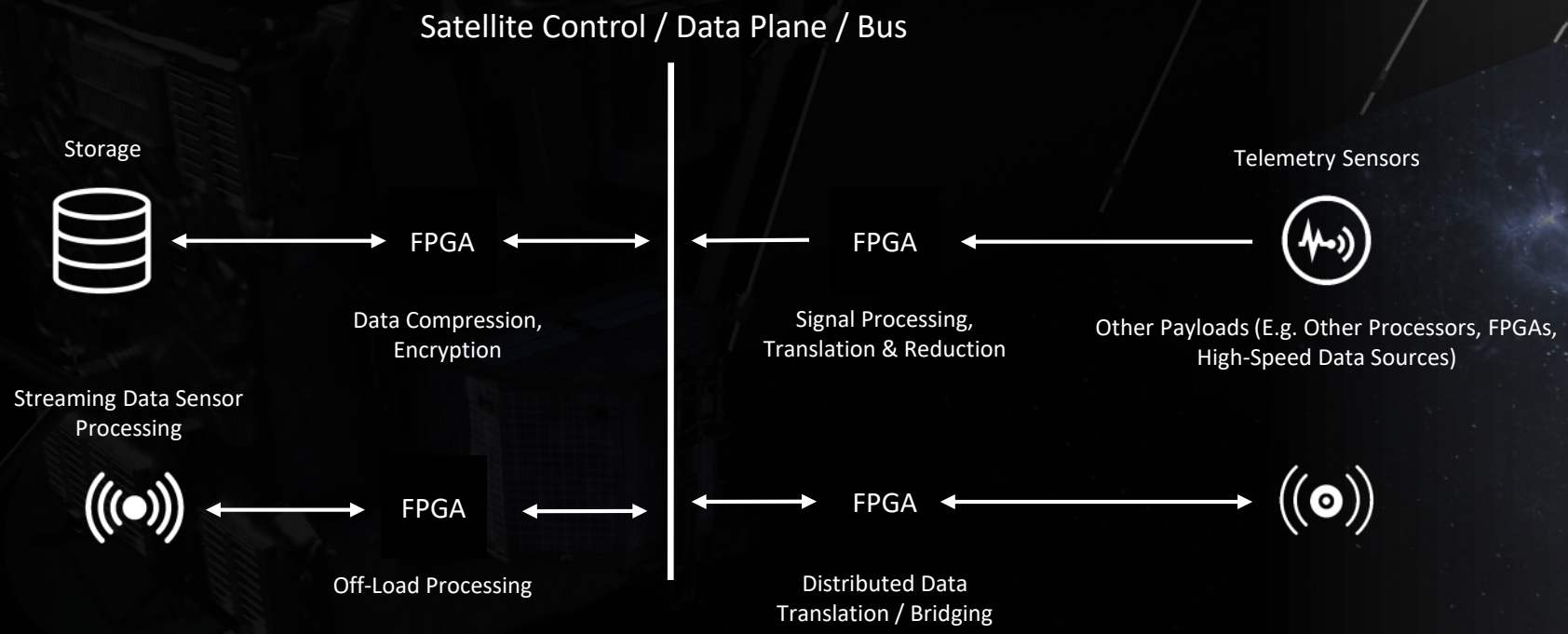
Scalable, High-Reliability Distributed Processing

Making Satellites Multi-Functional, Reconfigurable and Autonomous

FRONTGRADE

Space engineers need versatile, reliable processing solutions that are easy to use and scale

- Inter-box comms, data translation and bridging
- Distributed sensor processing and platform management
- Robotics and motor control
- Off-load processing



Versatility / performance has made FPGAs the indispensable distributed processing building block

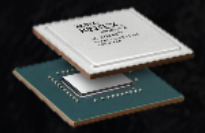
When Small FPGAs and Microcontrollers Are Not Enough

And Large FPGAs Are Overkill

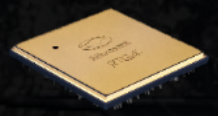
FRONTGRADE

Performance

Large FPGAs and Processors



Xilinx KU060



Microchip RTG4

Microchip RT Polarfire

Xilinx Versal

FPGAs for Distributed Space Processing

Small FPGAs and Microcontrollers

Vorago VA41630

Microsemi RT ProASIC3

Microchip RTAX

SWaP-C

Frontgrade, the leading electronics space products provider and Lattice, the low power programmable leader are solving the space industry's need for efficient FPGAs

Frontgrade and Lattice

Why Our Partnership Matters

FRONTGRADE

- Leading dedicated space electronics provider
- 30 years space flight heritage
- Flight-proven space-grade QCOTS, QML-Q and QML-V processing flow assurance

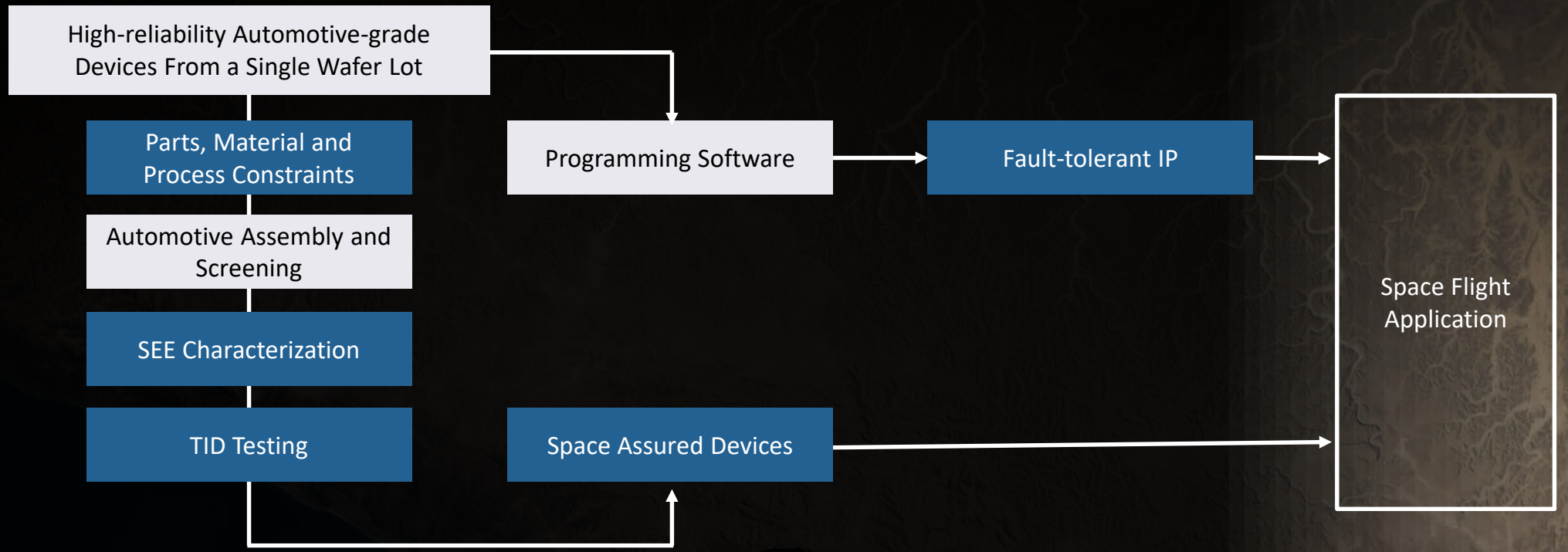
LATTICE SEMICONDUCTOR

- Low power programmable device leader
- 20 years automotive domain expertise
- Industry leading performance and reliability

Our proven space heritage and the latest commercially developed FPGA technology will supercharge next-gen services in support of government, civil & commercial missions

The Latest Commercially Developed Technology

For Space Missions



Lattice

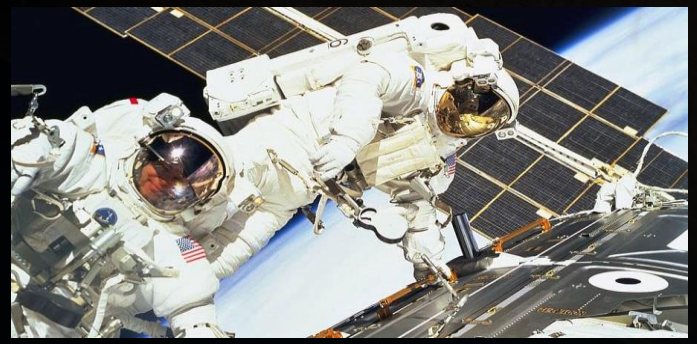
- FPGA based on inherently resilient 28nm FDSOI technology
- Design and manufacture commercial devices
- Specially built FPGA lots for radiation testing

Frontgrade

- Tightly coupled interaction with Lattice manufacturing & source
- Radiation assurance
- Augment SW with fault-tolerant libraries
- Device traceability

Engaging With Frontgrade

What We Are Delivering



- Space flight assurance
  - Packaging for flight: SnPb balling
  - Single wafer lot traceability
  - Radiation lot acceptance testing
  - Radiation reports
  - NASA out-gassing compliance
  - Flight assurance expertize
- Design-in and technical support from program start to finish
  - Development kits
  - Fault-tolerant IP
  - Easy access to engineering support
- Comprehensive HW and design SW ecosystem
- Long-term assured supply

Assurance

Inherently Radiation Tolerant FD-SOI Technology Upscreened For Space Flight

Our space flight heritage expertise adds assurance to the insertion of best automotive technology

Technology Assurance

- Total ionizing dose (TID) and single event effects (SEE) testing
- Thorough SEE testing and evaluation

Wafer/Die Integrity and Manufacturing Process Traceability

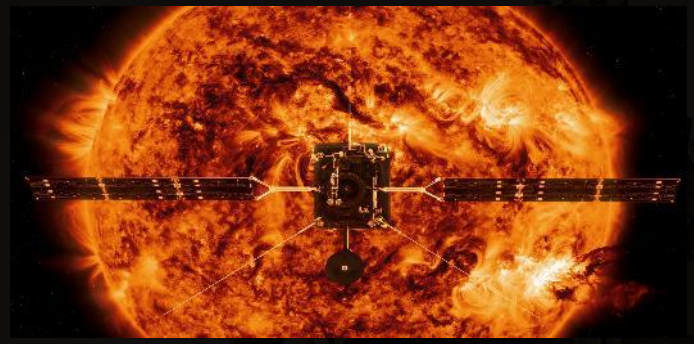
- Single homogenous wafer lot traceability from source to delivery
- Silicon design revision and fabrication process revision tracking

Data Sharing Transparency and Program Support

- Extensive characterization TID and single event fault interrupts, effects, gate rupture, upsets and latch-up data packs and analysis available
- Program support from start-to-finish from experienced space and FPGA experts
- QCI summary available with each lot

Better Technology

Radiation Resilient, SWaP-Efficient, High Performance



Reliable, fully depleted silicon on insulator (FD-SOI) fabrication technology is a planar process that is ideally aligned to modern space missions

Designed by Lattice, The Low Power Programmable Leader with the performance, features and bandwidth required for modern embedded processing

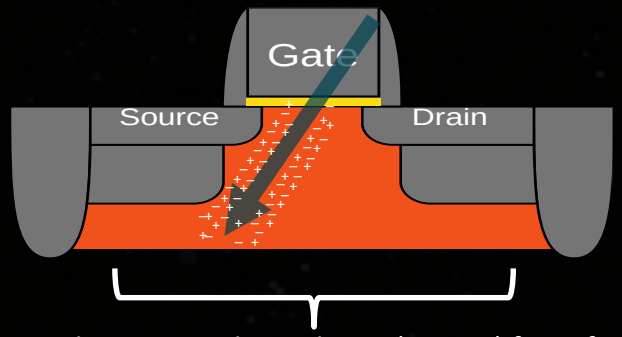
28nm technology provides greater processing density and reduced size, weight, and power consumption

Inherently radiation tolerant architecture minimizes SEUs, and is augmented with built-in error detection and correction features

FD-SOI Is Inherently Radiation Tolerant

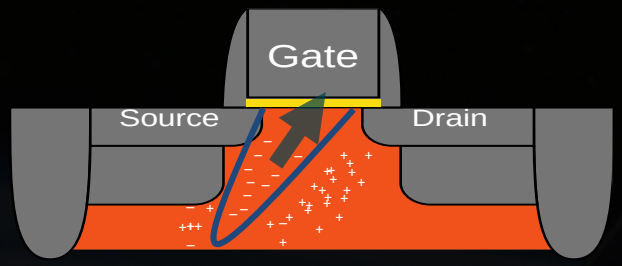
Effect of Ionizing Particles

Traditional FPGA on Bulk

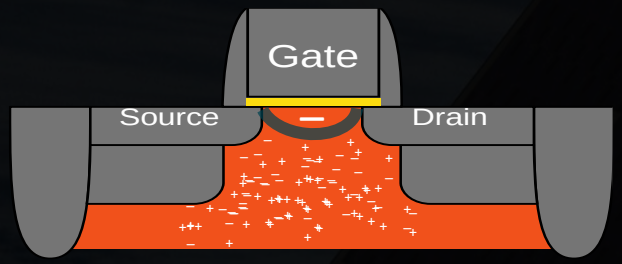


Critical transistor channel area (orange) for soft errors (several µm thick)

Radiation strike ionizes Si atoms, forming cylindrical track of electron hole pairs

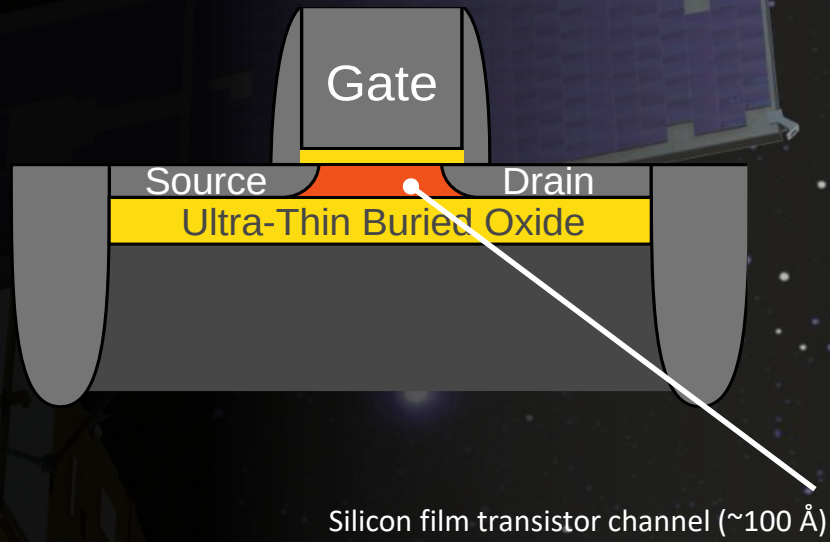


Funnel-shaped charge collection occurs



Charge collects into current pulse, state of charge inverts

FPGA in 28nm FD-SOI



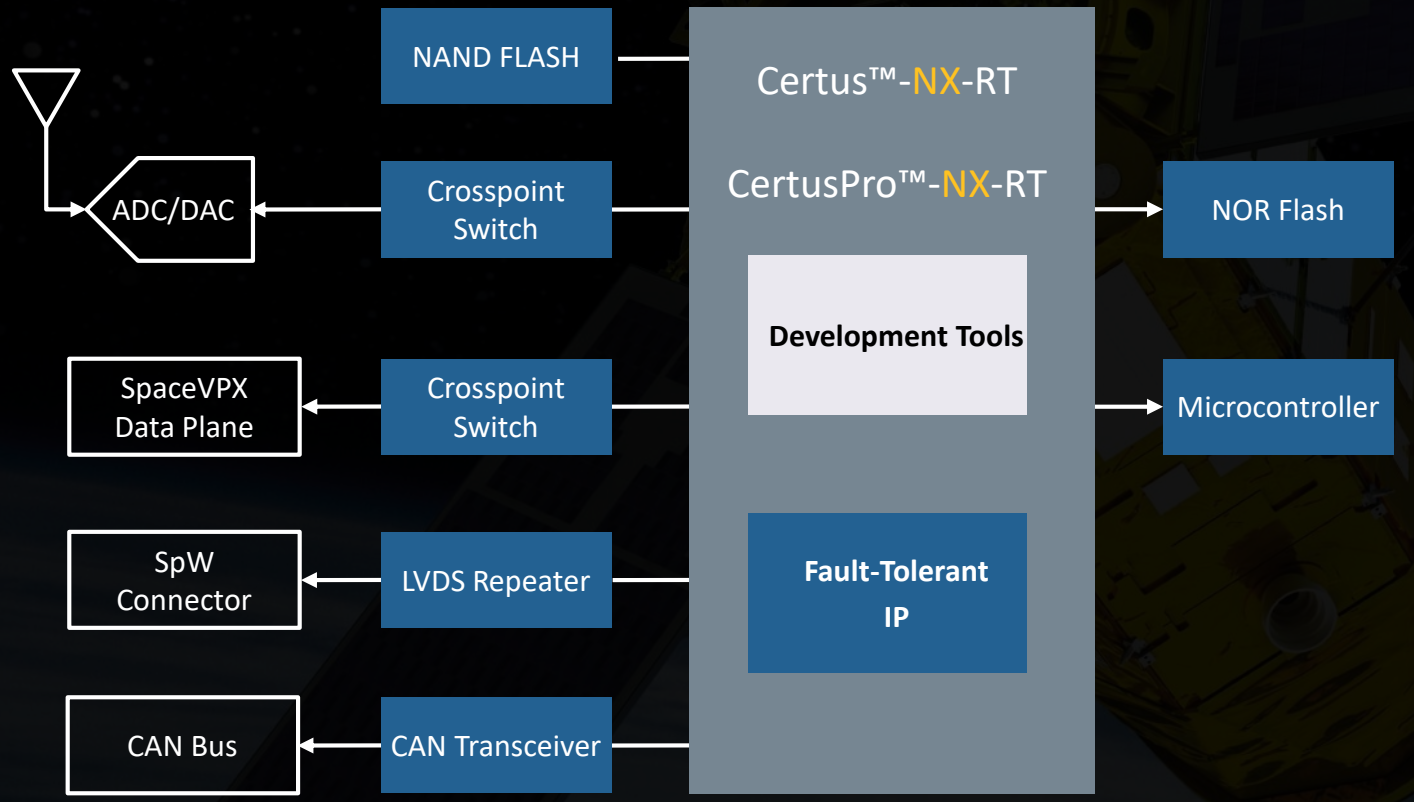
Silicon film transistor channel (~100 Å)

- Critical area significantly reduced, minimizing charge collection
- Built-in SEC (fabric SRAM) and ECC (EBR & large RAM) for added mitigation
- Greatly improved soft error rate (SER)

Comprehensive Ecosystem

Hardware

Full suite of SWaP optimized peripheral devices, all with space flight assurance



- Interoperable and proven
- Highest through-put and densities
- Reference design & engineering support
- Long-term assured supply

Certus™-NX-RT and CertusPro™-NX-RT

Filling the Performance / SWaP-C Gap For Distributed Satellite Processing

	Certus-NX-RT	CertusPro-NX-RT
Technology	28nm FD-SOI	28nm FD-SOI
Logic Cells	39K	96K
LUT4/Flip Flop	32.3k	79.9k
Embedded Memory	2.5Mb	7.3Mb
Supply Voltage (V)	1.0 Core, 1.8V Aux	1.0 Core, 1.8V Aux
Maximum Image Size (w/ max. LRAM & EBR)	8.807Mb	22.333Mb
I/O Voltage (V)	1.0 – 3.3	1.0 – 3.3
PLL	3	4
Primary I/O	LVDS, Soft D-PHY, SGMII, PCIe, GbE	LVDS, Soft D-PHY, SGMII, PCIe, 10GbE
SERDES	4 lanes	8 lanes
Supported Memory	DDR2/3L, LPDDR2/3 x8, x16	DDR2/3L, LPDDR2/3/4 x8, x16, x32, x64
Security	Bit stream encryption (AES-256) & authentication (ECDSA)	Bit stream encryption (AES-256) & authentication (ECDSA)
ADC	2x 1 MSPS, 12-bit SAR	2x 1 MSPS, 12-bit SAR
Typical Power (mW)	100	600
Size (mm)	14 x 14, 0.8 pitch	19 x 19, 0.8 pitch
Temp. (°C)	-40 to 125	-40 to 125
Packaging	Plastic package, SnPb balling (x256)	Plastic package, SnPb balling (x484)
TID (kRad (Si))	100	100
SEL immune (MeV-cm^2/mg)	≤80	≤80
Export Classification	EAR99	3A991.d

Two options to support your needs

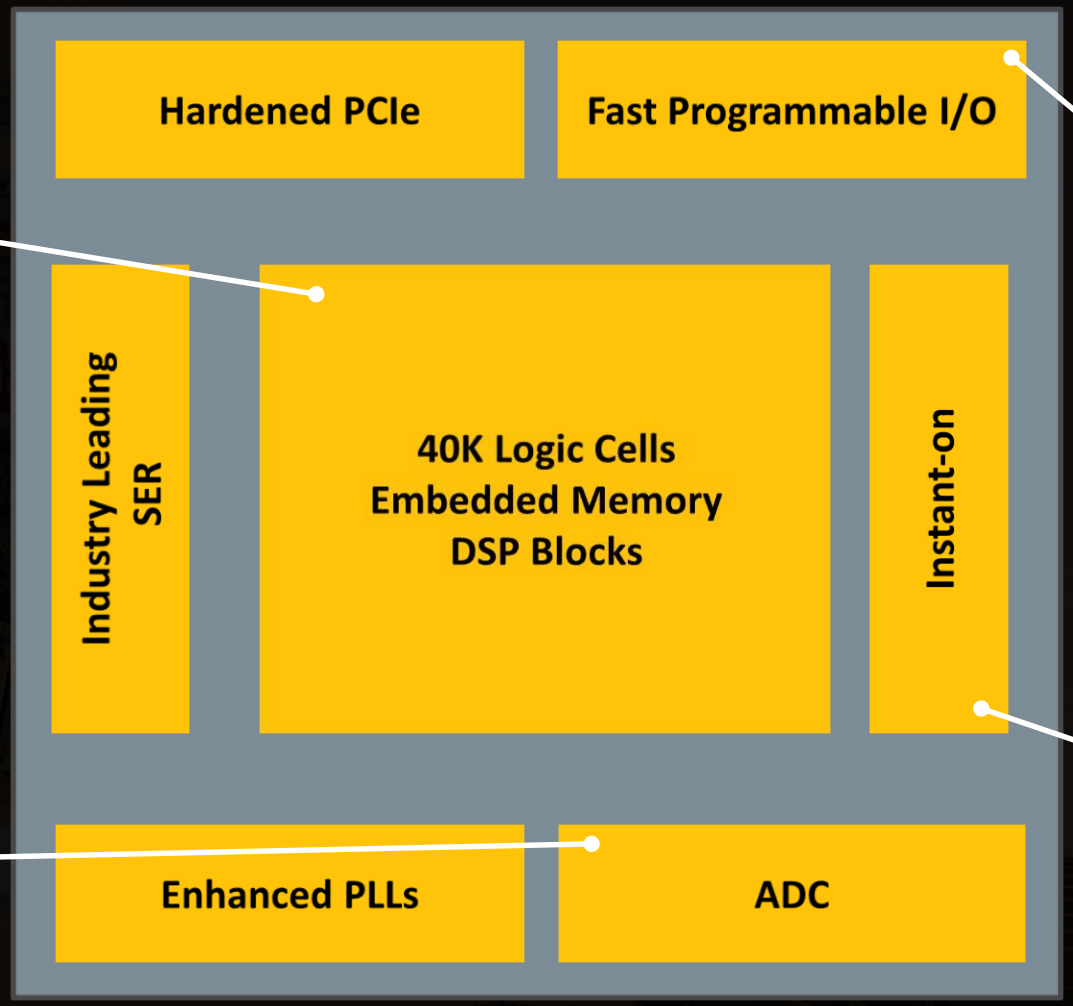
A Closer Look at Certus™-NX-RT

Reinventing the Low-Power General Purpose FPGA For Space

FRONTGRADE

Programmable Core

- Infinitely reconfigurable
- Low-power mode
- Industry-leading reliability
- High-performance mode
- High embedded memory count
- 56 SysDSP blocks



Fast Programmable I/O

- Diff I/O (1.5 Gbps)
- LVDS, subLVDS, SGMII
- DDR3 (1066 Mbps)
- 192 total I/O (118 at 3.3V)

Hard Macro Blocks

- One lane PCIe (5 Gbps)
- CDR for SGMII (1.25 Gbps)
- ADC

Instant-On

- 3 ms I/O config.
- 15 ms device configuration

A Closer Look at CertusPro™-NX-RT

Optimized For Embedded Edge AI Processing

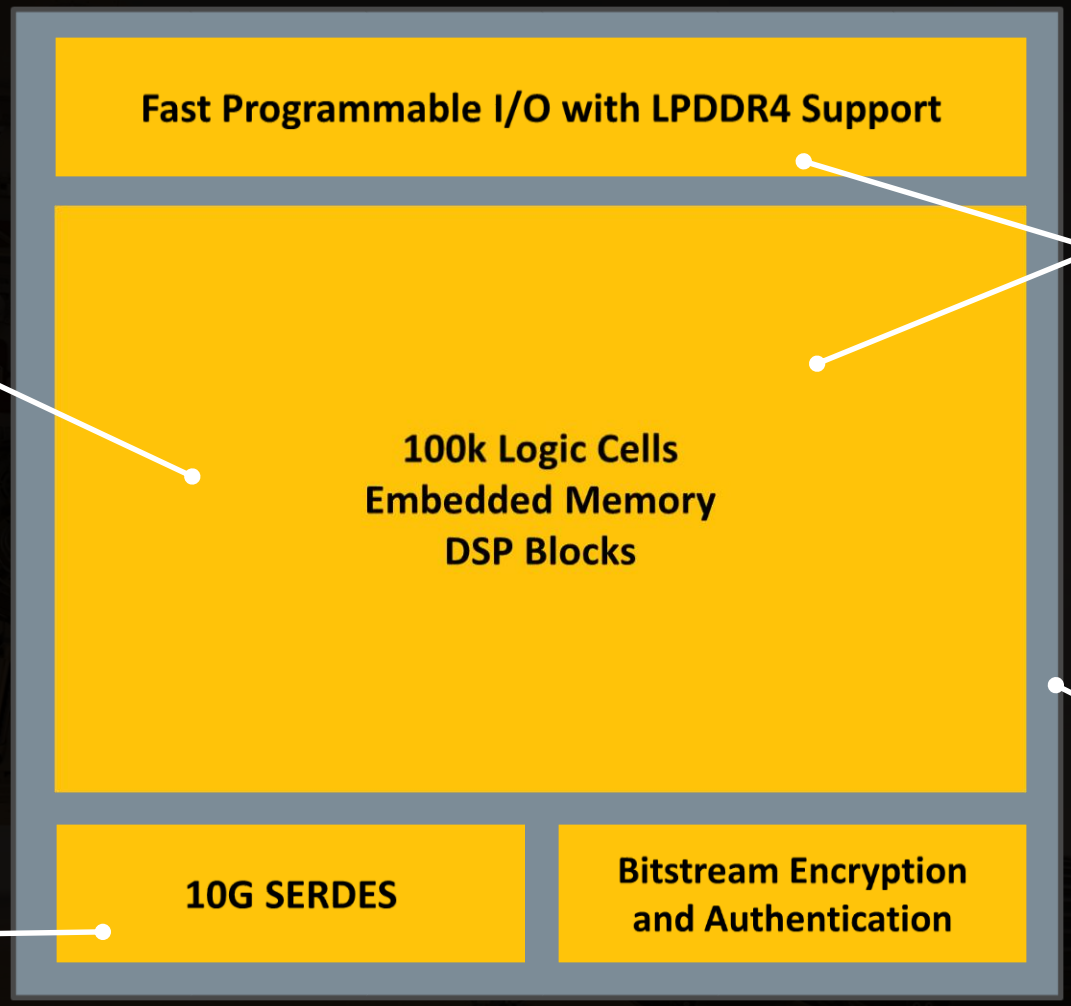
FRONTGRADE

Low Power FPGA Fabric

- Power efficient performance
- Built on FD-SOI technology
- Industry-leading reliability
- 100k logic cells
- 156 SysDSP blocks

High Bandwidth Interfaces

- 8 SERDES lanes up to 10 Gbps
- Flexible multi-protocol PCS
- Supports 10GE, PCIe Gen 3 and more



Optimized For Edge Processing

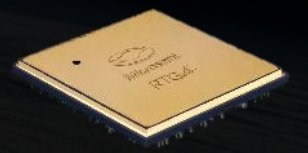
- DSP, LRAM and EBR
- 7.3 Mb on-chip memory
- LPDDR4, DDR3 (1066 Mbps)
- ADC
- 305 total I/O (167 at 3.3V)
- 4ms I/O configuration
- 30 ms device configuration

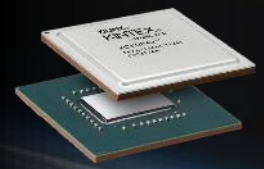
Small Form Factor

- 19 x 19 mm package

Space Grade FPGAs

FD-SOI Delivers Better SWaP Performance For Processing Closer To The Data Source





	Microsemi RT ProASIC3	NanoXplore NG-MEDIUM	Frontgrade / Lattice Certus-NX-RT	Frontgrade / Lattice CertusPro-NX-RT	Microsemi RTG4	Microsemi PolarFire	Xilinx KU060
Footprint (mm^2)	576	841	196	361	1,764	1,600	1,600
	24 mm	29 mm	14 mm	19 mm	42 mm	40 mm	40 mm
Typical Power (mW)	1,250	1,500	100	600	9,000	5,000	10,000

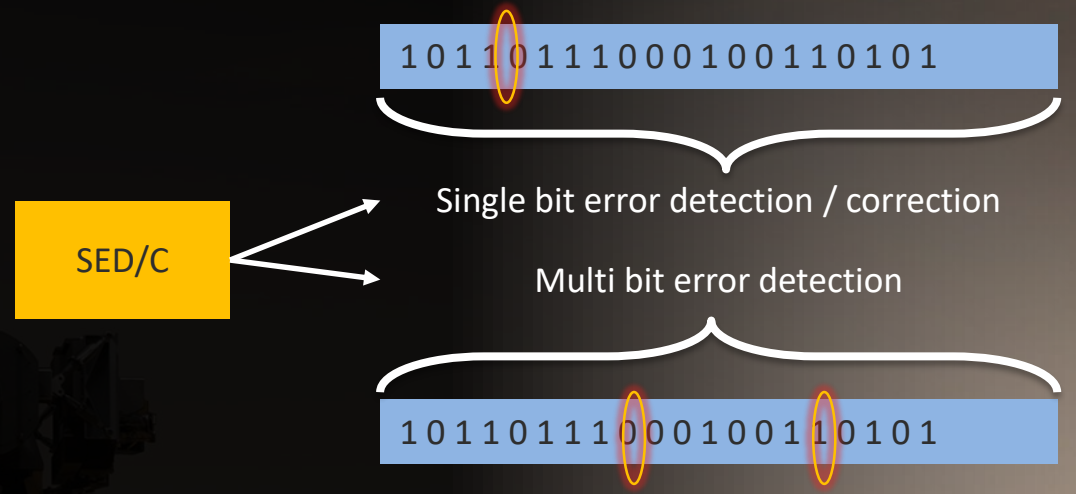
Competitive Features

	RT ProASIC3	RTAX	NG-Medium	Certus™-NX-RT UT24C407	CertusPro™-NX-RT UT24CP1008	RTG4
Logic Density	14K	25K LE	35K	39K LC	96K LC	150K
Embedded Memory(Mb)[1]	0.1	0.16	2.7	2.5	7.3	5.2
18 x 18 Multipliers	N/A	N/A	112	56	156	462
I/O Count	270	418	192-374	192	305	720
SERDES	N/A	N/A	N/A	x1 PCIe Hard IP(5G) X2 SGMI (1.25G)[2]	8 x 10Gbps	24 x 3.125 Gbps
Configuration / Security	139nm Built-in Flash	150nm, Antifuse(OTP) RHBD	External Flash	External Flash (with instant-on) / AES-256, ECDSA/HMAC	External Flash (with instant-on) / AES-256, ECDSA/HMAC	65nm Built-in Flash RHBD
Key Features	1Mb flash ROM, DPA	SEU hardened registers, 5V tolerant I/O	Embedded Spacewire	Lowest power, Smallest package with PCIe & GigE, EDAC	PCIe Gen III, LPDDR4, SGMII, EDAC	SEU hardened register, EDAC, DDR3
Package[3]	B, E class CCGA484 -40 to 155C Temp	B, V class CG624 -40 to 155C Temp	CQFP352, CCGA 625,	256 BGA 0.8mm – 40 to 125C Temp	484 BGA, 0.8mm -40 to 125C Temp	B, V class CCGA1657, -40 to 155C Temp
Static Power	134mW	240mW	871mW	87 mW	220mW	3900mW
DFF operating saturated cross-section	$2x10^{-7}$	$1x10^{-7}$	$5x10^{-9}$	$2.7x10^{-8}$	$2.7x10^{-8}$	$2x10^{-8}$
TID	25krad	200krad parametric, 300krad functional	100krad	100krad parametric, 200krad functional	100krad parametric, 200krad functional	200krad parametric, 300krad functional
SEL	Estimated at 68MeV	Immune to 117 MeV	Immune to 60MeV	Immune to 80MeV	Immune to 80MeV	Immune to 103MeV

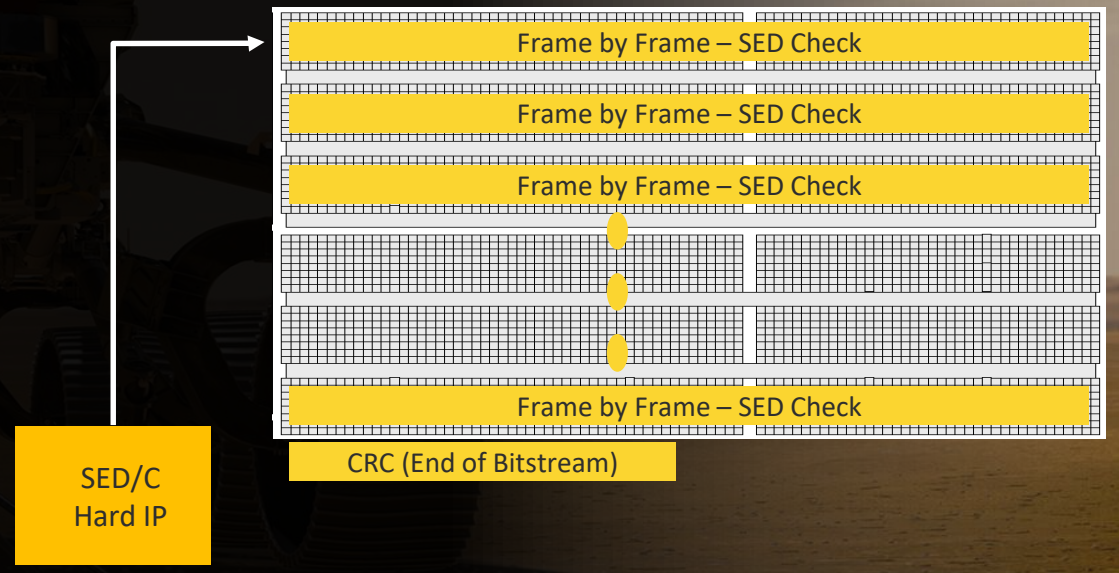
Soft Error Detection and Correction

Certus™-NX-RT and CertusPro™-NX-RT

- Built-In Error Detection and Correction On All Embedded Memory Bits
- Dedicated hard logic to detect soft errors
- Frame by frame SED check
- Single and multi-bit error detection
- Frame level single bit error correction
- Programmable SED clock with wider clock frequency option
- Soft error injection (SEI) tool available in Radiant



- Two levels of SED check
  - Level 1: Frame level
  - Level 2: Bitstream level
- Frame by Frame SED check
- CRC at the end of bitstream
- Correction using ECC for single bit error
- Multi-bit error detection only
- Report out error location of error frame
- Report out bit location inside the error frame

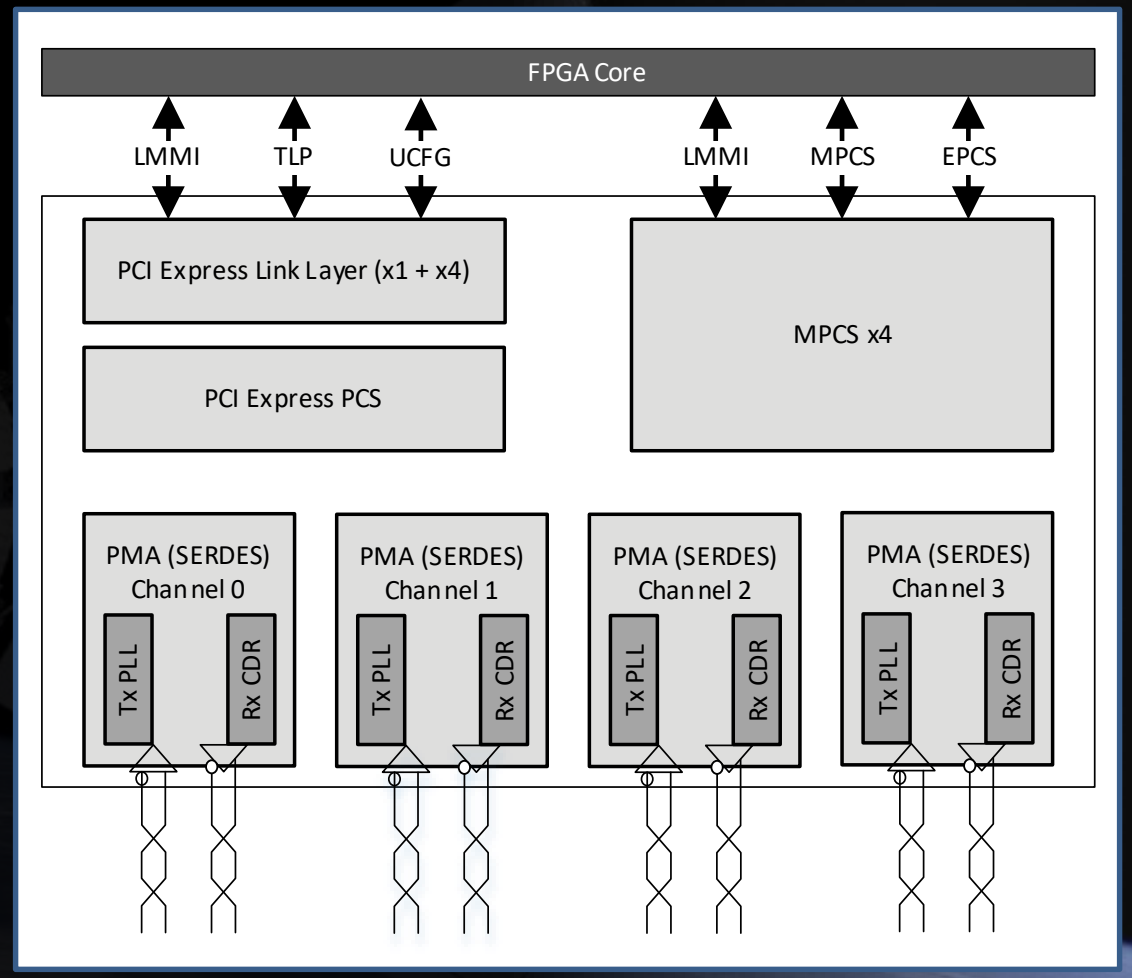


SerDes Quad

CertusPro™-NX-RT

- CertusPro-NX-RT SerDes/PCS Quad includes
  - Four PMA channels
  - One PCIe PCS
  - One MPCS
  - One PCI Express Link Layer(X4+X1) (Only for the left-most Quad)
- PCI Express PCS is designed for PCI Express only
- MPCS is designed for general protocols
- Below table shows the different mode for the SerDes/PCS feature combination

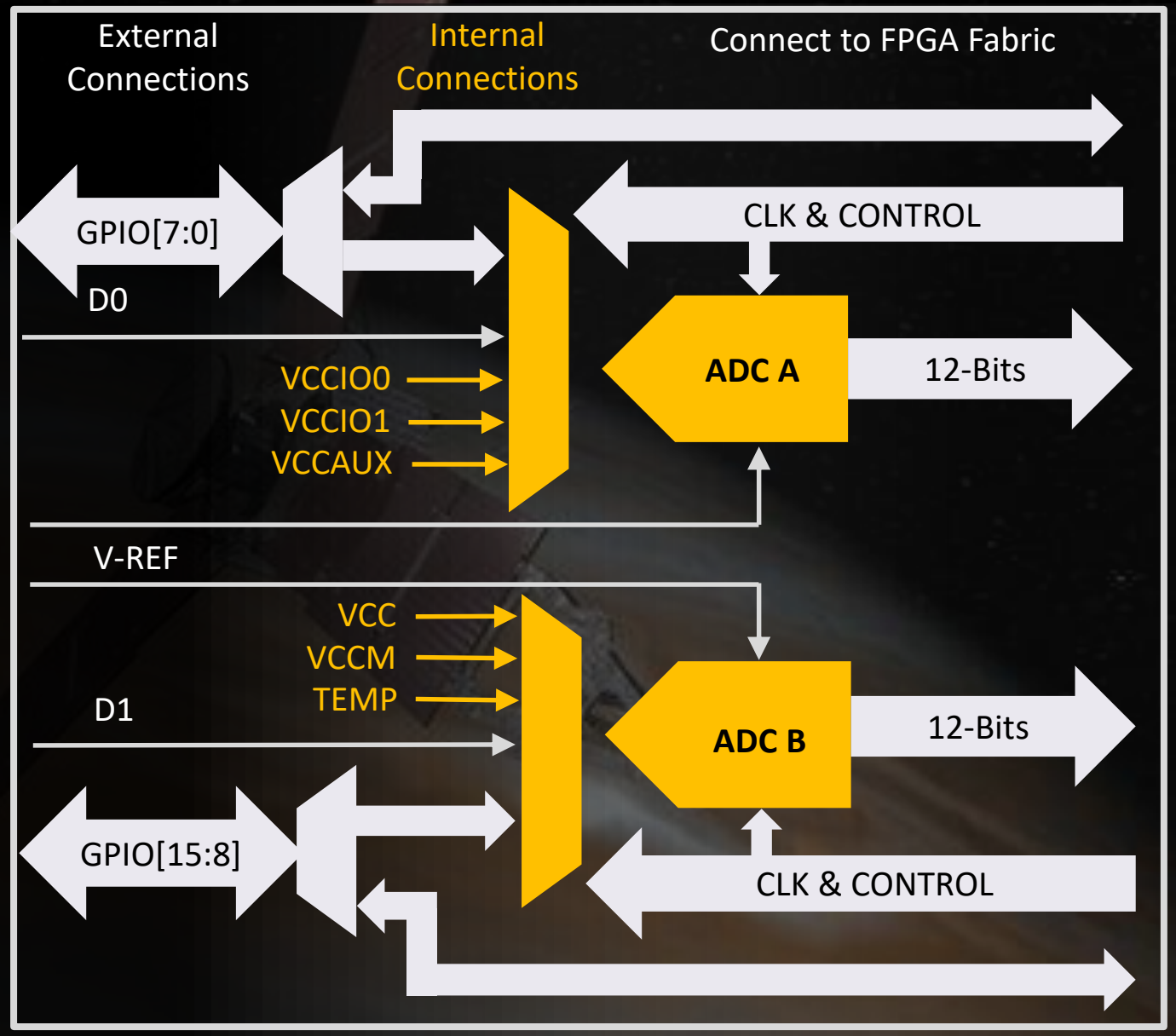
SerDes/PCS Mode	PCI Express	MPCS	PMA Only	PIPE
PMA	√	√	√	√
PCI Express PCS	√	bypass	bypass	√
PCI Express Link Layer Quad	√			
MPCS		√		



Embedded ADCs

CertusPro™-NX-RT

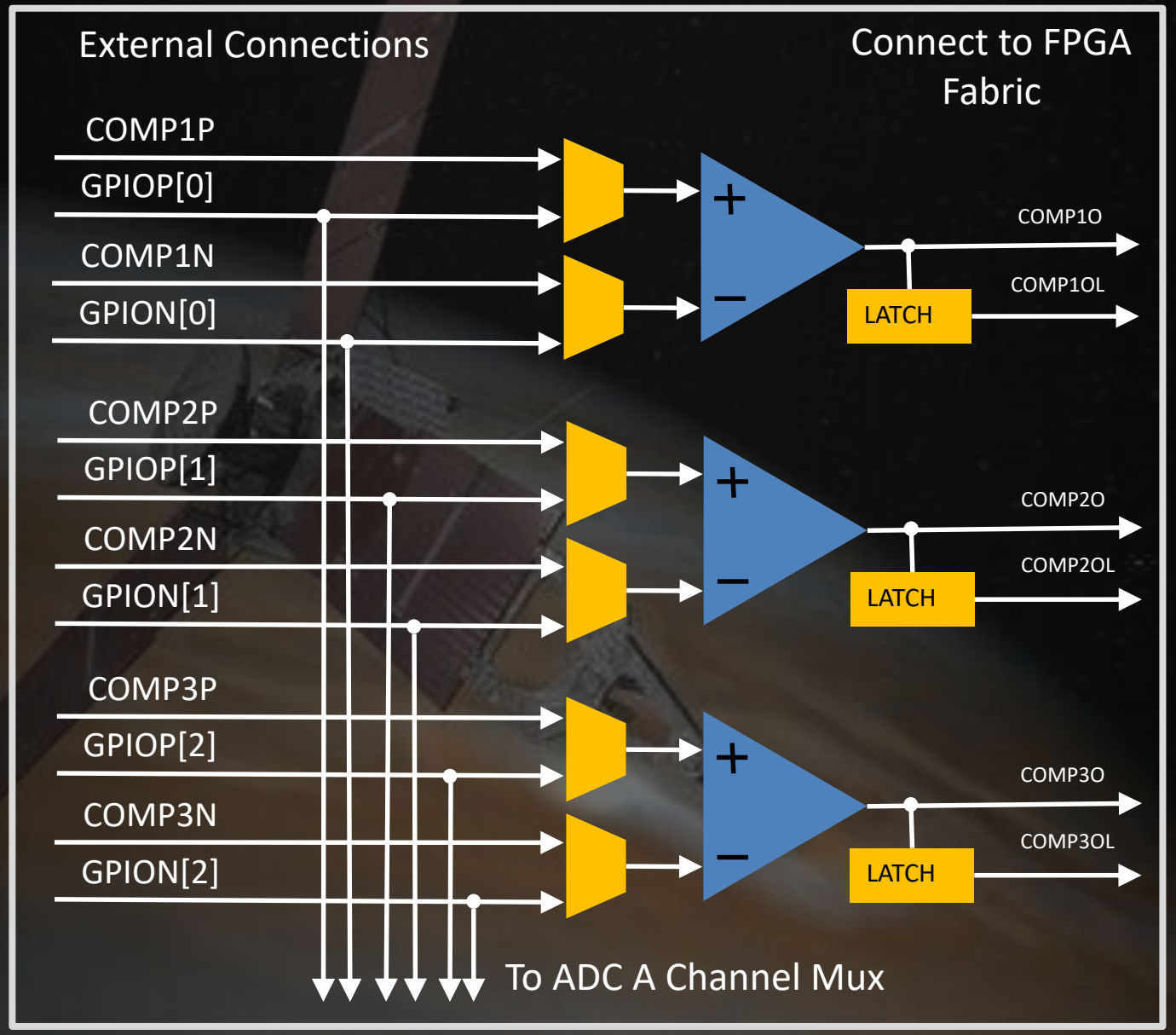
- Built-In Analog Features For Mixed Signal Sensing and Processing
- 2x (independent) ADCs per device
  - 1 MSPS, 12-bit SAR
- Simultaneous sampling
- 18 differential analog inputs
- 5 internal voltage rail inputs
- One internal temperature input
- Requires external V-Ref
  - 1.2 to 1.8 V



Embedded Comparators

Certus™-NX-RT and CertusPro™-NX-RT

- Three continuous-time comparators
  - Shared GPIO to ADC A or,
  - Independent Analog Inputs
- Real time or latched outputs
- Requires external reference to compare with input signal
- For Telemetry, fault detection, level sensing and more



Clocks - Resources and Routing

Certus™-NX-RT and CertusPro™-NX-RT

High Performance Clock Distribution:

- Up to 64 Primary Clocks
- Four edge clocks per bank at bottom of device.
- Total 12 edge clocks.
  - Low Skew, high speed clock resources for I/O Logic

Efficient clock logic modules:

- Clock dividers, Dynamic clock select, Dynamic clock control

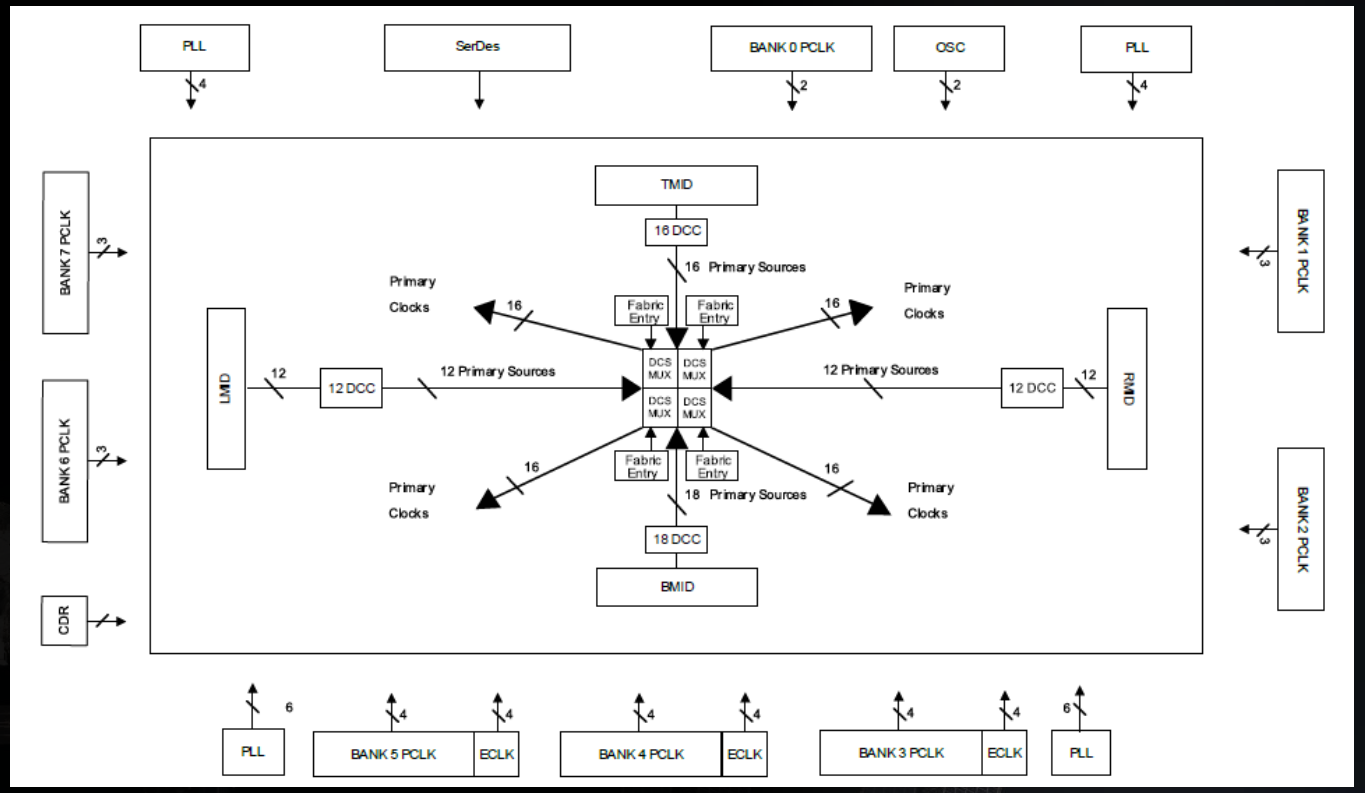
sysCLOCK PLL:

- 3 PLLs in C-NX-RT, 4 PLLs in CP-NX-RT

2 DDR DLL for DDR memory and HP IO

Internal Oscillators

- One high frequency and one low frequency clock osc

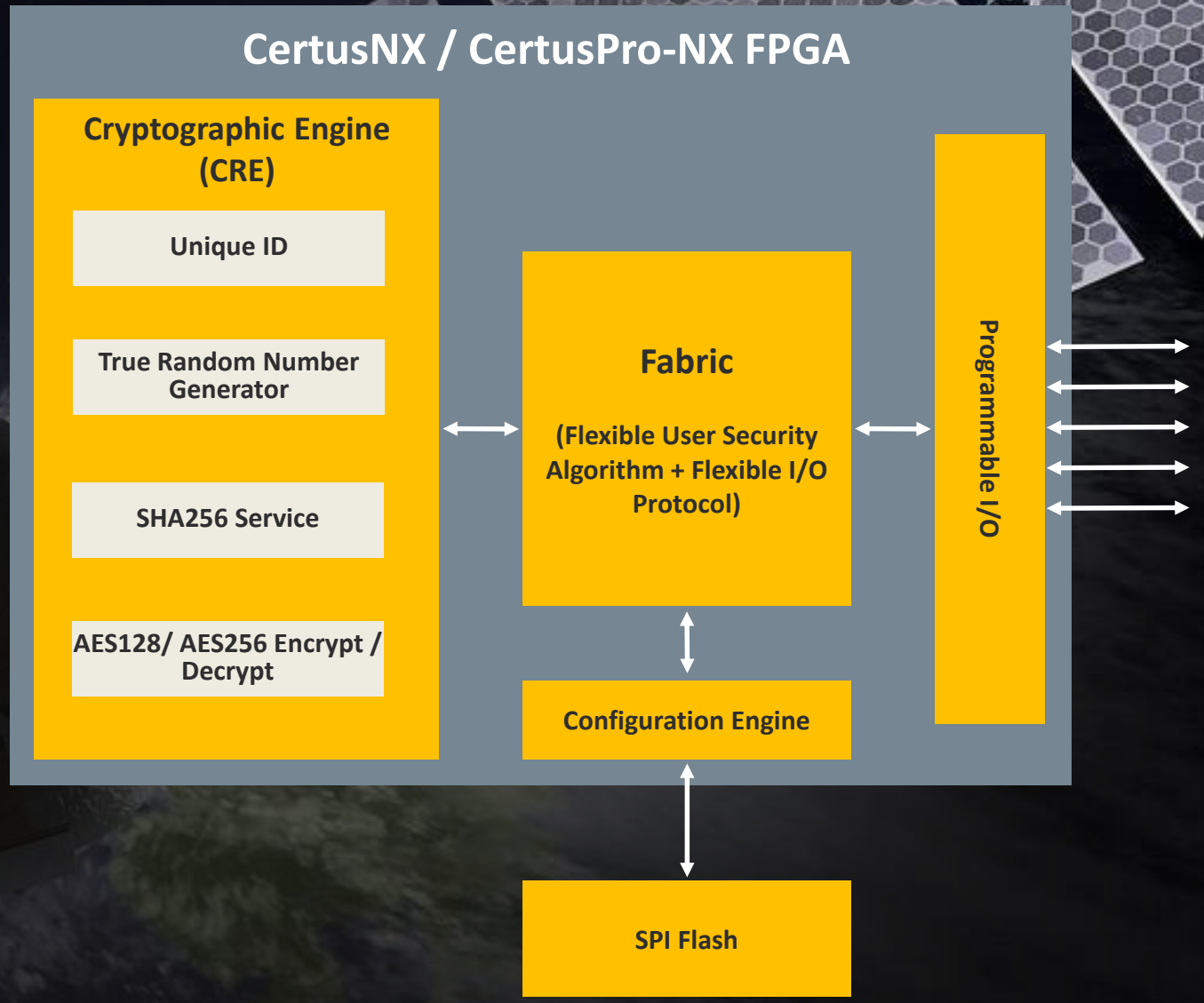


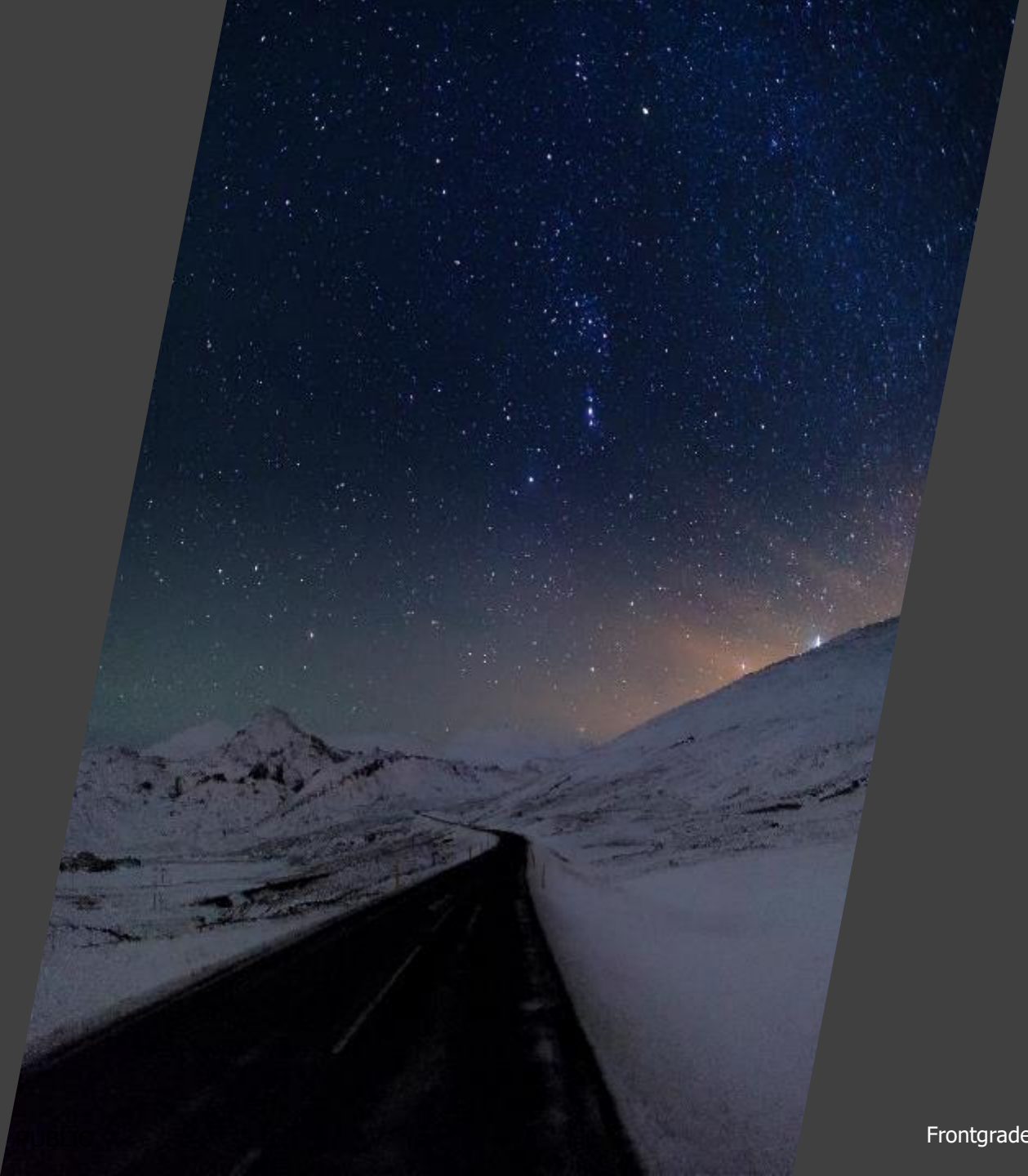
Security Features

Certus™-NX-RT and CertusPro™-NX-RT

Built-in bitstream encryption and authentication for system integrity

- Bitstream security
  - ECDSA256 authentication
  - AES256 encryption
  - Radiant support enabled by default
- User mode security features
  - Access CRE functions thru fabric (using CRE IP)
  - Radiant support enabled upon request (under license control)
  - Unlimited reprogramming cycles





FRONTGRADE

Support Hardware & Tools

Comprehensive Ecosystem

Hardware, Software, Design Tools, IP

Devices

Certus™-NX-RT

FPGA Devices

- Flight devices
- Application Engineering Support
- Radiation reports
- Reliability and TCI summaries

Holistic SW, HW, Radiation Technical Support

- Frontgrade
- www.Frontgrade.com

Design Tools

Lattice Radiant

Lattice Radiant® design SW

- Easy design navigation and debugging
- Powerful optimization tools that feature best in class algorithms
- Precise analysis tools for design, timing, and power analysis
- Complete closed-loop cross probing from physical to logical design implementation

SW Technical Support

- Frontgrade
- Extensive support at: www.Latticesemi.com

IP Libraries

Frontgrade GRLIB

GRLIB FT-FPGA IP library with fault-tolerance features

- LEON series (UT700, GR712RC, and GR740) & NOEL-V RISC-V processors
- System peripherals
- Reference designs
- Communication controllers, including SpaceWire and SpaceFibre
- Cryptography accelerators

SW Technical Support

- Frontgrade
- www.Gaisler.com

Lattice Propel

Propel – Analysis, compile and debug tools

- Includes Propel SW Dev. Tools and Propel Builder
- High productivity HW/SW debugging
- Drag and drop IP instantiation
- Correct by construction design methodology

SW Technical Support

- Frontgrade
- Extensive support at: www.Latticesemi.com

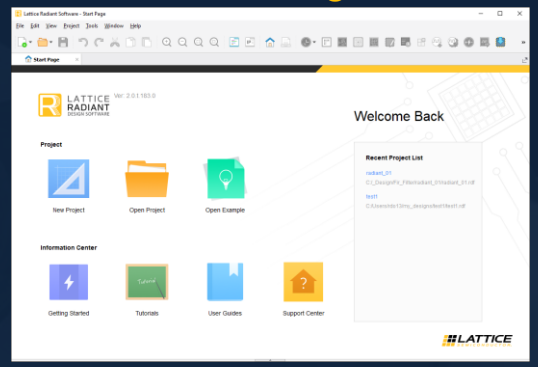
Lattice Radiant

Intuitive and Easy Design Experience

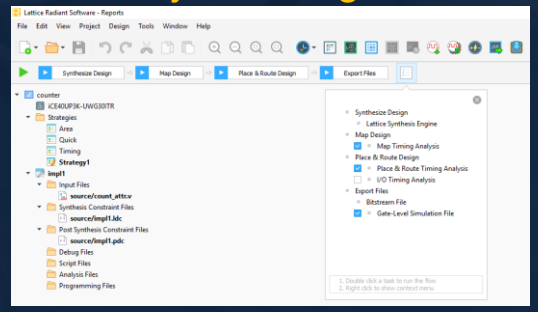
Small-Fast Download & Installation

Easy Navigation

Start Page



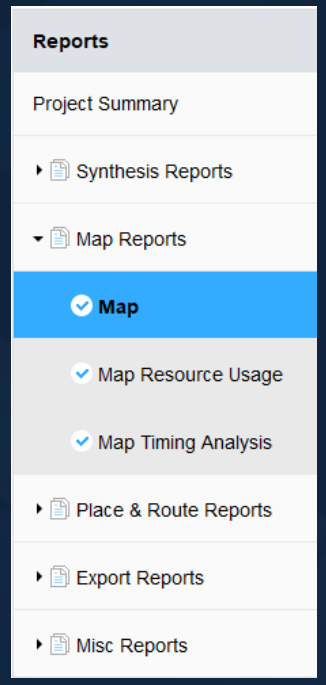
Project Navigator



1-Click Execution

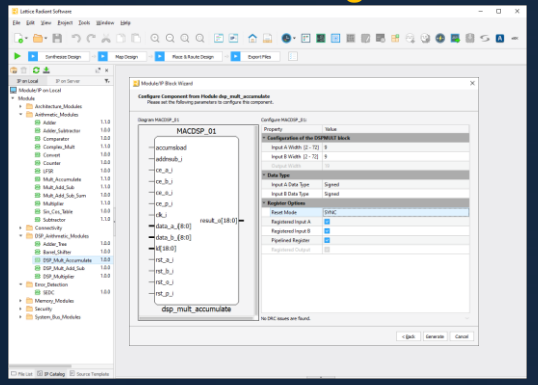
Execution Toolbar

Report Panel

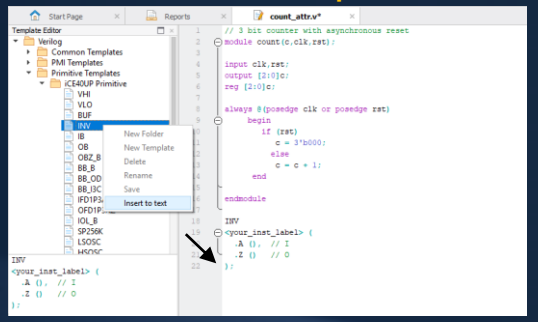


Intuitive IP Assembly

IP Catalog



Source Template



GRLIB Support

Certus™-NX-RT and CertusPro™-NX-RT

Milestone	Q1	Q2	Q3	Q4
Description	Initial support	GRLIB COM support Experimental FT-FPGA support	GR740-MINI board Space SoC reference design	GRLIB FT-FPGA support Lattice Propel integration
Functionality	Complete technology mapping and project file generation support.	Timing optimizations of GRLIB IP for Lattice FPGAs. Validation of processor IP on Lattice Nexus FPGAs PRE-built bitstreams: LEON3 - Certus™-NX Versa LEON3 - CertusPro™-NX.	GR740-MINI board with pre-built bitstream for CertusPro™-NX.	TENTATIVE- subject to execution of SEE test campaigns Design recommendations for radiation mitigation of SoC designs in Lattice FPGAs. Lattice Propel integration of standalone IPs
IPs available (area figures in grlib_area)	CAN, SPIMCTRL, FTMCTRL, SpaceWire, GR1553B	LEON3, GRHSSL, GRPCI2		NOEL-V (MC32 configuration)
Template designs	LEON3 in CrossLink-NX Evaluation Board LEON3 in Certus™-NX Versa Evaluation Board	LEON3 in CertusPro™ Versa Evaluation Board	FPGA reference designs showing guidelines for a traditional SoC system for space applications. SoC for GR740-MINI board	NOEL-V in CertusPro™ Versa Evaluation Board

Evaluation Boards

Certus™-NX-RT and CertusPro™-NX-RT

Certus™-NX-RT

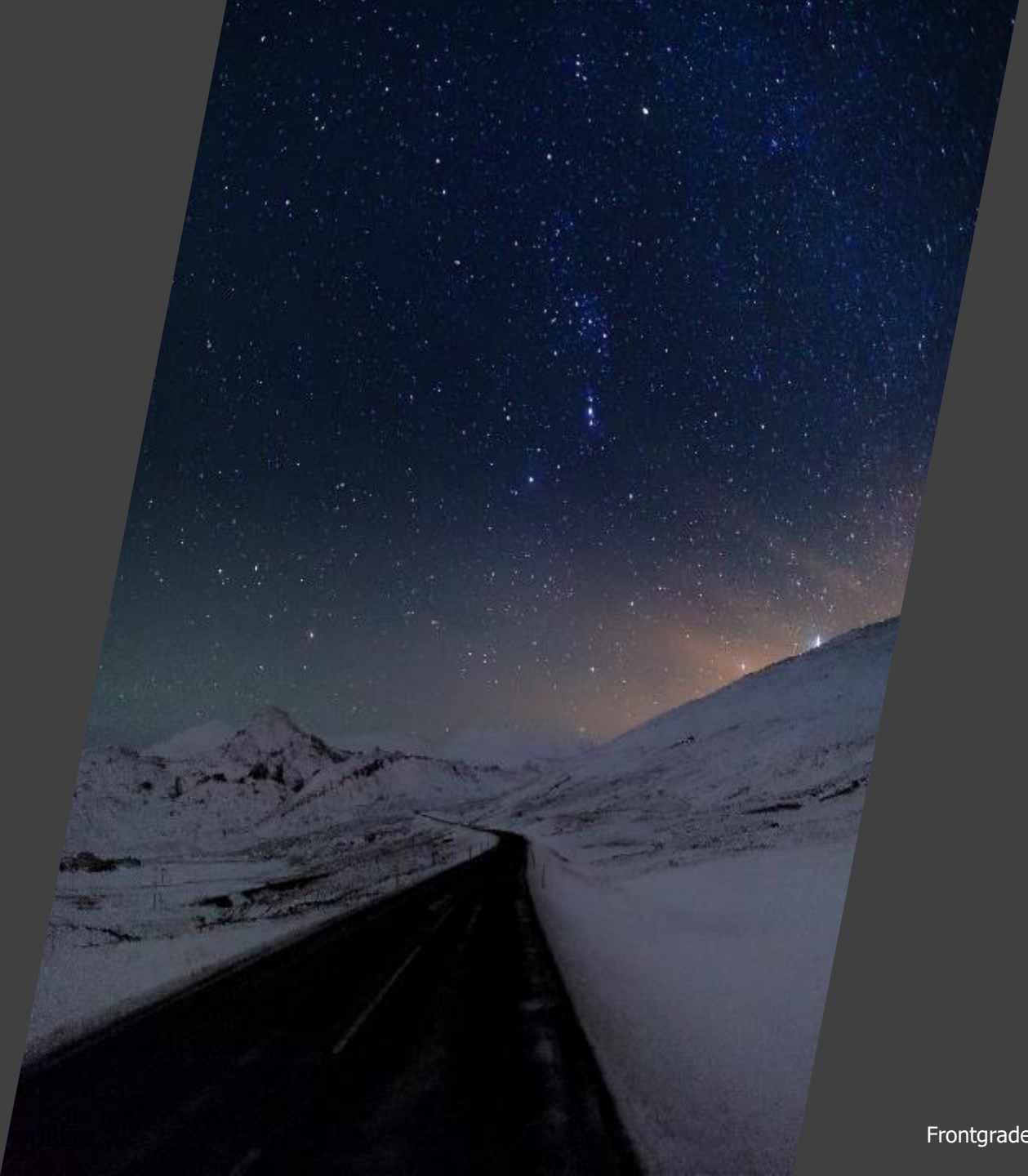
Adiuvo Space Development board
PMOD, Raspberry PI Pico

Lattice Versa Board
DDR3, Ethernet, PCIe

CertusPro™-NX-RT

Lattice Evaluation board
Easy access to I/O and SerDes

Lattice Versa Evaluation board
LPDDR4, 10G Ethernet, 1G Ethernet, PCIe

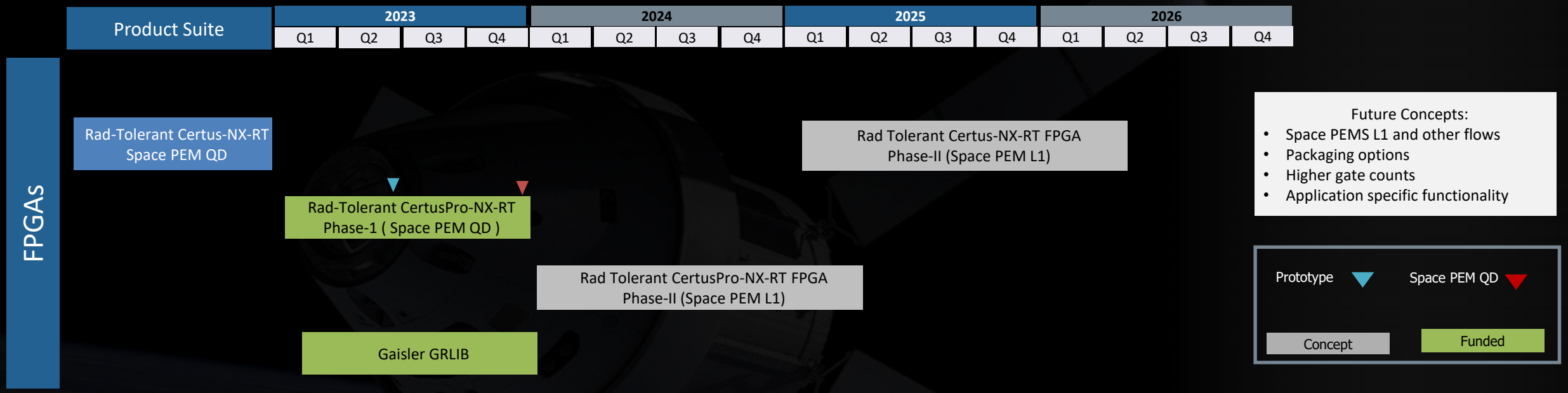


FRONTGRADE

Roadmap

Certus™/Pro-NX-RT FPGAs

Roadmap and Introduction Schedule



Certus-NX-RT

- Space Grade Automotive Parts Shipping NOW!
- Evaluation Boards – Available NOW !
- Radiation & Outgassing Reports Available

CertusPro-NX-RT

- Q1 2023: Industrial grade devices
- Q1 2023 : Evaluation Boards
- Q4 2023: Space grade (Characterized purpose built lots)
  - Will include ATE test bring up to characterize TID in depth

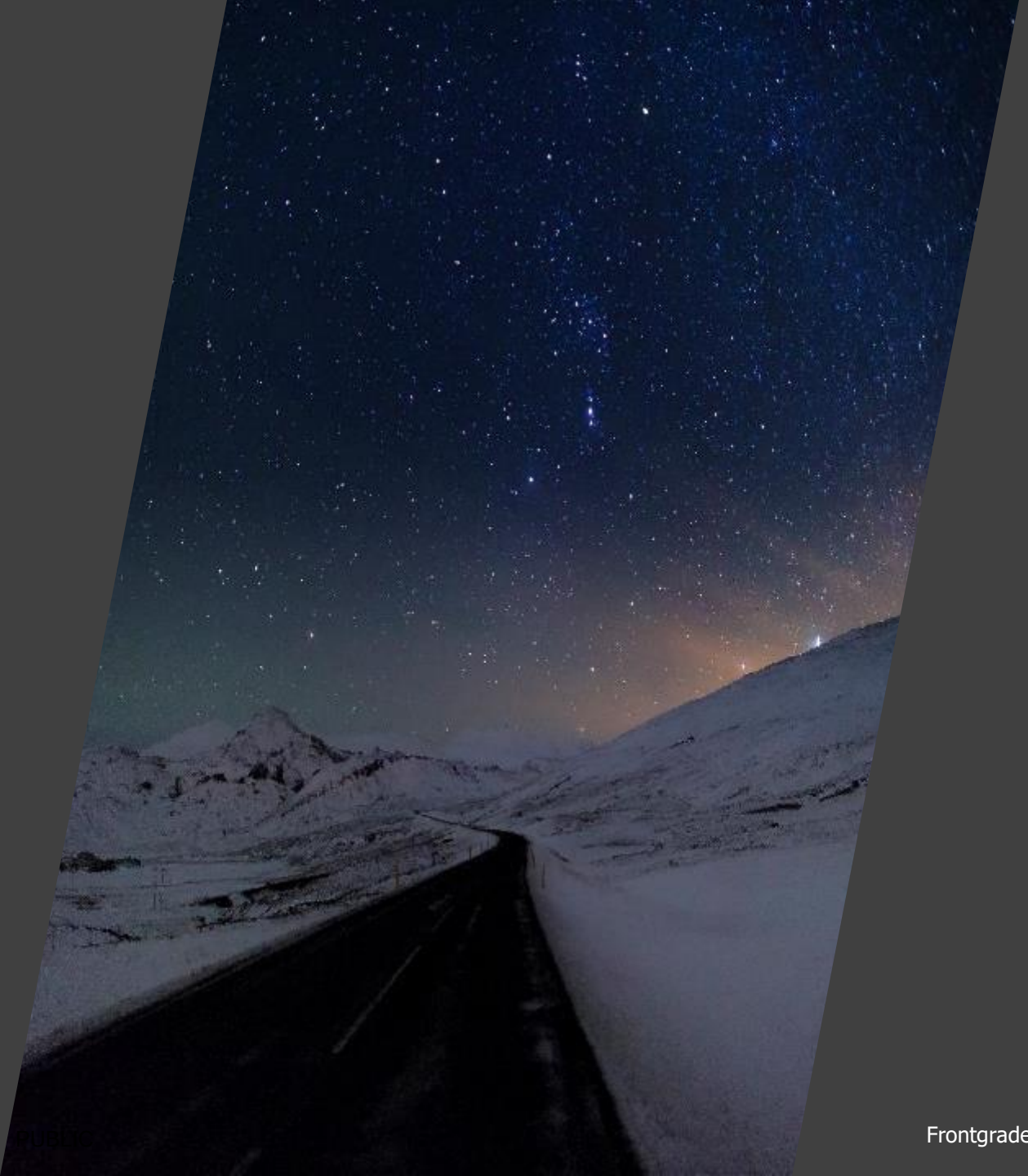
Frontgrade FPGA’S

Certus™-NX-RT and CertusPro™-NX-RT

Features	Lattice Automotive Grade	FRONTGRADE – Space PEM QD	FRONTGRADE – Space PEM L1
Baseline Electrical Performance & Qualification & Reliability Monitors	✓	✓	✓
Parts Material and Process Control agreement		✓	✓
Single Wafer lot Traceability		✓	✓
In-line Tin Lead Solder balling assembly		✓	✓
Outgassing reports		✓	✓
DPA Report		✓	✓
SEE Report		✓	✓
TID Radiation Lot acceptance testing per wafer lot		✓	✓
Temp Cycling			✓
X-Ray and CSAM			✓
Burn-In			✓
Multi-Temp Electrical Testing			✓
Added Qual Activity			✓

Screening Flows - Abbreviated

		PEM-INST-001	ECSS-Q-ST-60-13C	FRONTGRADE SOLUTIONS	
Operations	**Specification or Standard**	**Level 1**	**Grade 1**	**Space PEM L1**	**Space PEM QD**
Single Wafer Lot Source	Internal/Vendor Specification			✓	✓
Temp Cycle	MIL-STD-883 TM1010 (-65°C to +150°C)	Cond B (or at manufacturer storage temp range, whichever is less); 20 cycles	10 Cycels @ Cond B (or at manufacturer storage temp range, whichever is less); 20 cycles	JESD22 A104; 20 cycles	Optional
Radiography	MIL-STD-883 TM2012	✓	✓	✓	Optional
Pre BI Electrical Test	Per Device Specification	25°C, Min, and Max	+25°C	25°C, -40°C, and 125°C	
Dynamic Burn-in	MIL-STD-883 TM1015	✓	✓	Per device specification	
Interim Electrical Test	Per Specification (+25°C)	✓		25°C, -40°C, and 125°C	
Static Burn-in (I or I/II)	MIL-STD-883 TM1015	✓		✓	
Final Electrical Test (+25°C)	Per Specification (+25°C)	✓	✓	✓	✓
Delta	Per Specification	✓		Per device specification	Per device specification
Cumulative PDA		5%		5%	
Final Electrical Test (Max Temp)	Per Specification (Max Temp)	✓	✓	✓	✓
Final Electrical Test (Min Temp)		✓	✓	✓	✓
External Visual	MIL-STD-883 TM 2009	✓	✓	✓	✓



FRONTGRADE

Radiation & Reliability

Presenter: Brian Baranski – Systems Architect

Radiation Test Team & Locations

Certus™-NX-RT

Team

Melanie Berg : Principal Investigator , Scott Linton : Test Engineer, Matt Von Thun : Radiation Effects
Brian Baranski : Systems Architect

Heavy Ion

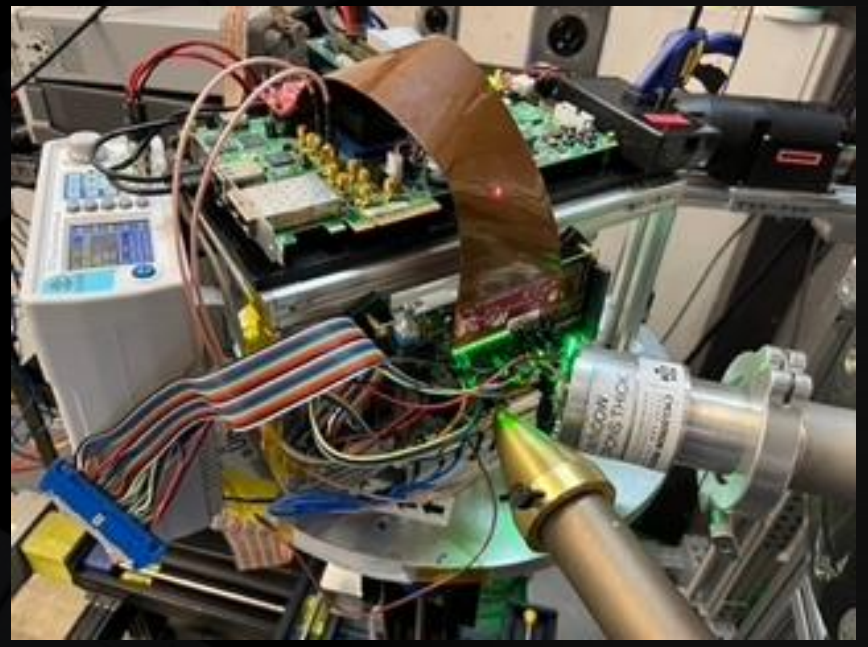
Texas A&M K500 Cyclotron 15MeV (05- Aug-2022)
Texas A&M K500 Cyclotron 15MeV (17-Nov-2022)

Proton

James M. Slater MD Proton Center, Loma Linda (17-Sep-2022)

Total Ionizing Dose

Radiation Test Solutions, Colorado Springs (30-Nov-2022)



SEL Testing at Texas A&M

Test approach

NASA Electronics Parts and Packaging (NEPP) FPGA SEU Test Guidelines:
https://nepp.nasa.gov/files/23779/fpga_radiation_test_guidelines_2012.pdf

Radiation Test Group

Data shared during the February 2023 Consortium meeting chaired by Sandia

Heavy Ion Testing

Certus™-NX-RT

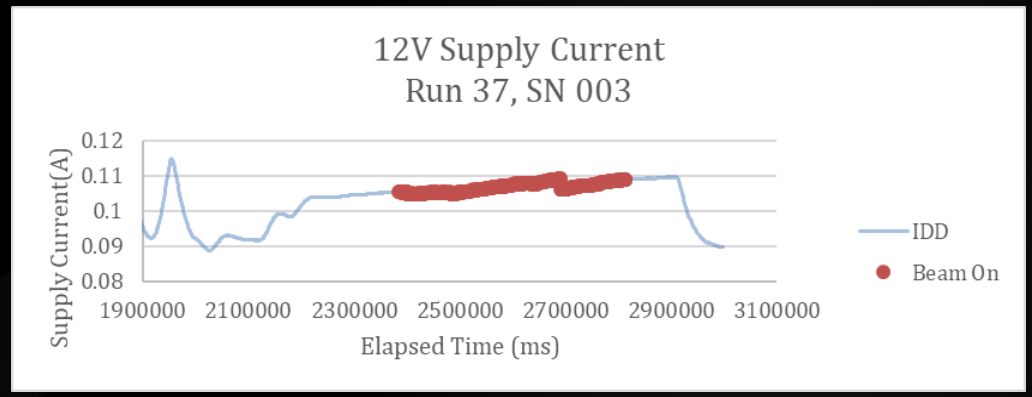
- Devices were irradiated with Xe, Kr, Ar, Ne, N ions at angles between 0 and 45 degrees with effective LETs ranging from 1.35 to 88.6 MeV·cm^2/mg
- SEL immunity was verified at 125˚C at max voltages to 80 MeV·cm^2/mg
- Full report contains cross-sections for each of the below tests:
- Single Event Failure cross-section characterized on four designs:
  - Windowed Shift Register (WSR)/PLL
  - PCIe
  - ADC/Comparator
  - DDR3
- Single Event Upset cross-section characterized for:
  - Configuration Memory (CRAM)
  - Embedded SRAM (without EDAC)
  - Shift registers DFFs
- PCIe design was evaluated with and without the scrubber

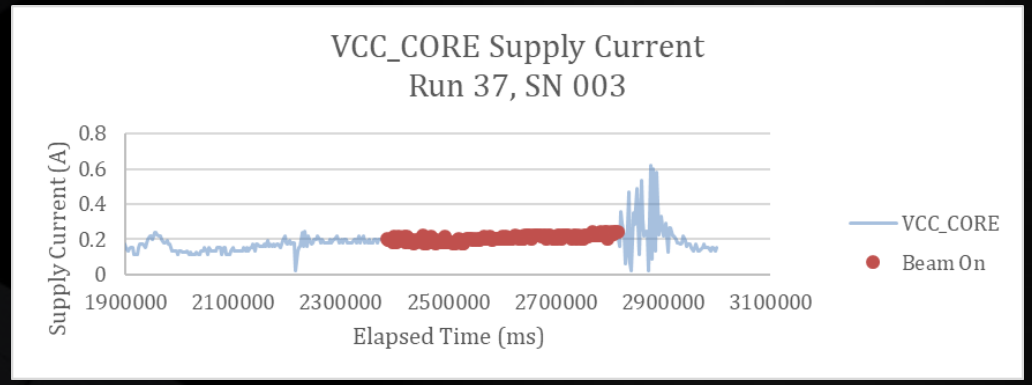
SEL Test Data

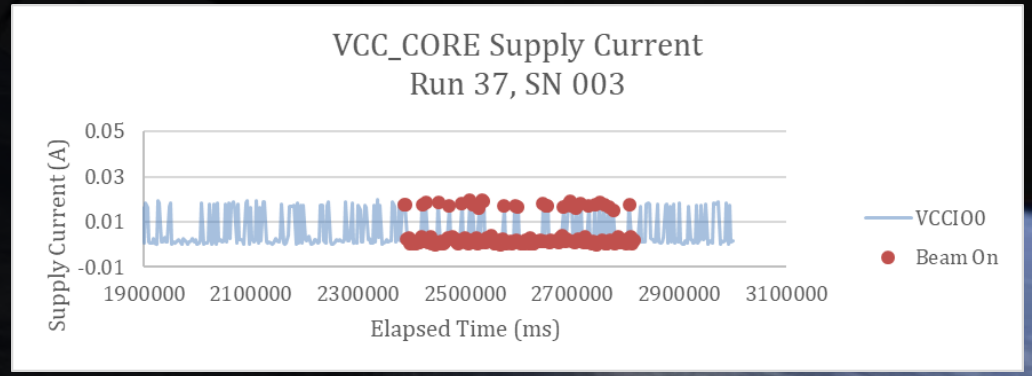
Certus™-NX-RT

- No sustained current excursions observed indicating no SEL events. All testing performed at 125C
- Run 37 current plots shown as representative examples
- VCC Core dominates combined current

Session	Run #	SN	12V Vdd (V)	Internal Vdd(s) (V)	Ion	Eff. LET (MeV·cm²/mg)	Eff. Fluence (ions/cm²)	Latchup
Aug	1	1	13.2	Nom	Xe	88.6	1.0×10^{7}	No
Aug	2	2	13.2	Nom	Xe	88.6	1.0×10^{7}	No
Nov	37	3	13.2	+10%	Xe	80.2	1.0×10^{7}	No



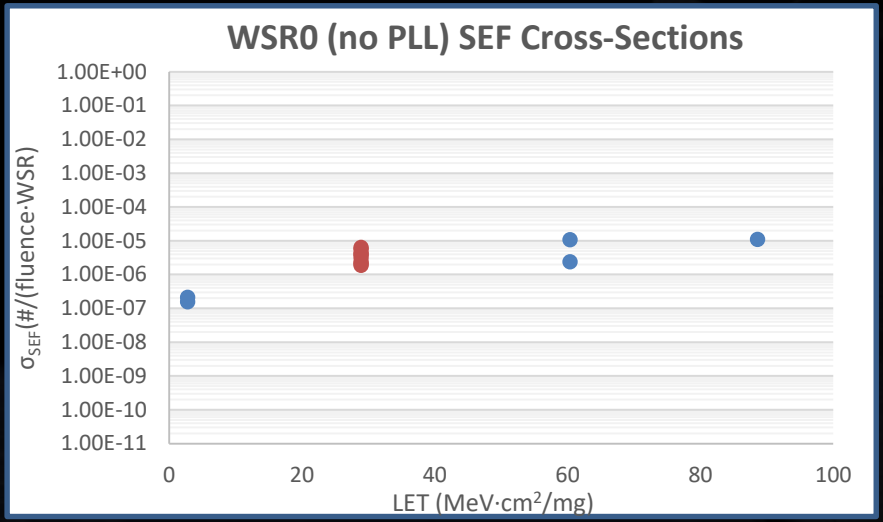




Fabric DFF Operating SEU Cross-Section

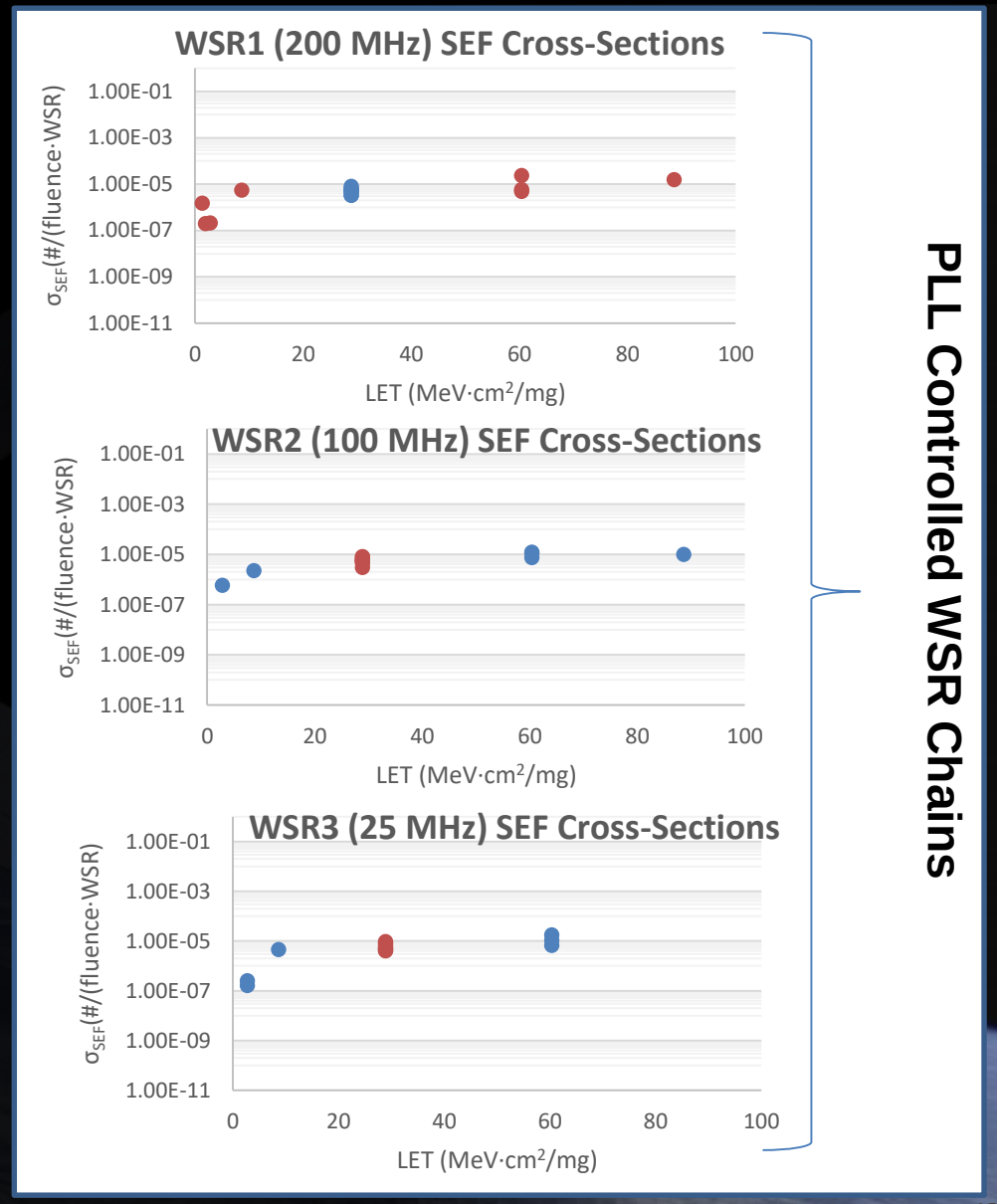
Certus™-NX-RT

- There are 400 DFFs per string. (SEF represents SEU in shift registers or configuration failures).
- PLL or frequency changes, do not significantly affect WSR SEF susceptibility.



No PLL clock is direct from clock pin + global buffer

Parameter	Comment
On-set LET (L_0)	L_0 = 8.66 MeV·cm²/mg.
On-set (σ_0)	$\sigma_0 \approx 1.0\times10^{-11}$(# /fluence·DFF)
Saturation LET (L_{sat})	8 MeV·cm²/mg< L_{sat} < 12 MeV·cm²/mg
Saturation SEF cross section (σ_{sat})	$\sigma_{sat} \approx 2.7\times10^{-8}$ (# /fluence·DFF)



PLL Controlled WSR Chains

Configuration RAM

Certus™-NX-RT

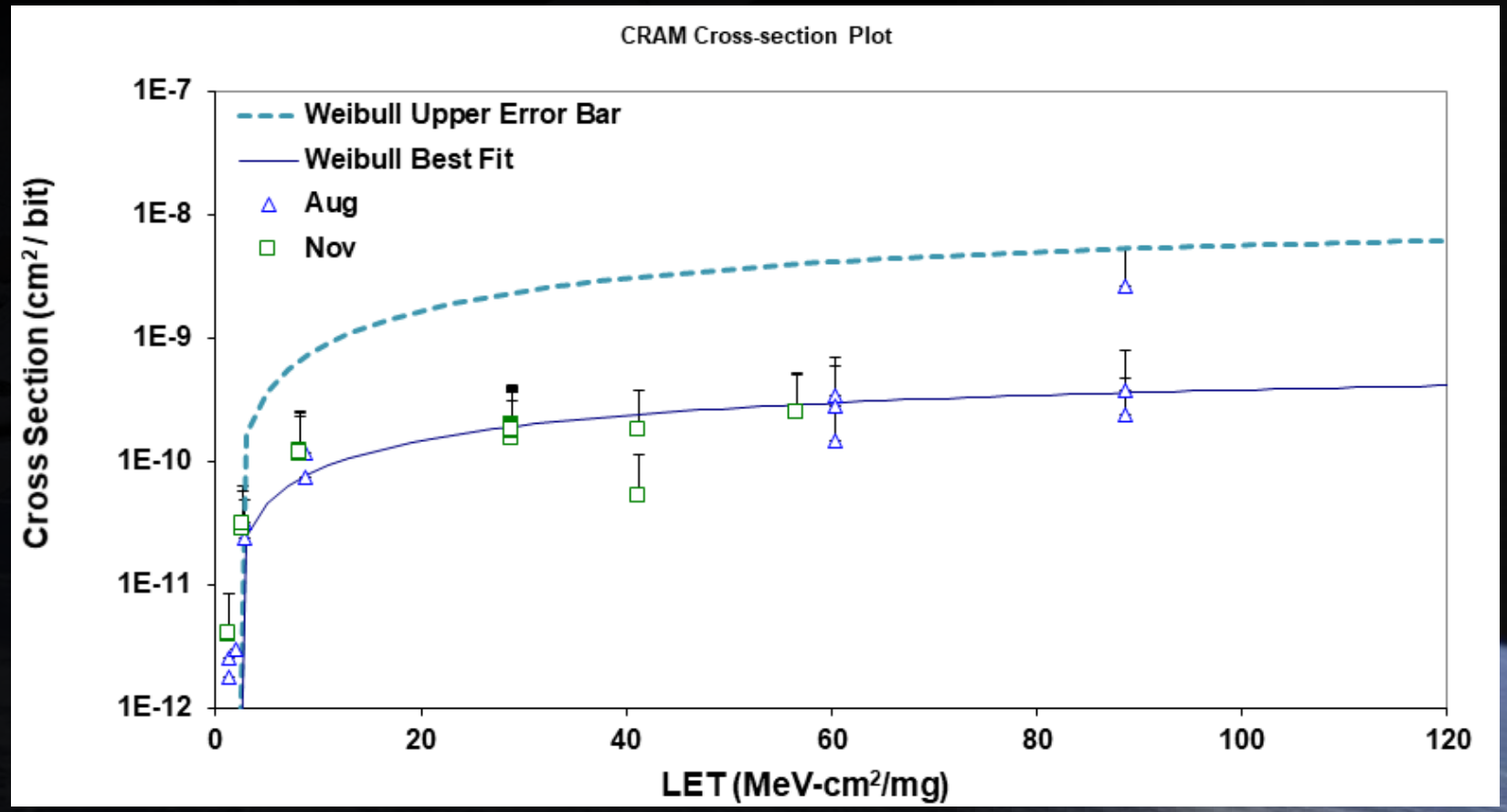
- Error rates for configuration memory are very low
- There are 6.2E6 configuration bits in the Certus-NX-RT

Best Fit Weibull

Shape	Width	Sat. X-sect	LETonset	GEO Adams 90% err/bit·day	LEO-ISS Adams 90% err/bit·day
0.8	80	5.5E-10	1.3	3.94E-10	5.54E-12

Upper Error Bar Weibull

Shape	Width	Sat. X-sect	LETonset	GEO Adams 90% err/bit·day	LEO-ISS Adams 90% err/bit·day
1	80	8.0E-09	1.3	1.02E-08	4.91E-10



TID Test Results

Certus™-NX-RT

- 5 parts tested to 100krad(Si), 2 additional parts step stressed to 200krad(Si). See full report for details
- All seven devices passed the Windowed Shift Register functional tests, DC levels tests, rise/fall time tests to the 100krad(Si) specification level
- Above 100krad(Si) on step stress parts, effects of TID were observed on the VIL, VOL and VIH

Test	Qty	Voltage Bias	WSR	VIL	VIH	VOL	VOH
TID Step Read points	5	Nom + 5%	100k rad(Si)				
TID Specification	5	Nom + 5%	100 krad(Si)				
Lowest WSR failing TID	5	Nom + 5%	No fails	No fails	No fails	No fails	No fails
Highest WSR passing TID	5	Nom + 5%	100k	100k	100k	100k	100k
Lowest TID at which all Fail	5	Nom + 5%	No fails	No fails	No fails	No fails	No fails
Highest TID at which all Pass	5	Nom + 5%	100k	100k	100k	100k	100k

Test	Qty	Voltage Bias	WSR	VIL	VIH	VOL	VOH
TID Step Read points	2	Nom + 5%	30k, 60k, 100k, 150k, 200k rad(Si)				
TID Specification	2	Nom + 5%	100 krad(Si)				
Lowest WSR failing TID	2	Nom + 5%	No fails	200k	200k	200k	200k
Highest WSR passing TID	2	Nom + 5%	200k	150k	200k	150k	200k
Lowest TID at which all Fail	2	Nom + 5%	NA	200k	NA	200k	NA
Highest TID at which all Pass	2	Nom + 5%	200k	150k	150k	100k	150k

Proton Testing

Certus™-NX-RT

- Devices exposed to proton energies of 25, 50, 100, 200 MeV
- Single Event Failure cross-section characterized on four designs:
  - PCIe with scrubbing
  - PCIe without scrubbing
  - WSR/PLL
  - ADC/Comparator
- Single Event Upset cross-section characterized for:
  - Configuration Memory (CRAM)
- Details of above in full report

Configuration Memory (CRAM)

Certus™-NX-RT

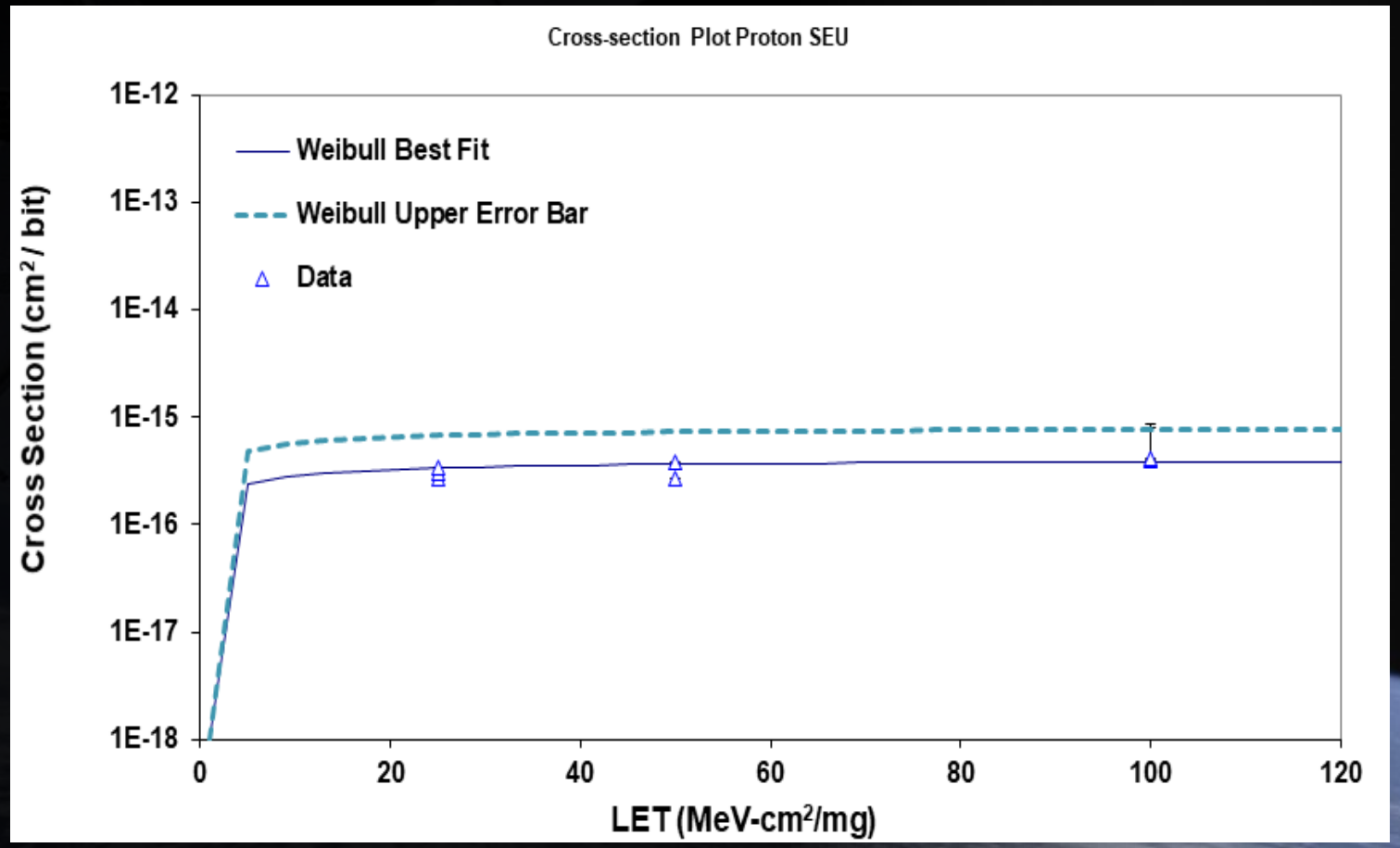
- Configuration cross-section data plotted as number upset cells divided by fluence and number of bits
- Data appear to be relatively flat across the tested range of proton energies

Nominal Fit Weibull

Shape	Width	Sat. X-sect	LETonset	LEO ISS err/bit·day
0.4	5	4.00E-16	1	3.75E-10

Upper Error Bar Weibull

Shape	Width	Sat. X-sect	LETonset	LEO ISS err/bit·day
0.4	5	8.00E-16	1	7.50E-10



QA/Reliability Assessment

Certus™-NX-RT

- Reliability Assessment of Technology/Product Complete
  - Technology documentation provided by Lattice
  - Assessed for 10 years @ 85°C lifetime:
    - HCI – Hot Carrier Injection
    - BTI – Bias Temperature Instability
    - TDDB – Time Dependent Dielectric Breakdown
    - EM – Electromigration
    - IMD-TDDB – Intermetallic Dielectric TDDB
    - SM – Stress Migration
  - Technology qualification follows JEP001 Level 1 and Level 2

All mechanisms passed for the target lifetime of 10 years

Product Qualification Summary

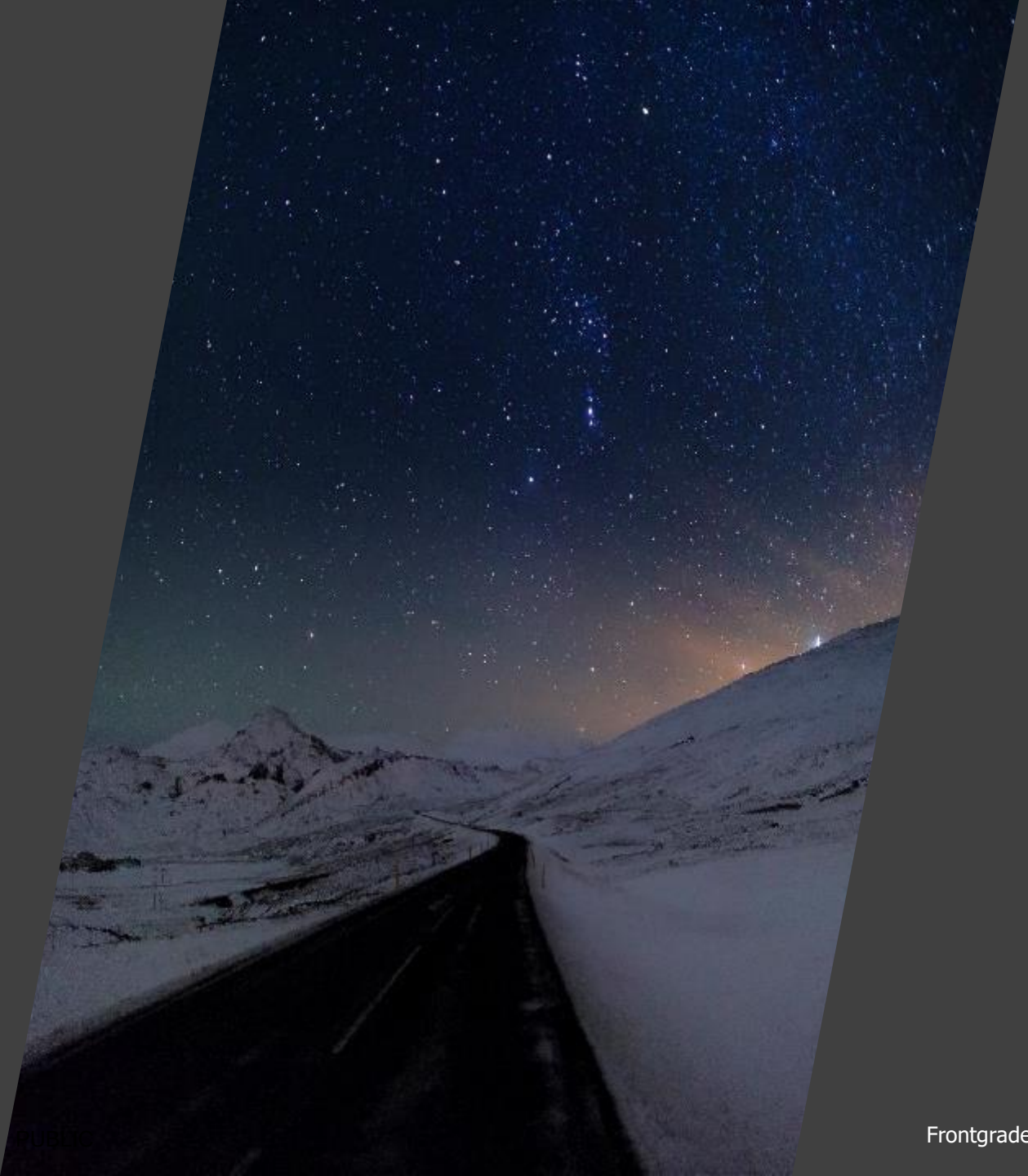
Certus™-NX-RT

Test Name and Conditions	Hours or Cycles (Failures / Devices Tested)	
High Temperature Operating Life & Early Life Failure Rate JESD22-A108 125°C, Max Vdd Typical Operating Conditions (Tjuse=55C, CL=60%, Ea=0.7eV): 23.6 FITs	500,500 Hrs	
	0 / 3616	
ESD	HBM	CDM
	Class 2 (2000 to < 4000V)	Class C1 (250 to < 500V)
Latch-Up	I-Test	Voltage Supply Overvoltage
	Class II (> +/- 100 mA)	Class II (> 1.5x Vdd)
Pre-Conditioning Level	MSL 3	
Temperature Cycling JESD22-A104, Condition B	700 cycles	
	0 / 75	
Temperature Humidity JESD22-A101, 85°C/85%	1000 hrs	
	0 / 75	
Temperature Humidity Bias JESD22-A101	1000 hrs	
	0 / 75	
High Temperature Storage Life JESD22-A103, Condition B, 150°C	1000 hrs	
	0 / 75	

Key Takeaways

Certus™-NX-RT and CertusPro™-NX-RT

- Low power, small footprint and high performance FPGAs
- Built on reliable and radiation tolerant 28nm FD-SOI
- 100krad(Si) TID, SEL immune @ 80 MeV·cm^2/mg and 125C
- Frontgrade reliability, radiation and application engineering support
- GRLIB IP Library support
- Certus-NX-RT available now with 2 week leadtimes
- CertusPro-NX-RT available Q4 2023



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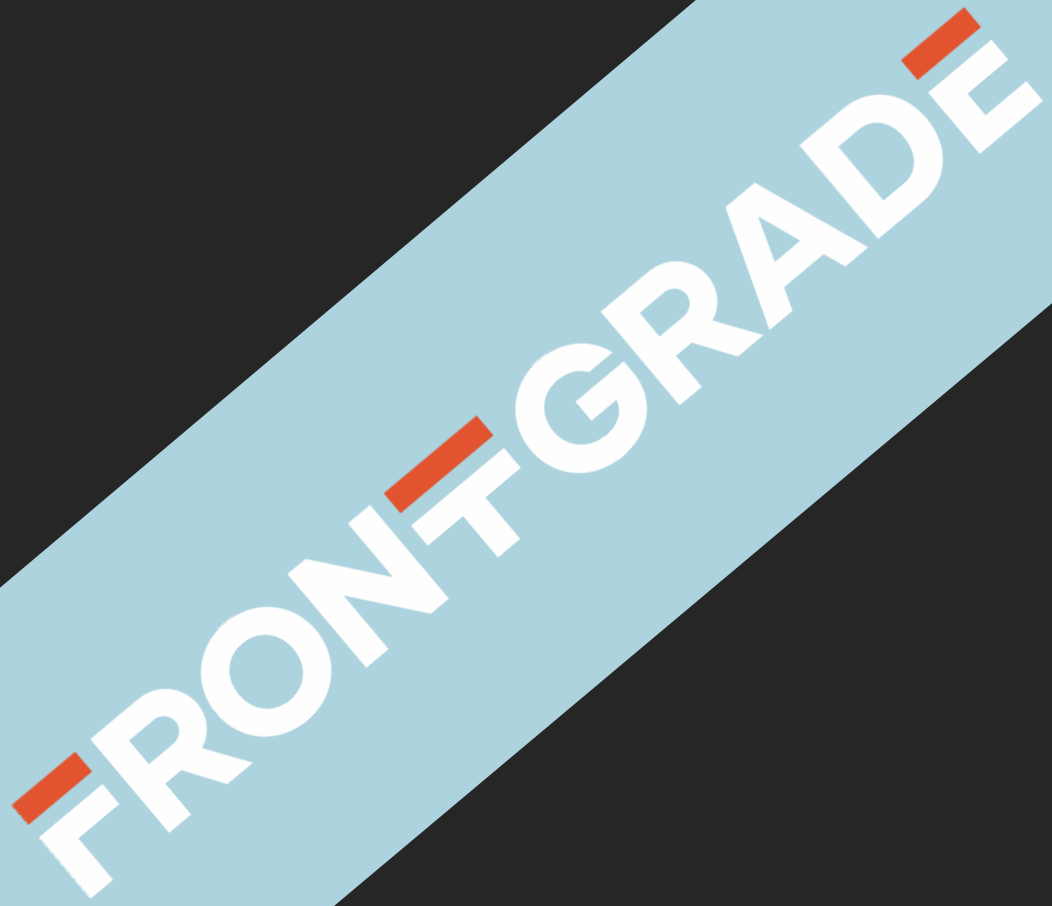
Q&A



THANK YOU