GRLIB VHDL IP Library

SEFUW 2023

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Product Marketing Engineer

FRONTGRADE Gaisler

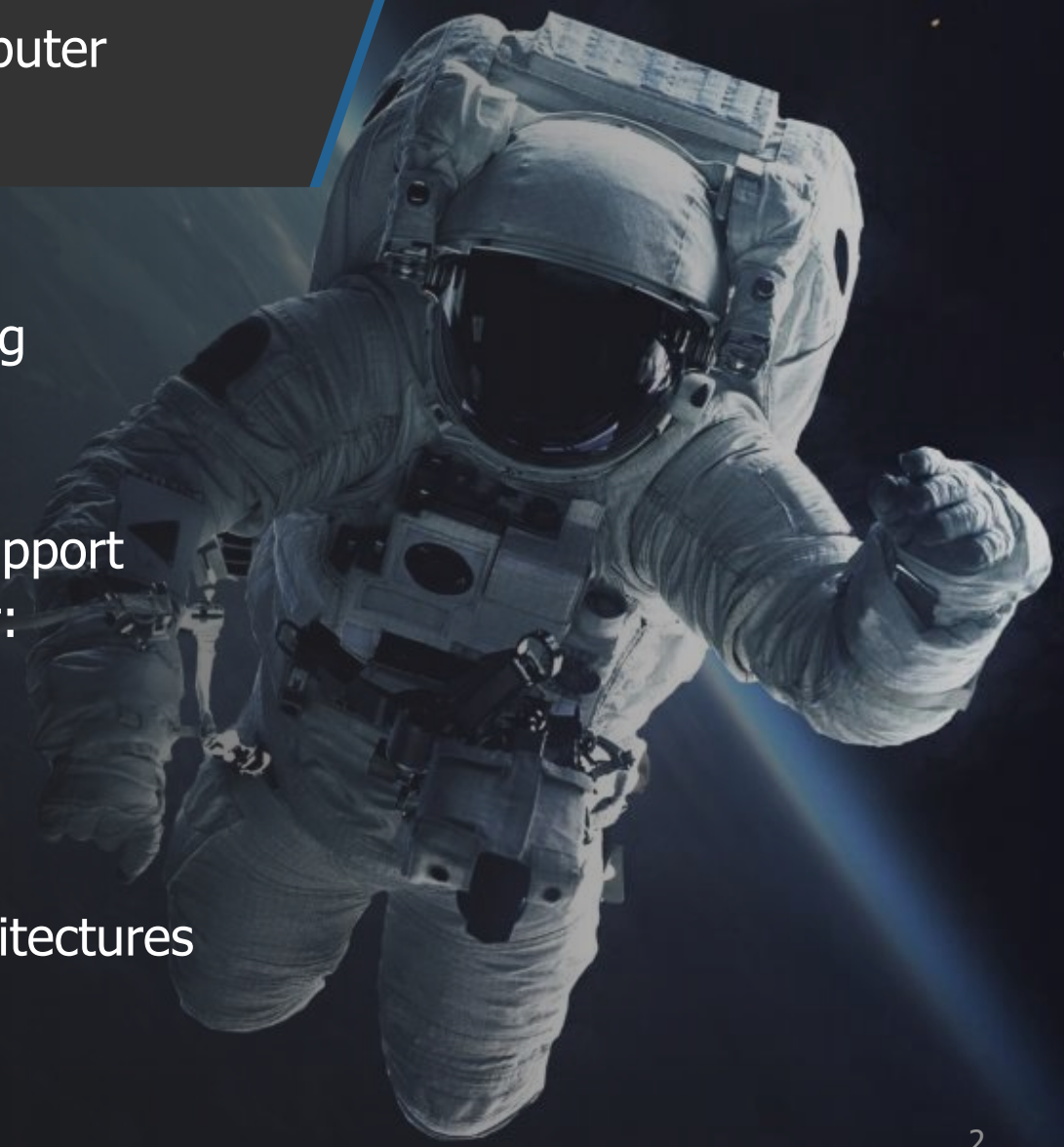
A world leader in embedded computer systems for harsh environments

Experts in fault-tolerant computing

We provide a full ecosystem to support hardware and software design for:

- Standard components
- Semi-custom FPGA
- Full custom ASIC

Based on SPARC and RISC-V architectures



Gaisler's EEE Portfolio

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High-reliability

- Radiation hardened
- Space qualified
- Fault-tolerant

NOEL Processor Family

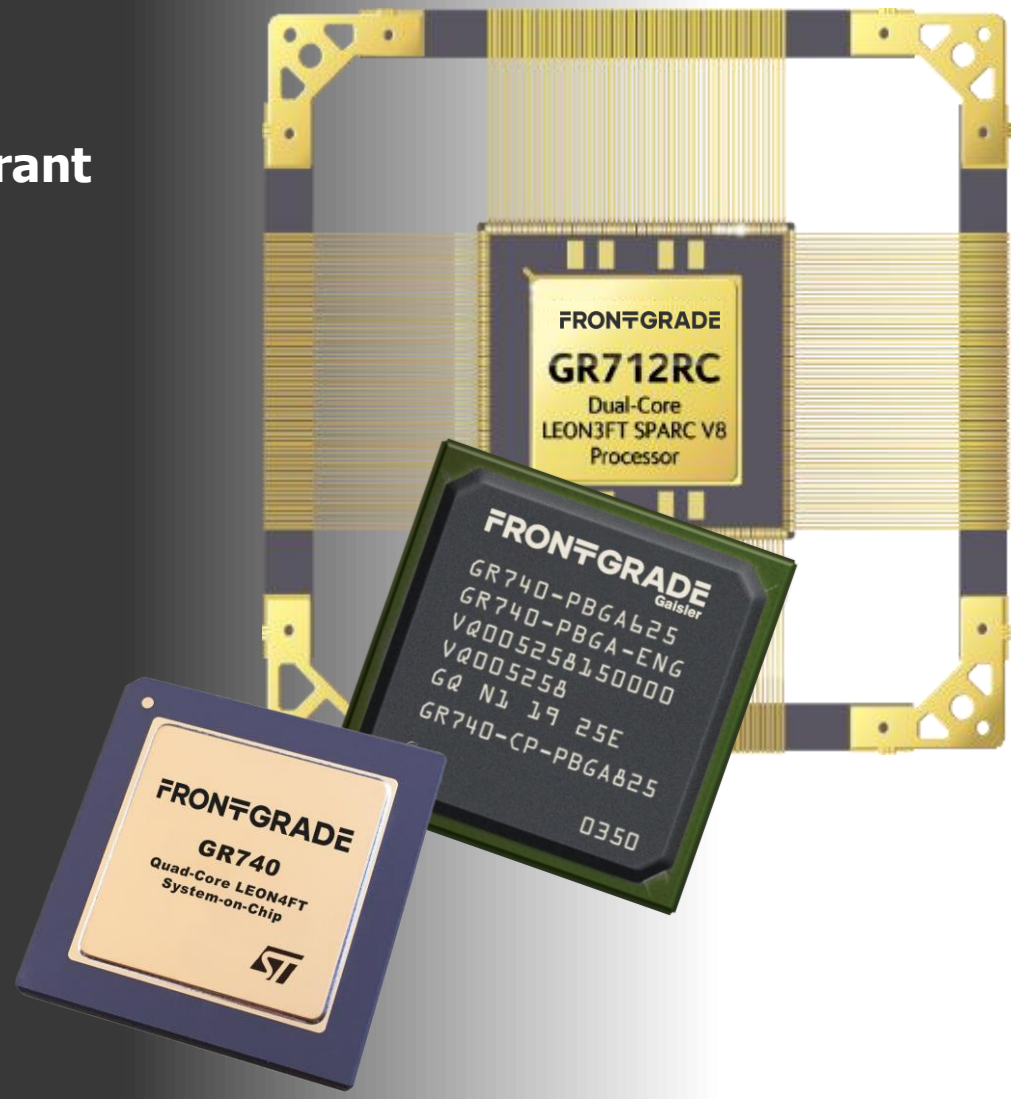
- GR7xV, NOEL-V, 16-Core, in development
- GR765, NOEL-V, 8-Core, in development

LEON Processor Family

- GR765, LEON5FT, 8-Core, in development
- GR740, LEON4FT, quad-core, 250 MHz, QML-Q, QML-V
- GR740 PBGA, LEON4FT, quad-core, 250 MHz, Flight units in Q1 2023
- GR716A, LEON3FT, single-core, 50 MHz, Flight units in Q1 2023
- GR716B, LEON3FT, single core 100 MHz, in development
- GR712RC, LEON3FT, dual-core, 100 MHz, Vendor class S
- UT700, LEON3FT, single-core, 166 MHz, QML-Q, QML-V
- UT699E, LEON3FT, single-core, 100 MHz, QML-Q, QML-V
- UT699, LEON3FT, single-core, 66 MHz, QML-Q, QML-V

Interface Family

- GR718B, Radiation-Tolerant 18x SpaceWire Router, Vendor class S



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How to design a space-grade SoC?

GRLIB - VHDL IP LIBRARY

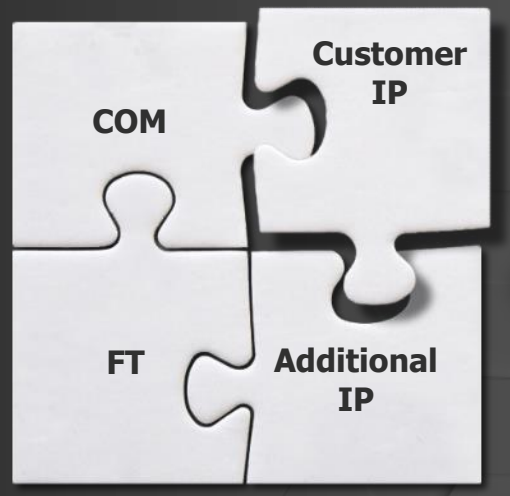
- GRLIB is a complete SoC design environment:
  - IP Cores
  - AMBA on-chip bus with plug & play
  - Scripts to support implementation tools
  - Template designs for FPGA evaluation boards
- GRLIB supports all space FPGAs

IP core licensing model

www.gaisler.com/getgrlib

Commercial licensing

- Three groups of IP cores:
  - COM – standard distribution
  - FT – Standard with fault-tolerant features
  - Additional IP cores
- Enables proprietary designs
- Covered by support agreement



Free open source, GNU GPL

- Limited number of IP cores
- Enables evaluation before decision
- Extensively used by academia and hobbyists
- Not for commercial designs
- GRLIB community

IP core building blocks

- Synthesizable processor cores and system peripherals
- Described in VHDL code
- Excel sheet for SoC area estimation

GRLIB community

NOEL Processor Family
- NOEL-V

LEON Processor Family
- LEON5
- LEON4
- LEON3

Peripherals
- Memory controllers
- On-chip interconnect
- Communication interfaces
- Encryption and compression
- Error detection and correction
- Spacecraft data handling functions
- Verification
- Auxiliary functions
- Test functions

All peripherals can be used with NOEL and LEON families

NOEL-V | LEON

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GRLIB IPs: Processors

LEON3 & LEON4 – SPARC Processors

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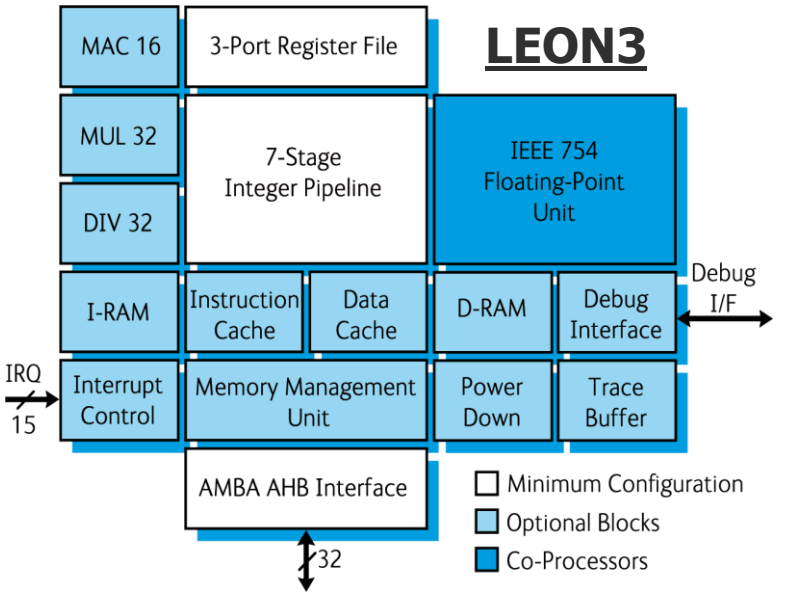
Baseline Features

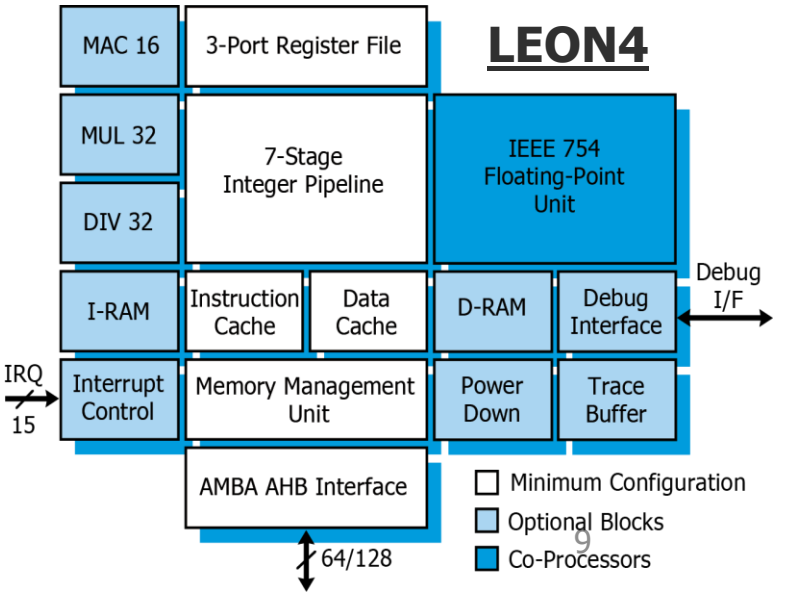
- **32-bit SPARC V8 processors**
  - In-order single-issue pipeline
- **Extensive flight heritage**
- **Multi-core support** (AMP & SMP)
  - Optional Memory Management Unit
- **Highly configurable**
  - Ex. configurable cache size, replacement policy and more
  - Optional Hardware Multiply/Divide/MAC
  - Optional floating-point unit (FPU), high-performance or area efficient
- **Performance**:
  - LEON3: 1.4 DMIPS/MHz
  - LEON4: 1.7 DMIPS/MHz

LEON SPARC

Optional Fault-tolerance
Single event upsets (SEU) errors in all on-chip memories are detected and corrected transparently to software

Users considering LEON4 for new designs are recommended to evaluate LEON5





LEON3-GP in space-grade FPGAs

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	Certus-NX UT24C407	CertusPRO-NX UT24C1007
Max frequency	50 MHz	50 MHz
LUTs	40%	16%
Registers	15%	6%
Block RAMs	57 %	23%

MICROCHIP

	RTG4 CG1657	PolarFire MPF300T
Max frequency	50 MHz	80 MHz
LUTs	10%	4%
Registers	4%	2%
BRAMs	18%	1%

NanoXplore

	NG-MEDIUM NX1H35AS	NG-ULTRA
Max frequency	20 MHz	40 MHz
LUTs	33%	3%
Registers	11%	1%
Block RAMs	55%	9%

XILINX

	Ultrascale XCKU060	Versal VC1902
Max frequency	150 MHz	230 MHz
LUTs	2%	<1%
Registers	<1%	<1%
BRAMs	1%	1%

LEON5 – SPARC Processor

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Baseline Features

- **32-bit SPARC V8 processor** core
- **Multi-core support** (AMP & SMP)
- **Improved performance** over LEON3 & LEON4
  - In-order dual-issue pipeline
- **Improved fault tolerance (FT) from SEUs**
- **Improved FPU**: Floating Point Unit with denormalized number support
- **Leverage existing software:** maintain binary compatibility with LEON3 and LEON4
- **Optional Local RAM** (Tightly coupled memory)

New Fault Tolerant features:
L1 cache SECDED ECC allows error correction on the fly. Optional internal hardware scrubber for L1 and register file

Performance:

- Dhrystone*: 3.23 DMIPS/MHz
  (-O3, inlining allowed)
- Coremark* : 4.52 CoreMark/MHz
  (-O3,-funroll-all-loops -finline-functions -finline-limit=1000)

* All the results generated using BCC 2.0.7 toolchain

NOEL-V – RISC-V Processor

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Characteristics:

- RISC-V processor core
  - 32- or 64-bits architecture
- Superscalar – in order pipeline
- Fault Tolerance features
- Leverages RISC-V software and tool support in the commercial domain together with our offering
- Highly configurable

Primary feature set:

- **RISC-V RV64GCH or RV32GCH**
  - Can run complex OS (like Linux) in full virtualization
- AHB and AXI4 bus support

Performance

- Comparable to ARM Cortex A53
- CoreMark*/MHz: 4.41**

* GCC9.3.0 20200312 (RTEMS 5, RSB 5 (c53866c98fb2), Newlib 7947581
-g -march=rv64ima -mabi=lp64 -B /gsl/data/products/noelv/rtems-noel-1.0.3//kernel/riscv-rtems5/noel64ima/lib --specs bsp_specs -qrtems -lrtemsdefaultconfig -O2 -funroll-all-loops -funswitch-loops -fgcse-after-reload -fpredictive-commoning -mtune=sifive-7-series -finline-functions -fipa-cp-clone -falign-functions=8 -falign-loops=8 -falign-jumps=8 --param max-inline-insns-auto=20

** Using "#define ee_u32 int32_t" in core_portme.h, as is common for 64 bit RISC-V.

NOEL-V Example Configurations

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GENERAL			CONTROLLER	
HP	**GP**	**GP-lite**	**MC**	**MC-lite**
• High-performance • Supports full virtualization of OS like Linux & VxWorks	• General purpose • Supports full virtualization of OS like Linux & VxWorks	• General purpose • Area optimized • Supports OS like Linux & VxWorks	• Micro-Controller • Supports OS like RTEMS	• Micro-Controller • Area optimized • Supports OS like RTEMS

All the configurations support:

- 32- or 64-bits architectures
- Fault-tolerance features

It is also possible to finely tailor more configurations by changing simple parameters

noel-V RISC-V®

NOEL-V & LEON5 Fault tolerance overview

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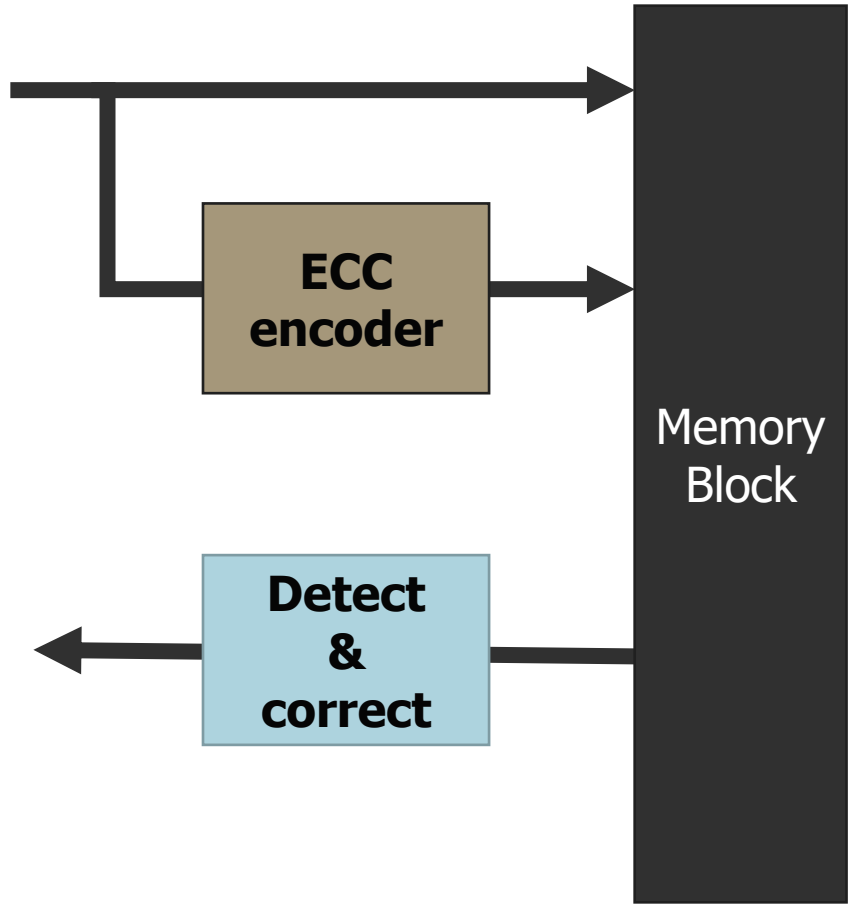
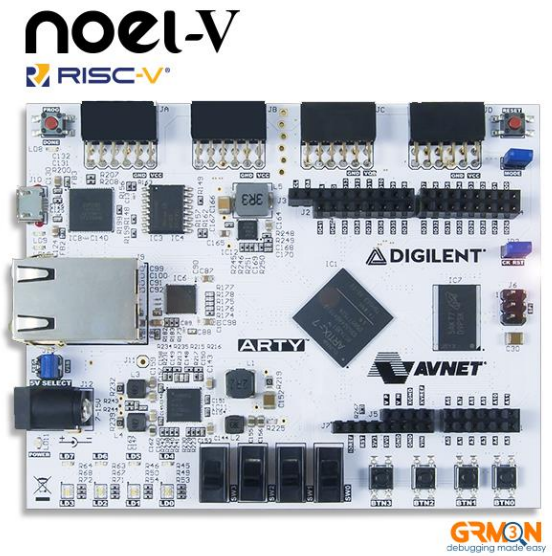
- No need for lock-step or redundant CPUs
- Protection of memory blocks (in caches & register file) using error correcting codes.
- Protected with a full SECDED code with custom scheme:
  - Deliver correct data locally without causing memory access
  - Guaranteed detection also of 3-bit and 4-bit adjacent bit errors
- Hardware scrubber built into processor to avoid error build-up
  - Removes need for manual scrubbing routines
- Error counters and diagnostic interfaces
  - Monitor and inject errors



LEON5 & NOEL-V IP availability

- LEON5 and NOEL-V are available as part of the GRLIB IP library
- FPGA bitstreams for Xilinx and Microchip FPGA evaluation boards are available for download (See links below)
- Debug monitor and software toolchains (Bare-C, RTEMS, Linux, …) are also freely available



NOEL-ARTYA7

LEON-PF

NOEL-PF

LEON-XCKU

NOEL-XCKU

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GRLIB IPs: Fault-tolerant Memory Controllers

Fault-tolerant DDR2/3 SDRAM Controller

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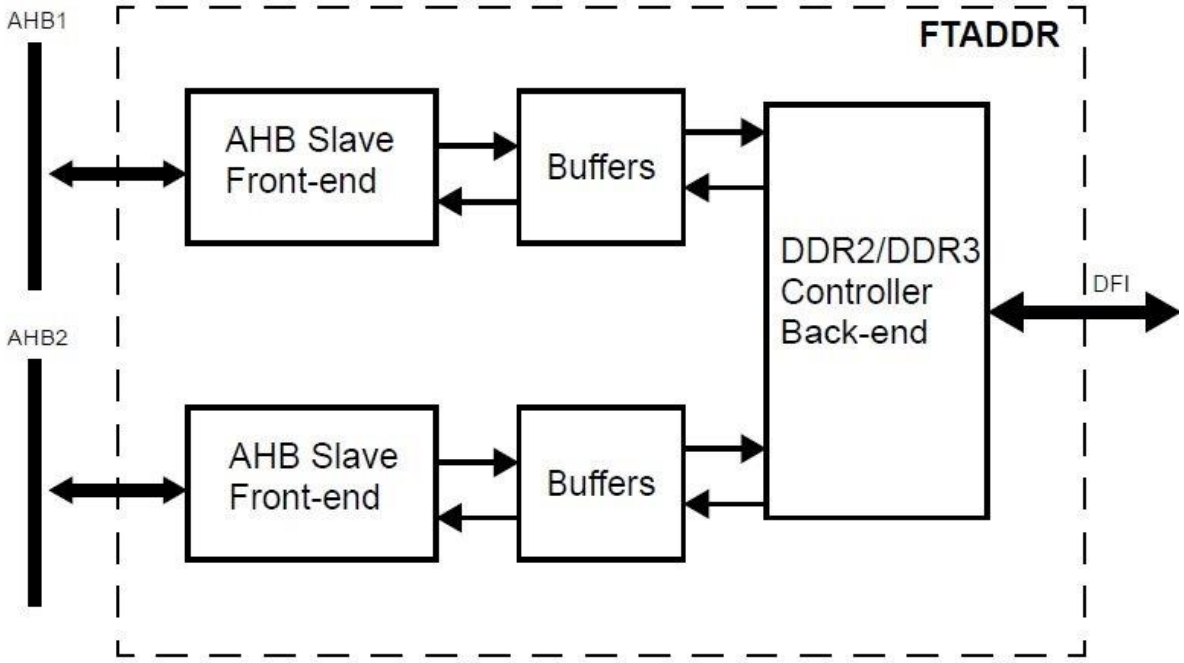
Baseline Features

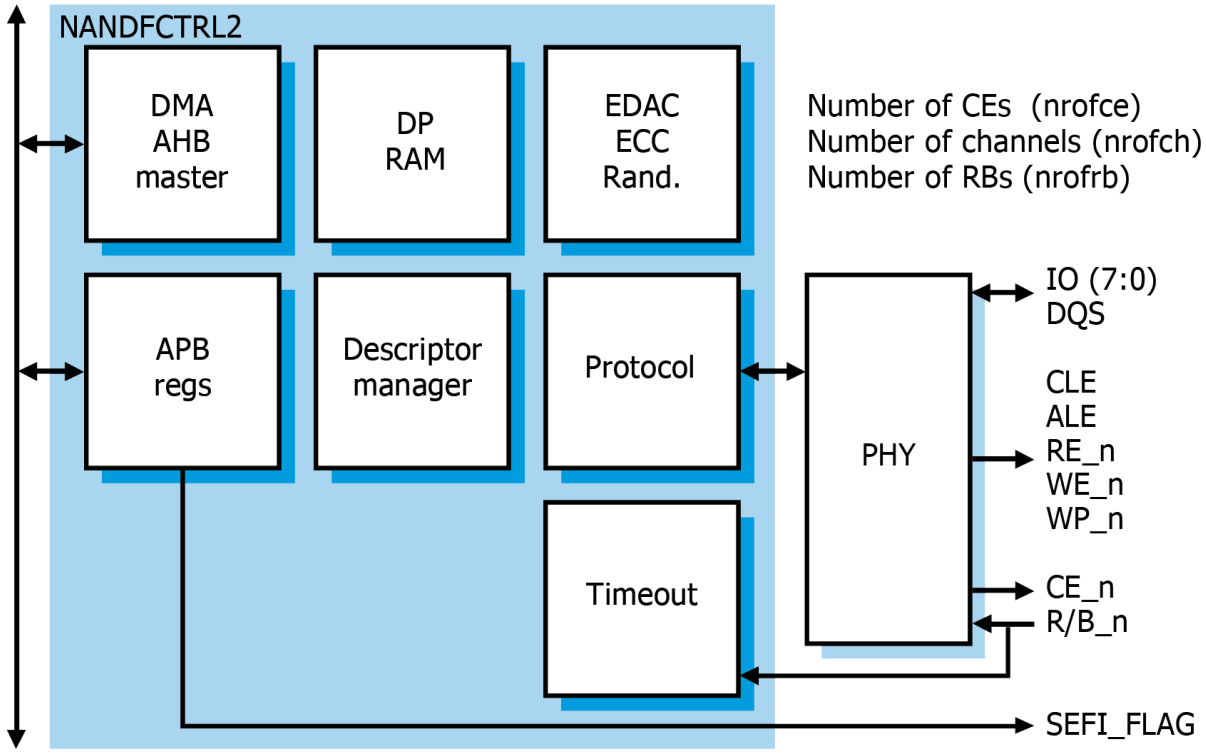
- DDR2 and DDR3 support
- Configurable to have multiple AHB ports with concurrent accesses to different memory banks
- 96-, 64- or 32-bits interface towards SDRAM
  - Devices of width x8 or x4
- Support for several PHYs:
  - Generic DFI
  - Altera UniPhy
  - Xilinx Ultrascale
- Strong error correction code to achieve double device correction capability
  - Deliver correct data despite one full device failure and random SEU-induced errors on the other devices.
- Up to 8 parallel banks (chip selects)
- Can operate autonomously:
  - Designed to support also processor-less configurations



Fault-tolerant NAND Flash Controller

Baseline features

- ONFI 4.0 support
- Configurable BCH EDAC with up to 60 bits correction capacity per 1024 (or 512) bytes
- Randomization of memory data
- Timeout based SEFI detection and reporting
- 8-bit data interface
- Support for up to 64 targets



Evaluation Hardware

- Evaluation FMC board featuring UT81NDQ512G8T
- Bitstreams for Xilinx KCU105 & AlphaData ADA-SDEV-KIT2

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GRLIB IPs: I/O Interfaces

High Speed Serial Links controller

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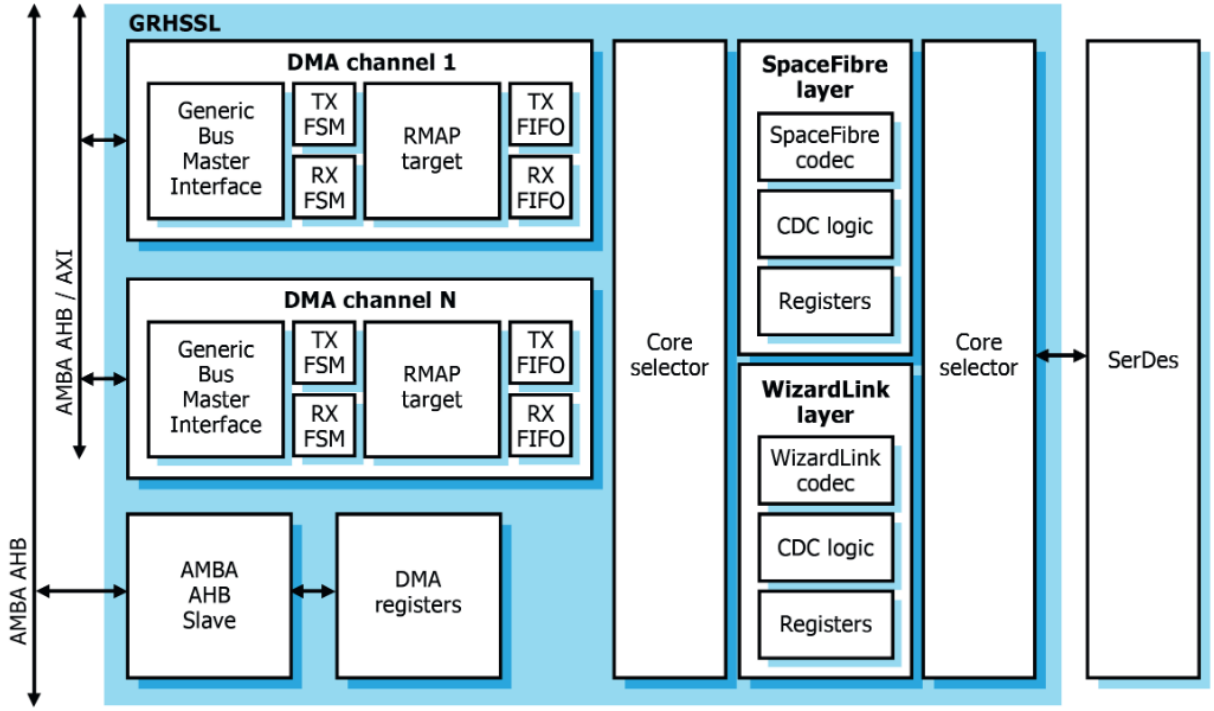
Baseline features

- Can Implement SpaceFibre, WizardLink or both
  - SpaceFibre single-lane implementation
  - WizardLink designed to interface with TI TLK2711
- Optional 8b10b encoding
- Support for wide (36/40) or narrow (16/20) SerDes interfaces
- Flexible DMA engine with multiple DMA channels
- Optional SpaceFibre RMAP support
- The IP can inter-operate with off-chip SerDes devices or with FPGA/ASIC hard macros
- Active controller (SpaceFibre or WizardLink) selectable at run-time via AHB registers
- Optional fault-tolerant features



Evaluation hardware

- Template designs for Xilinx Ultrascale boards

CAN FD controller

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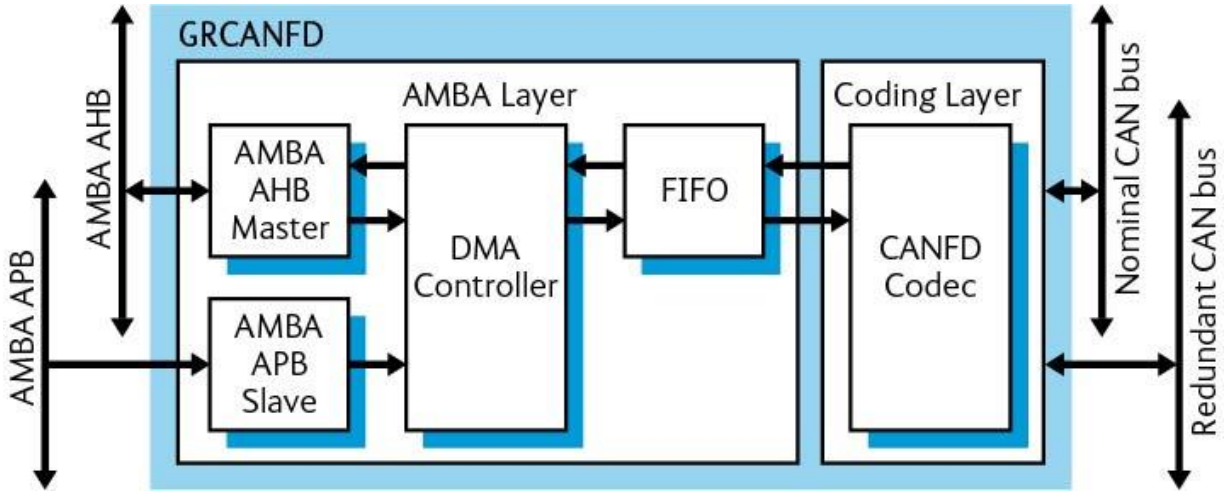
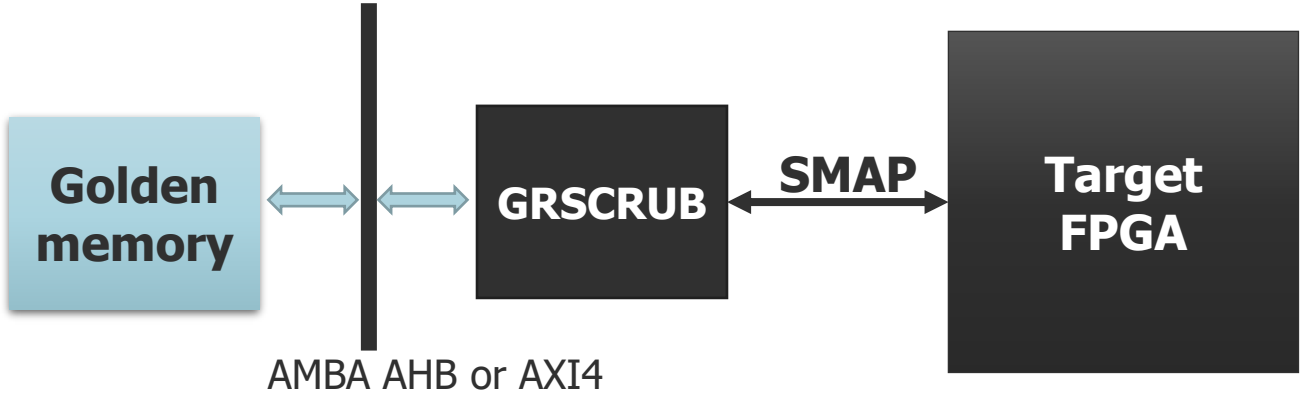
Baseline features

- Fully compatible with ISO 11898-1:2015
- DMA engine with either AMBA AHB 2.0 or AXI4 interface
- Optional fault-tolerant features
- Filters for frame acceptance and for synchronization
- CAN bus redundancy
- Transmitter Delay Compensation
- Internal or external loopback
- Optional CANOpen support (Minimal Set Protocol)
  - Provide R/W access to on chip-bus
  - Support for Heartbeat commands



FPGA Supervisor

GRSCRUB is an FPGA configuration supervisor responsible for programming and scrubbing FPGA's configuration memory in order to prevent the accumulation of radiation-induced errors.



Baseline features

- Access target FPGA through the SelectMap interface
- FPGA configuration
- Mapping of FPGA frame addresses
- Blind and readback scrubbing
- SEFI detection of the SelectMap interface of the target FPGA
- Current targets: Xilinx Kintex UltraScale and Virtex-5 FPGAs
- Can be configured to run periodic scrubbing with defined delay between runs

SEE testing

We performed two proton tests, demonstrating that introducing GRSCRUB considerably increases the radiation resilience of the design implemented in a Xilinx Kintex Ultrascale XCKU060.

GRSCRUB validation under SEE testing

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TEST SETUP

- **Protons testing:**
  - XCKU060 board: DUT SoC design based on NOEL-V processor with fault tolerance (FT)
  - Virtex5 board: SoC with GRSCRUB for programming and scrubbing the XCKU060
- **GRSCRUB configuration for the setup:**
  - SelectMap frequency: 25 MHz
  - Data bus width: 8 bits
  - Full readback and SelectMap integrity check period: 6.7s
- The scrubbing period is related to:
  - GRSCRUB settings
  - SelectMap configuration (frequency and bus width)
  - System frequency and golden memory bandwidth
  - Size of the target FPGA

RESULTS

- **No need for FPGA reprogramming while using GRSCRUB during the test campaign**
  - SEFIs recovered using SoC reset only
- **GRSCRUB greatly improves the system's reliability:**
  - GRSCRUB reduces **10x** the error susceptibility compared to an unprotected SoC (NVFT)
  - The error susceptibility is reduced **81x** by combining the GRSCRUB with a triplicated SoC (distributed TMR, NVFT-DTMR)

Orbital SEFI MTTF (Years)		
Orbit	NV FT	NV FT- DTMR
LEO	7.10	45.7
GEO	4.7	30.5

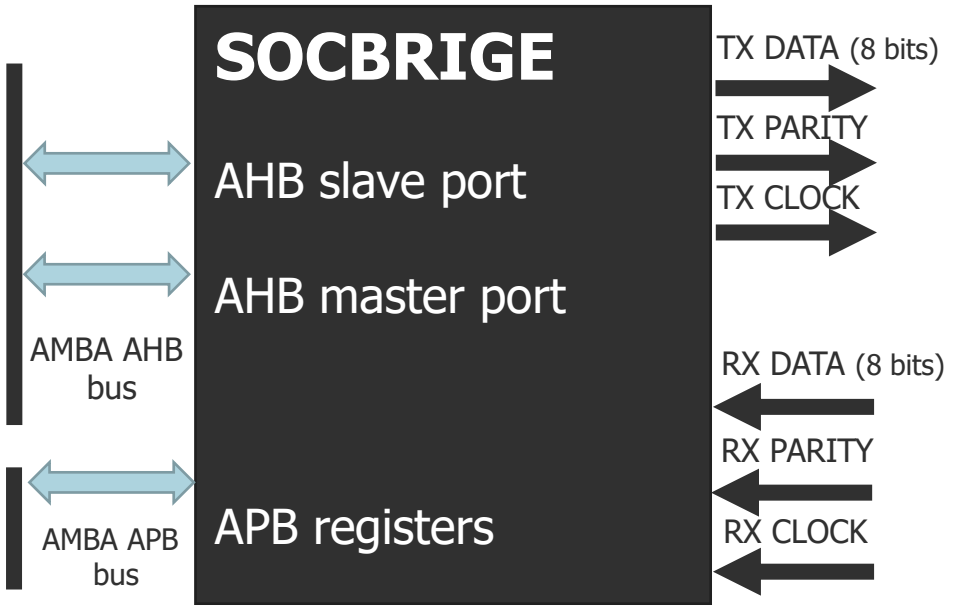
Combining the NOEL-V FT processor (with or without DTMR) with GRSCRUB is a robust hardness solution for SRAM-based FPGA designs

SoC BRIDGE

The SOCBRIDGE provides a bidirectional byte stream which allows a simple data transfer interface between the system-on-chip and an external device.

Baseline features

- Perfect for data transfers that require modest bandwidth
  - Example: command & control
- AHB master and slave ports
- Byte stream with data rate up to 1/8 of the AHB clock rate.
- Interface with 20 on-board signals
- Queue to hold any additional transfer requests that come in while a transfer is in progress
- Small area footprint and no impact on timing



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Conclusions

Conclusions

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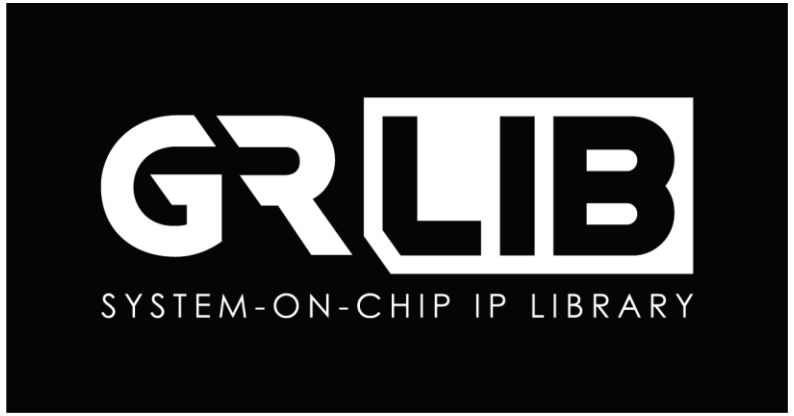
- **GRLIB is a complete tool-set to design a space-grade SoC**
- **GRLIB updates are released every quarter**
- **What's new in release 2023.1, coming in April?**
  - Frontgrade-Lattice FPGAs support
    - Technology mapping
    - Template designs
    - Project file generation
    - See GRLIB-Lattice website for roadmap
  - NanoXplore NG-Ultra FPGAs support
  - LEON5 performance improvements
  - NOEL-V new extensions
  - Improvements to Microchip Libero flow:
    - Passing of synthesis options to Synplify
    - Support for enabling/disabling retiming



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