FPGA- and Flash-based mass memory system: architectures, implementations, industry projects and future trends

Gang Zhou, Steffen Thiermann, Martin Herrmann, Christian Spindeldreier, Andre Schäfer, Ole Bischoff, Christian Dierker, Ulf Kulau, Elias Hashem

DSI Aerospace Technologie GmbH
Otto-Lilienthal-Str. 1, 28199 Bremen, Germany
Phone: +49 421 596969-0, Mail: info@dsi-as.de

INTRODUCTION

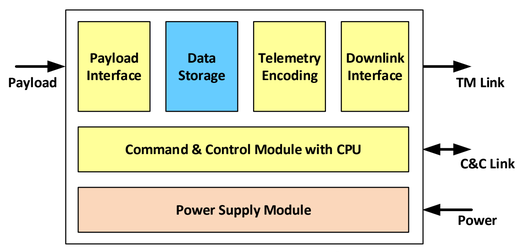
- The design challenge in PDHU (Payload Data Handing Unit) and OBC (On-Board Computer) exists for decades: increasing amount of data produced by high-resolution instruments vs. limited downlink bandwidth.
- Consequently, the demands for compact on-board data storage in terms of capacity and data rates are growing rapidly.
- High-end space grade FPGAs serves as the central controller and implements the most timing-critical data acquisition, buffering, storage and downlink functions.
- Design heritages: ESA Juice OBC mass memory board, ESA Biomass PDHU, KACST SCB (Satellite Computer Board), KARI Komposat 7 DSM (Data Storage Module), ESA Plato OBC mass memory board, ESA Hera OBC mass memory unit, S4Pro (H2020 demo project),
- On-going projects: ESA FLEX PDHU, ESA Copernicus CRISTAL and LSTM mass memory formatting unit, Copernicus CIMR PDHU, NASA+ESA ARTEMIS Gateway mass memory storage

DSI DESIGN APPROACHES TO MASS MEMORY MODULES

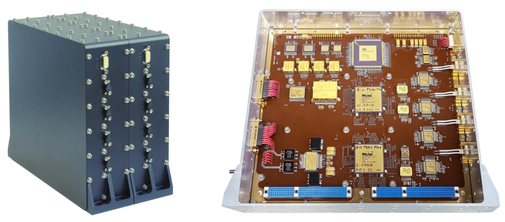
1) Compact PDHU Approach

The following design includes modern high capacity Flash devices and space grade FPGAs, which provides storage capacity of some Tbits and is capable to handle data rate of some Gbits within a small housing.

The Biomass PDHU consists of two PDHU slices (prime + redundant) with a volume of 260 × 133 × 224 mm³ and a mass of 6.4 kg. It accommodates 1 Tbit BOL (expandable) capacity per PDHU half and communicates with an aggregate data rate of approximately 1 Gbit/s over serial links (WizardLink) with the payload instrument and by parallel LVDS with the downlink transmitter. The power consumption is <15 W.



Compact PDHU Functions



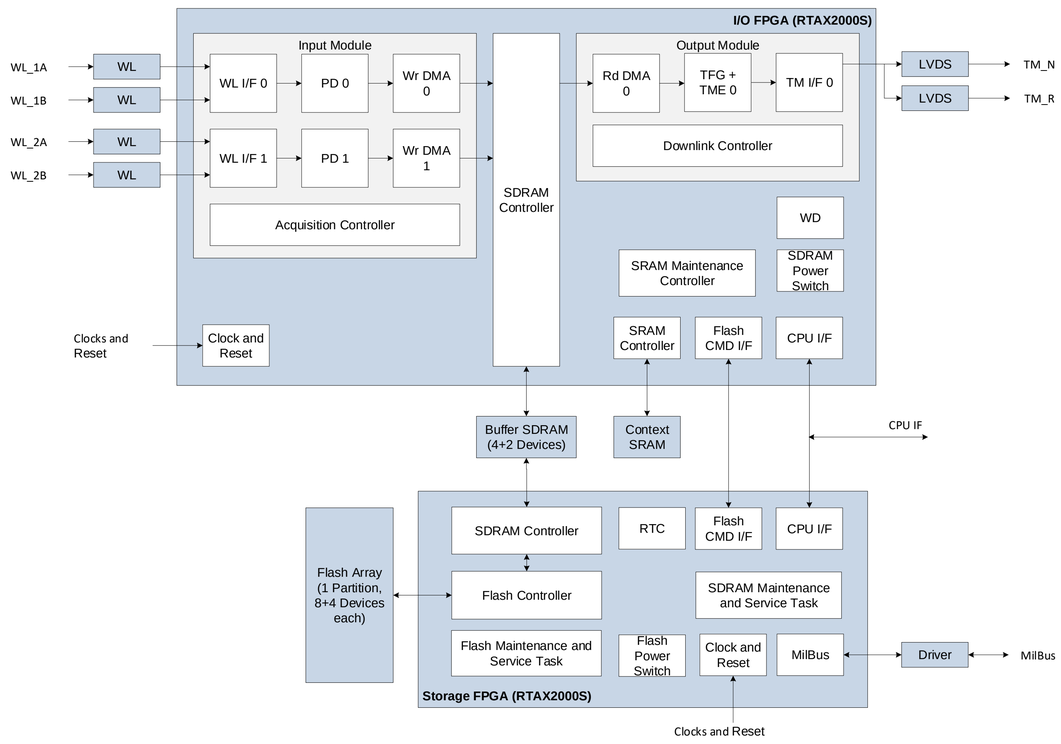
BioMass Compact PDHU
(one slice comprising 3 PCBs)

2) OBC-MM Approach

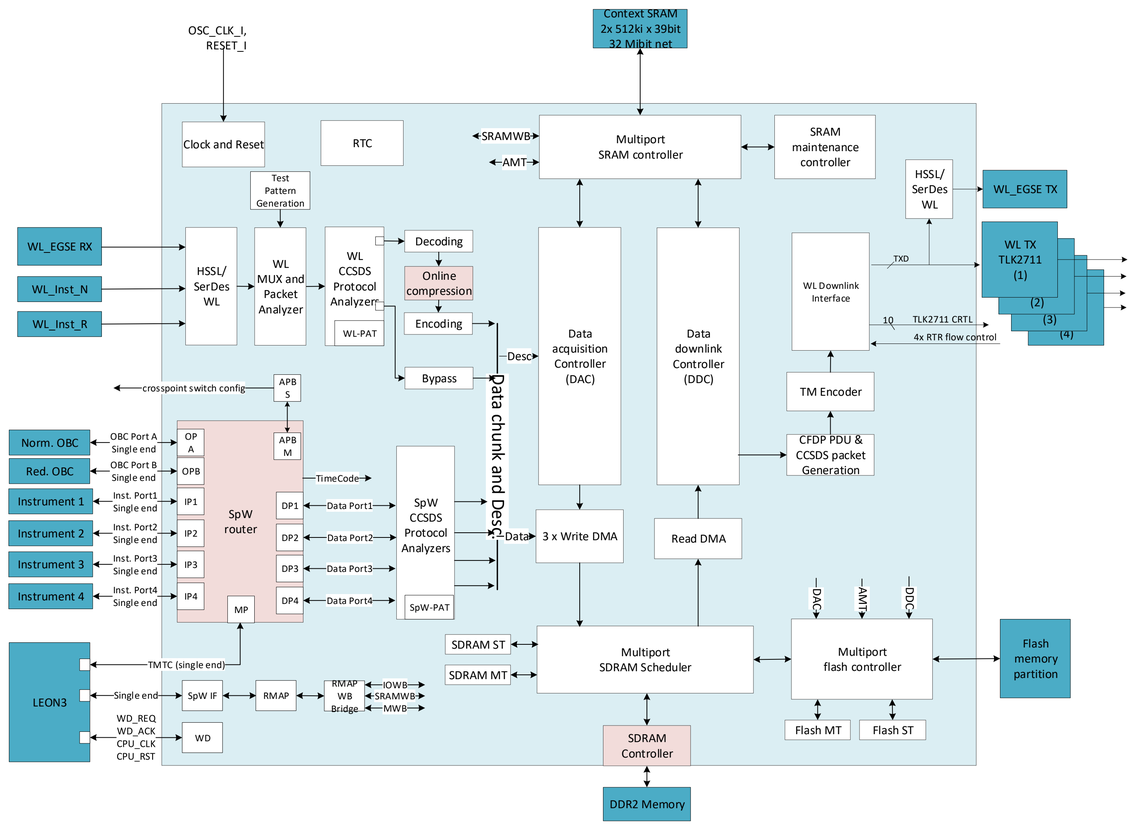
Together with RUAG and SCISYS DSI investigated a novel architecture for a Single Level Cell (SLC) NAND Flash based Mass Memory as an integrated module for OBCs with medium storage capacities (some Tbit) and data rates (some 100 Mbit/s).

The JUICE SSSM contains two printed circuit boards (PCBs) with an Interface Board (IFB) as baseboard and a Mass Memory Board (MMB) as daughterboard. It provides a capacity of 1.5Tbit (BOL) per module, a volume of 261 × 205 × 36 mm3, a mass of 1.8 kg with a power consumption of <13 W.

FPGA ARCHITECTURE EXAMPLE – TWO RTAX FPGAS



FPGA ARCHITECTURE EXAMPLE – SINGLE RTG4 FPGA



- Scalable flash controller, up to 4 partitions can be supported. The mass memory capacity is scalable
- Flexible logical to physical address mapping. The parallel accessed flash devices may have different flash block addresses so that flexible wear levelling algorithm can be supported in software
- Flexible flash access interleaving scheme to maximize flash interface performance
- Double symbol error correction (Reed-Solomon Code) for flash mass memory
- Flexible packet management: e.g., packet store based file management; logical address based mapping; application identifier based mapping; transaction identifier (CFDP) mapping, customized mapping
- Pass-through acquisition feature / near real time acquisition and downlink feature
- High data rate SDRAM controller for data buffering: SDRAM, DDR2, DDR3 etc
- Diverse payload interfaces with divise protocol analyzers, e.g. WizardLink, SpaceWire, Channel links, Ethernet, SpaceFibre etc
- Diverse downlink interfaces, data formatting and telemetry encodes, e.g. WizardLink, LVDS parallel interface, Ethernet, SpaceFibre etc
- External SRAM as context memory to compensate internal BRAM limitation (especially for Microchip RTAX FPGA)
- Diverse TM/TC interfaces, e.g., MIL-Bus, SpaceWire, Ethernet, UART, HPC (high power command), RSA (relay status acquisition), etc
- All memories (external and internal) are EDAC protected (Hamming / Reed-Solomon)
- Service tasks for all external memories e.g., direct memory access in user mode and raw mode.
- Maintenace tasks for all external memories, e.g., background write, fast verify, scrubbing etc
- Real-Time-Clock with diverse synchronization mechanisms, e.g., Milbus, SpaceWire TimeCodes, external PPS, customized methods
- Watchdog function with two stages timeout management
- Implementations on Microchip RTAX / ProASIC3E / RTG4 FPGAs
- On RTAX FPGAs, 2.2Gbps data acquisition + 640Mbps data downlink in an industry project
- On RTG4 FPGAs, 4Gbps data acquisition + 2Gbps data downlink
- Optional online/offline data compression / encryption / SpaceWire router

CONCLUSION AND FUTURE WORK

- Radiation-tolerant, compact, scalable and flexible mass memory unit for PDHU and OBC
- Fast time-to-market. Reprogrammable FPGA enables early HW procurement and manufacture
- Extension to synchronous flash memory achieved
- Extension to Xilinx FPGA on-going, expected to achieve aggregate 20Gbps data rate
- Working on radiation mitigation methods on Xilinx FPGA on-going
- Feasibility study of managed flash devices on-going

DSI Aerospace Technologie GmbH

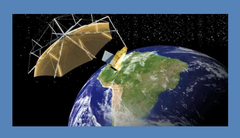
Otto-Lilienthal-Str. 1
28199 Bremen
Germany

Phone: +49 421-596969-0
Fax: +49 421-596969-59

www.dsi-as.de
info@dsi-as.de

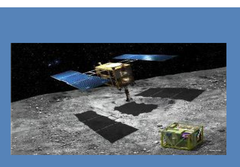
JUICE SSMM
Solid State Mass Memory of the CDMS

Biomass
Payload Data Handling Unit



KOMPSAT-7
Data Storage & Compression Equipment

Hayabusa-II MASCOT
On-board computer



MetOp-SG ICI
Command & data processing unit of the ice cloud imager instrument

Eu:CROPIS
Command & data handling sub-system

FLEX
Payload Data Handling Unit

ExoMars
Design & Development of the PDHU's Ctrl and I/O module