Estimating the Error Rates of Xilinx Zynq-7000 APSoCs in Space Radiation Environments

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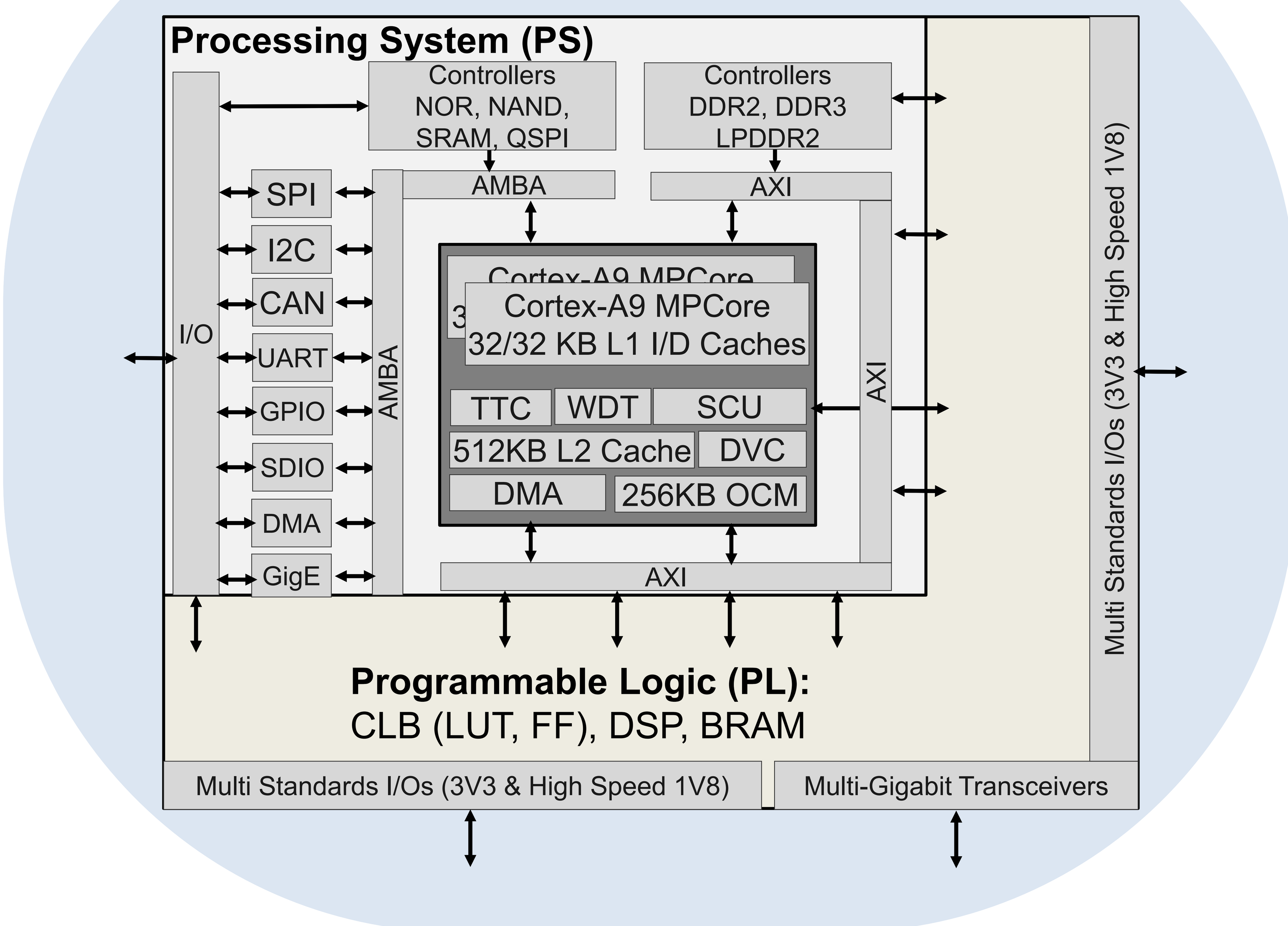
Motivation

- Previous works have investigated the impact of protons and heavy ions on the Zynq-7000 APSoC but not for a broad range of particle energies and of LETs
- This introduces uncertainty in predicting radiation-induced upset and error rates in various space radiation environments

Contribution

- Performed additional accelerated radiation tests at PSI (protons) and GSI (heavy ions) to widen the range of tested particle energies and LETs and thus be able to predict upset and error rates more precisely
- Provide cross-sections for both the PL and PS

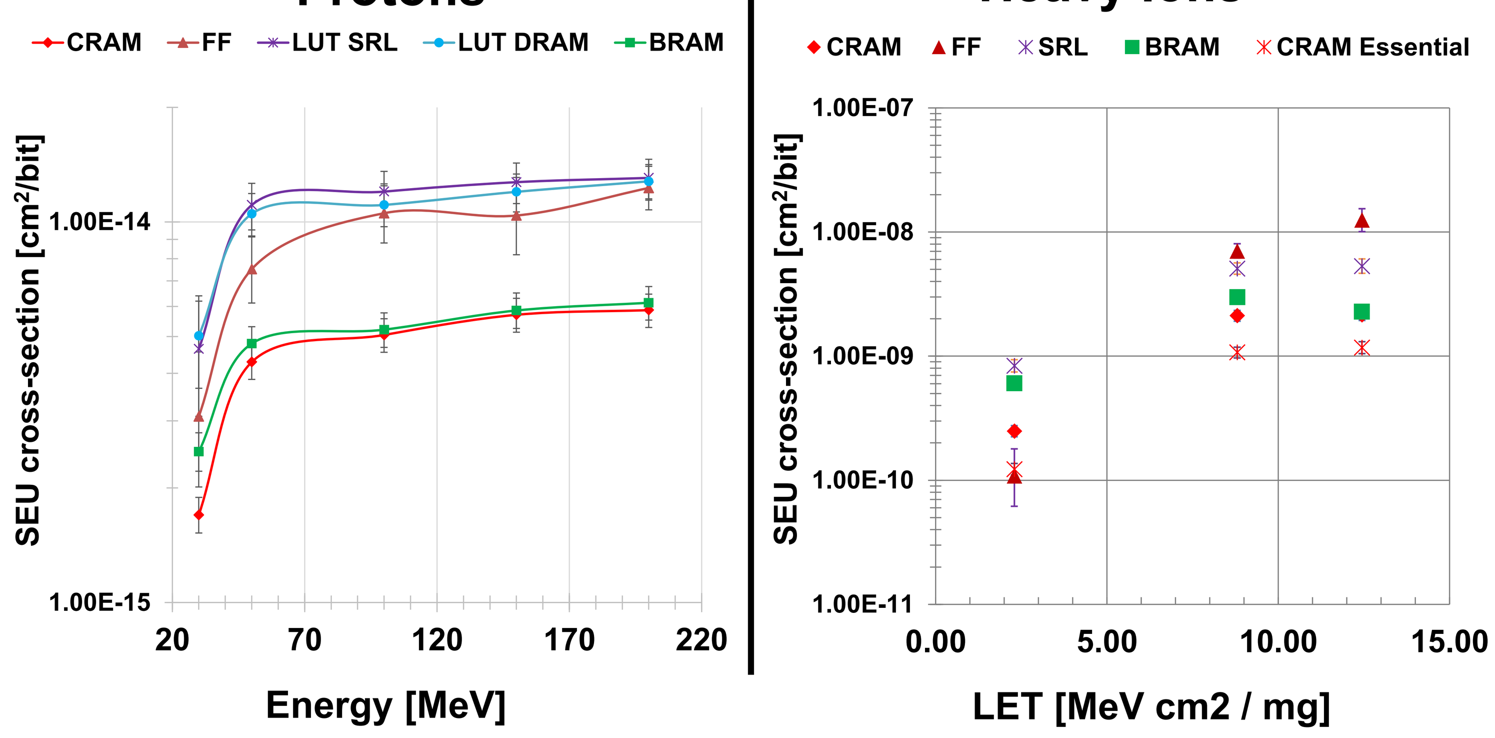
Xilinx Zynq-7000 APSoC



Accelerated radiation testing

- Paul Scherrer Institute (PSI), Switzerland (2022)
  - Protons Energies: 30 – 200 MeV
  - Programmable Logic (PL)
    - Static cross-section of Configuration RAM (CRAM), Flip-Flops (FFs), Shift Register LUT (SRLs), and BRAMs
  - Processing System (PS)
    - Static cross-section of L1 & L2 caches and On-Chip Memory (OCM)
    - Dynamic cross-section of benchmarks for various L1-I/L1-D/L2 enable/disable configurations
- CERN, Switzerland (2019) and GSI, Germany (2019, 2022)
  - Heavy-ions Linear Energy Transfer (LET): 2.30 – 12.45 MeV cm^2/mg
  - Programmable Logic (PL)
    - Static cross-section of Configuration RAM (CRAM), Flip-Flops (FFs), Shift Register LUT (SRLs), and BRAMs

SEU static cross-section of PL memories



Conclusions regarding the proton radiation testing

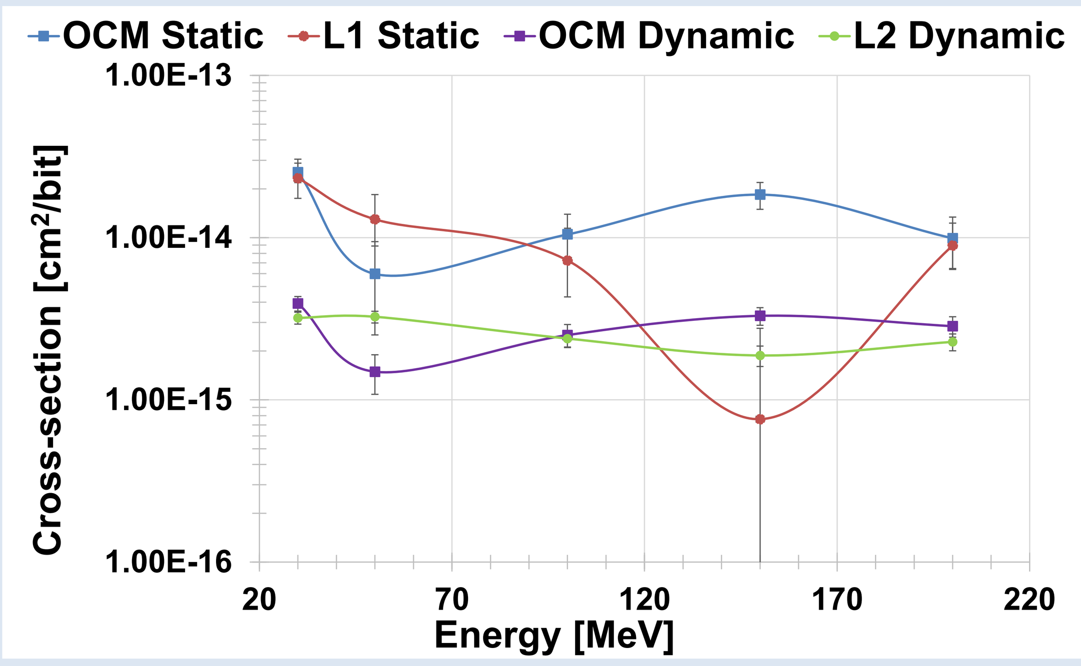
- First to report results for FFs and SLICEM LUTs
- Measured one order of magnitude higher cross-section than reported in the literature
- Cross-section of FF, LUT SRL and LUT DRAM is higher than CRAM

Upset and error rates prediction with TRAD's OMERE software

- Orbit: LEO (800 km, 98.0° inclination)
- Prediction for PL memories considers both heavy ions and protons
- Prediction for PS considers only protons

Measurements	In-flare rate [per device per day]			Out-of-flare rate		
	Heavy ions	Protons	Total	Heavy ions	Protons	Total
PL – CRAM SEUs	150	160	310	0.2190000	3.03	3.24
PL – Uncorrectable CRAM MBUs (SEM enhanced mode)	0.0005	1.47	1.47	0.0000006	0.03	0.03
PS – L2 cache SEUs	-	3.54	3.54	-	0.08	0.08
PS – SDCs - L1 & L2 (dynamic)	-	1.59	1.59	-	0.03	0.03
PS – Crashes - L1 & L2 (dynamic)	-	0.116	0.116	-	0.002	0.002
PS – SDCs - L1 only (dynamic)	-	0.019	0.019	-	0.002	0.002
PS – Crashes - L1 only (dynamic)	-	0.005	0.005	-	0.0004	0.0004

SEU static & dynamic cross-section of PS memories (Protons)



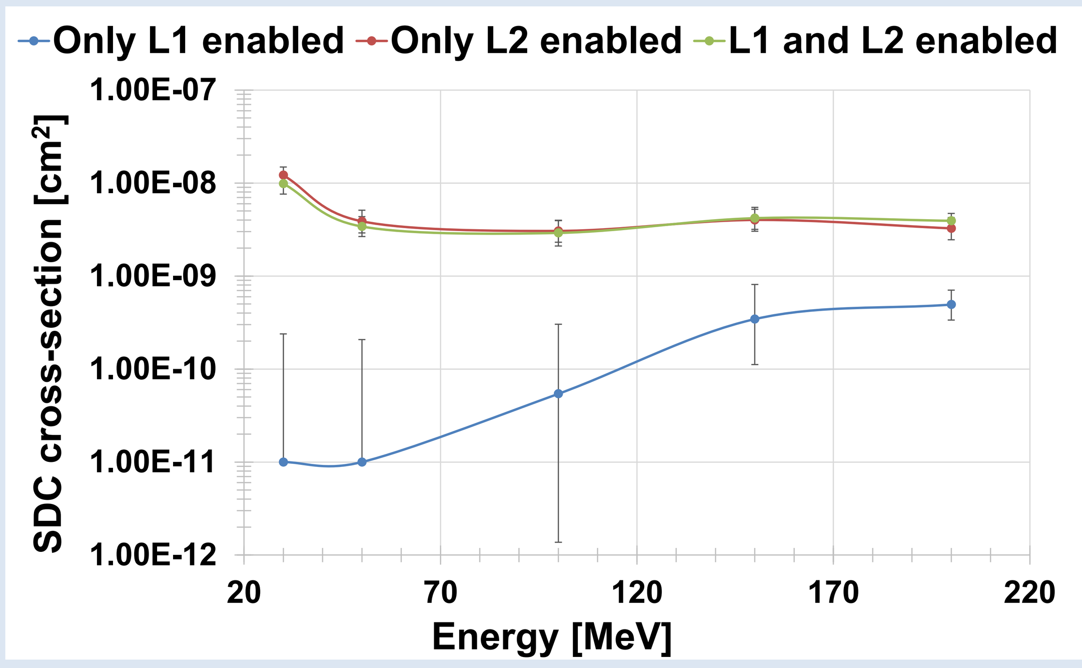
Test

- Static: One write / multiple reads
- Dynamic: March memory tests ↕ (w0); ↑ (r0, w1); ↑ (r1, w0); ↓ (r0, w1); ↓(r1, w0); ↕ (r0)

Comments

- First to report results for L1-D caches
- Highest cross-section at 30 MeV probably caused by low-energy direct ionizing
- Measured higher cross-section for L2 than reported in the literature

SDC dynamic cross-section of PS benhmarks (Protons)

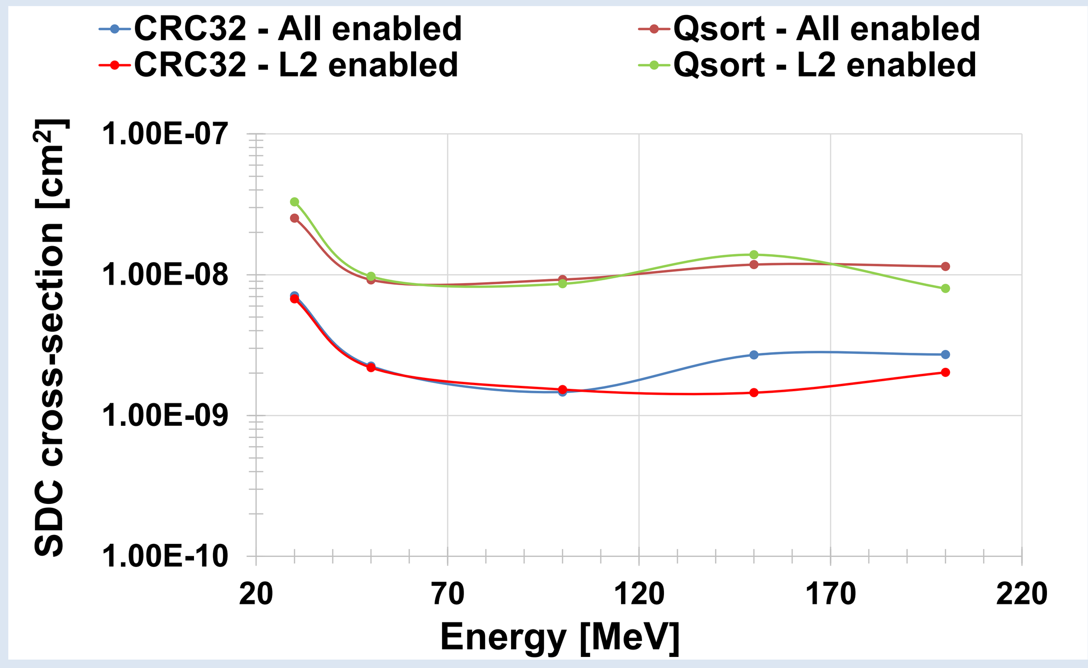


Test

- Dynamic: MiBench (CRC32, FFT, Qsort, BasicMath, SHA) and MatrixMul

Comments

- L1 cache does not deteriorate the SDC rate as much as L2
- The lower memory footprint and execution time of BasicMath, FFT, SHA and MatrixMul benchmarks compared to CRC32 and QSort result in a lower SDC cross-section



Test

- Dynamic: MiBench (CRC32, Qsort)

Comments

- CRC32 has a data segment larger than the L2 cache size, which results in frequent L2 cache replacements.
- In contrast, the data segment of Qsort fits in L2, resulting in less frequent L2 replacements.
- Thus, CRC32 has a lower SDC cross-section than Qsort, despite its larger memory footprint