COMPARISON OF A COTS FPGA IN MIDDLE EARTH ORBIT AND NUCLEAR LABORATORY

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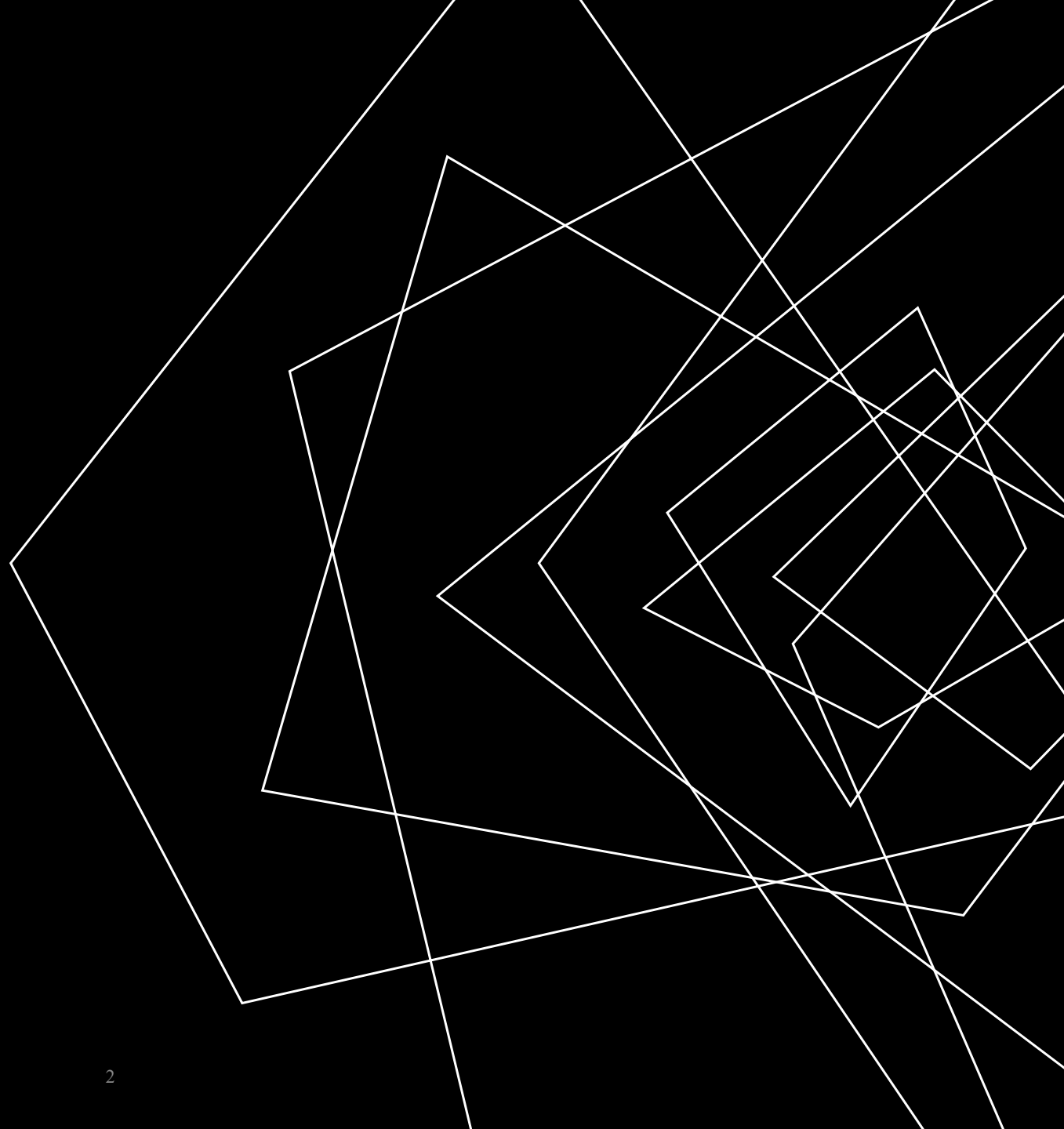
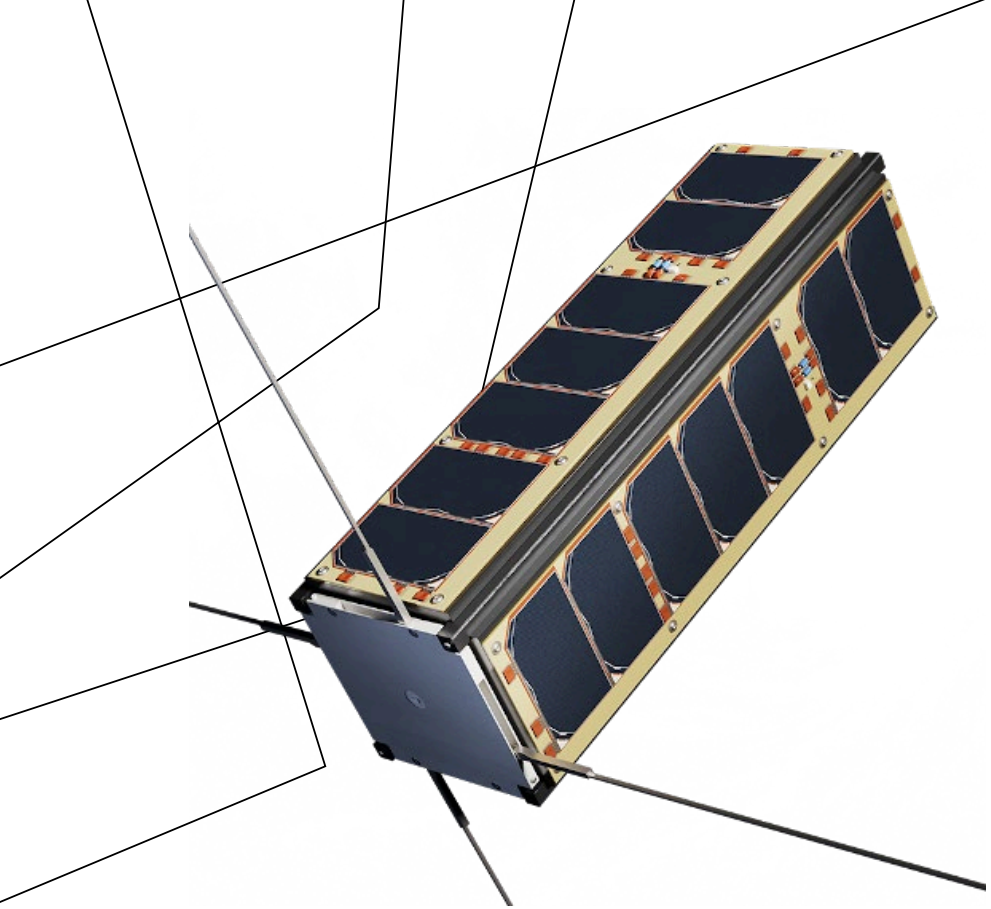
MOTIVATION

- Evaluate reliability of an FPGA functionality with three different types of TMR mitigations techniques
- Evaluate FPGA functionality with and without TMR protection onboard of TRISAT-R satellite.
- Evaluate FPGA functionality with and without TMR protection in controlled nuclear laboratory CHAMR.
- Correlation of measured data from both test campaigns





TRISAT-R SATELLITE MISSION

Mission description

- Orbit: MEO Earth orbit – altitude 5840 km – inclination 70°
- Platform: Modified NANOSky I (Skylabs)
- Launch vehicle: VEGA-C, VV21, Maiden flight, French Guiana on 29th of May. Duration of the mission 246 days

Satellite characteristics

- Class: Nanosatellite, standard 3U form factor
- Mass: 5.033 kg
- Dimensions: 11 x 12 x 34 cm (stowed), 111 x 48 x 34 cm (deployed antennas)
- Attitude control: 2-axis (optionally 3-axis) stabilized (3 magnetorquers, solar and highly sensitive magnetic field sensors)
- Power: 30 Wh battery, fixed solar panels
- Communication: VHF (GFSK, adjustable baud rate), UHF (GFSK, adjustable baud rate)

TRISAT- R SATELLITE MISSION

Onboard subsystems

- NANOeps with 30 Wh battery pack
- NANOcomm TM/TC communication subsystem
- NANOobc Fault tolerant on-board computer
- Attitude Determnination and Control Interface Module

Onboard subsystems

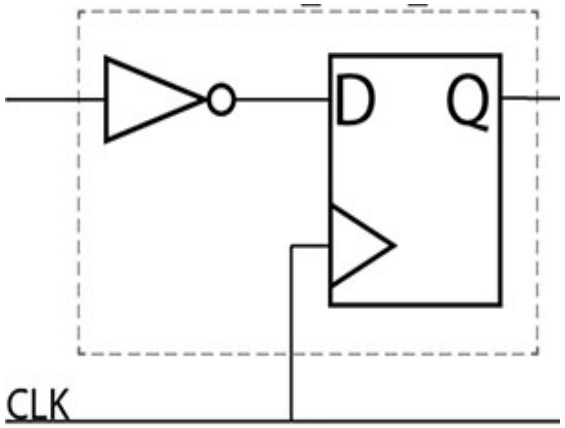
- SpaceRadMon (CERN)
- CHIMERA (ESA)
- NANOhpm (SkyLabs)
- NANOlink (SkyLabs)
- Additional instruments:
  - FGDOS - calibrated redundant Floating Gate Dosimeter
  - TID Monitor
  - Ultra miniaturized color cameras with resolution of 320 x 320 pixels

GROUND SEGMENT

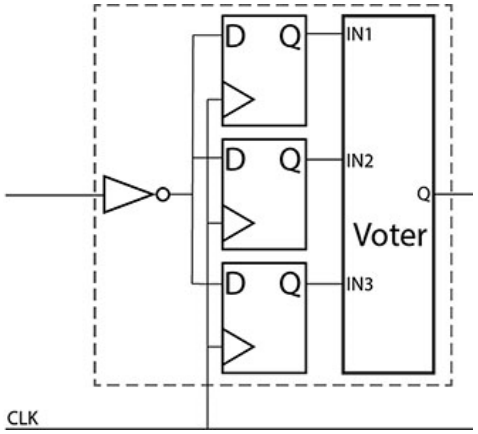
- Location: Maribor, Slovenia
- Communication: VHF UL, UHF DL
- Antenna: Yagi Array (VHF/UHF)
- Control: 2-axis tracking
- Radio: VHF/UHF SDR

FPGA IMAGES – CHAIN LINKS

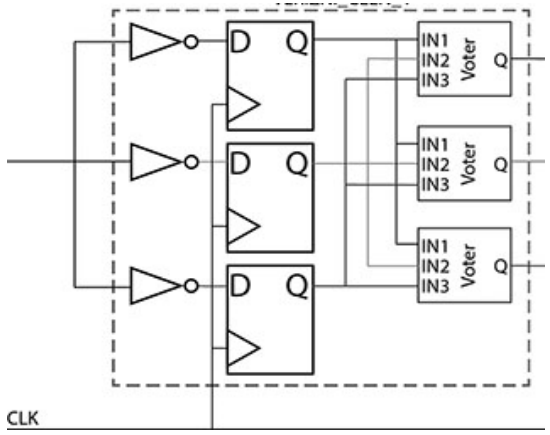
NO TMR



PARTIAL TMR



FULL TMR



FPGA IMPLEMENTATION

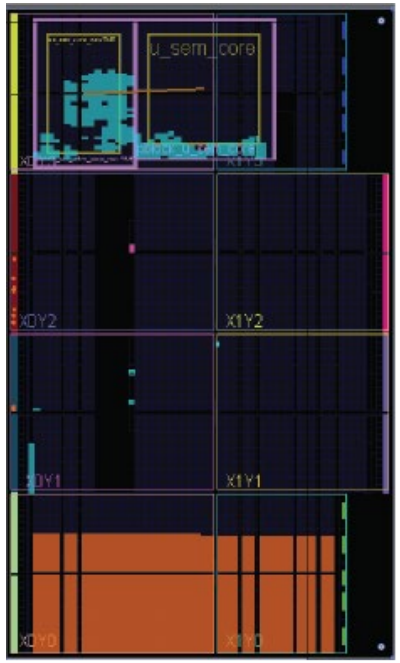


Figure above shows a floorplan in Artix-7 when non-protected Snake architecture RTL is implemented

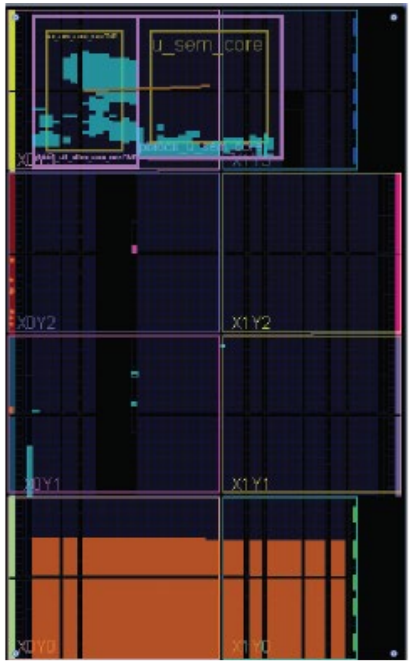


Figure above shows a floorplan in Artix-7 when partial-protected

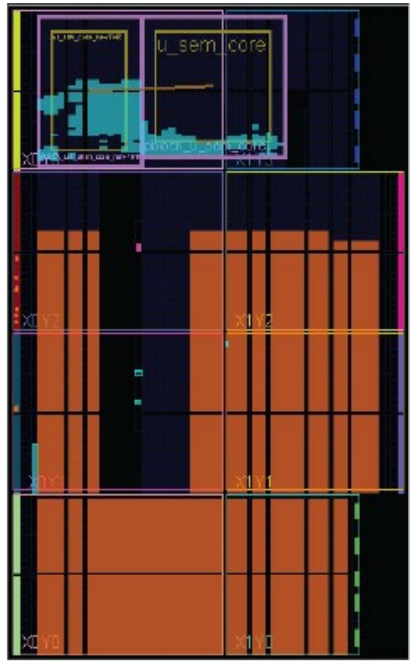
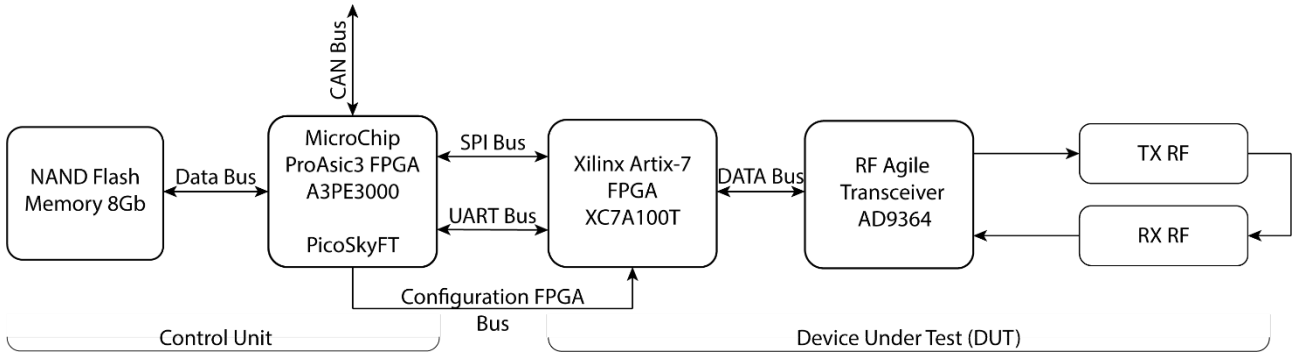
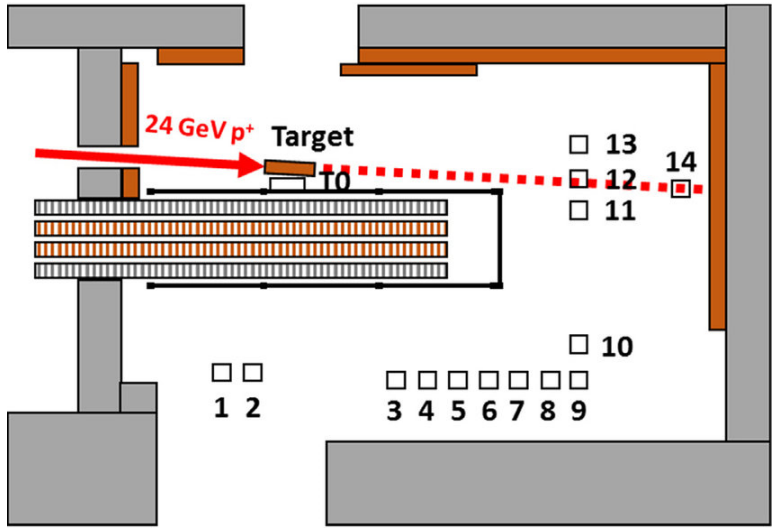


Figure above shows implementation of full-protected snake architecture

EVALUATION PLATFORM: NANOLINK (SKYLABS)

- COTS Xilinx Artix-7 FPGA – Device Under Test (DUT)
- MicroChip (MicroSemi) ProAsic3 FPGA with PicoSkyFT – Monitoring and Controlling device
- NAND FLASH memory





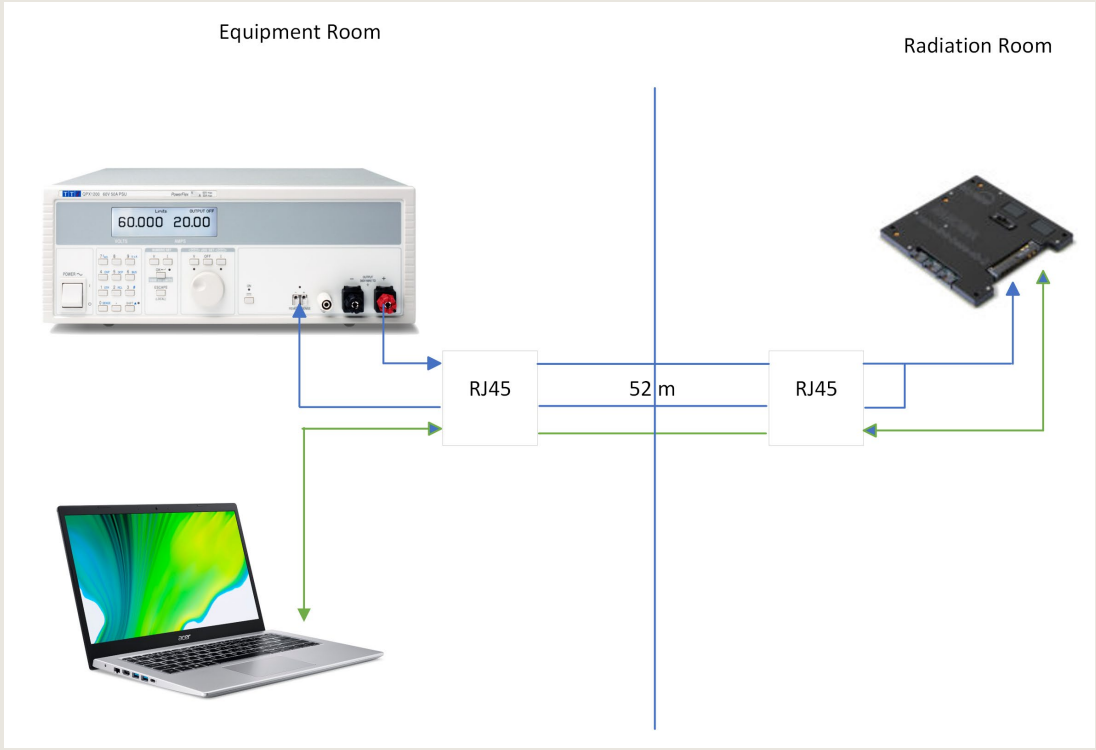
CHARM – MIXED FIELDS RADIATION FACILITY

Irradiation campaign was supported by RADNEXT project.

Irradiation campaign

- Duration: 7 days
- Max dose – TID (Gray): 398 Gray
- Max HEH Fluence (cm^{-2}): 1.01×10^{12}
- Thermal neutrons (eV): 5.38×10^{11}
- Position: 6

CHARM - SETUP



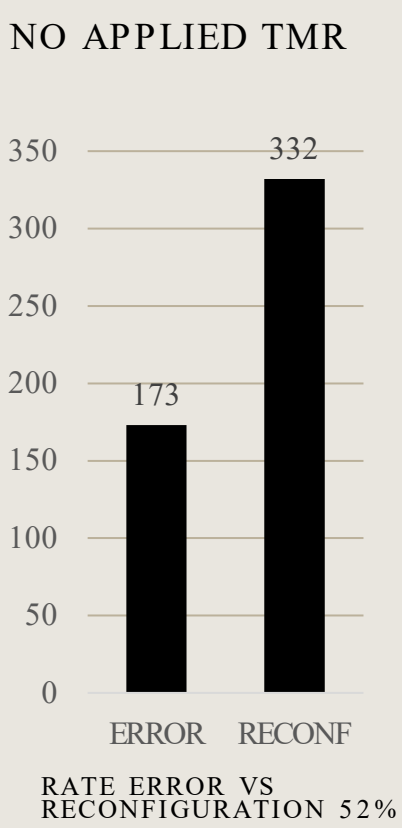
- NANOlink (SkyLabs)
- TTY power supply
- Personal computer with python script

MEASUREMENTS DURING IRRADIATION TEST

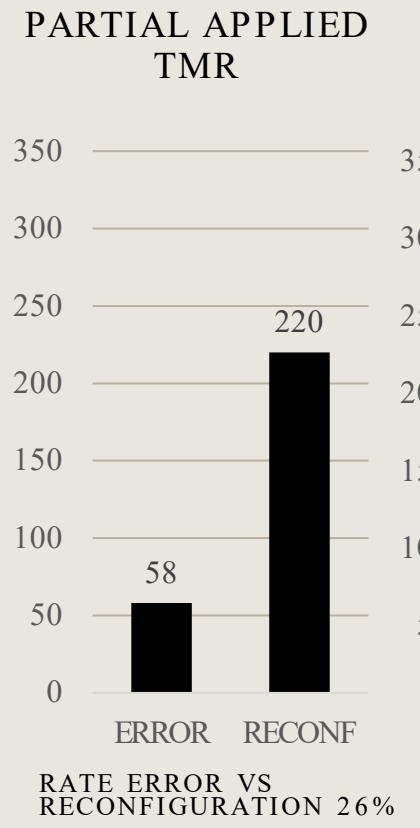
- Number of Single Event Transients (SET) in the chain links
- Number of Multiple Bit Upsets (MBU) in the configuration memory
- Number of reconfigurations
- Power consumption
- Latch-ups

FPGA RECONFIGURATION DURING IRRADIATION TEST

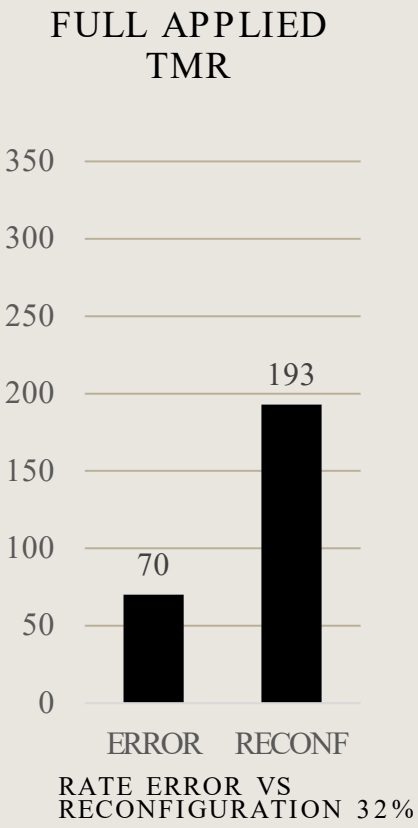
ERROR AND RECONFIGURATIONS		
RTL DESIGN WITH APPLEID TMR	RECONFIGURATIONS	RECONFIGURATIONS DUE TO ERRORS
NO	332	173
PART	58	220
FULL	70	193



RATE ERROR VS RECONFIGURATION 52%

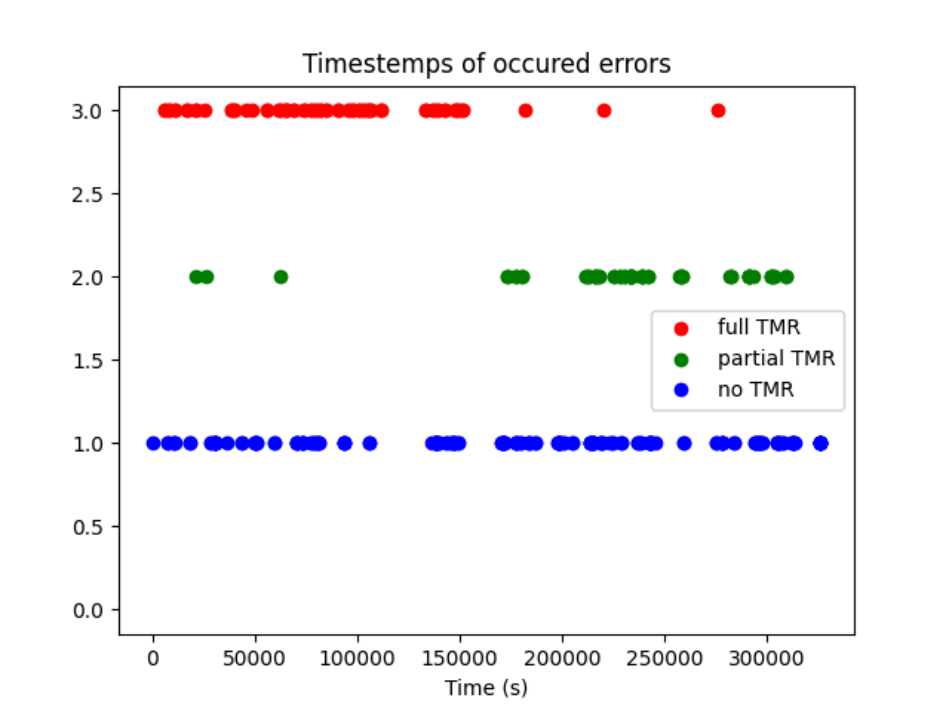


RATE ERROR VS RECONFIGURATION 26%

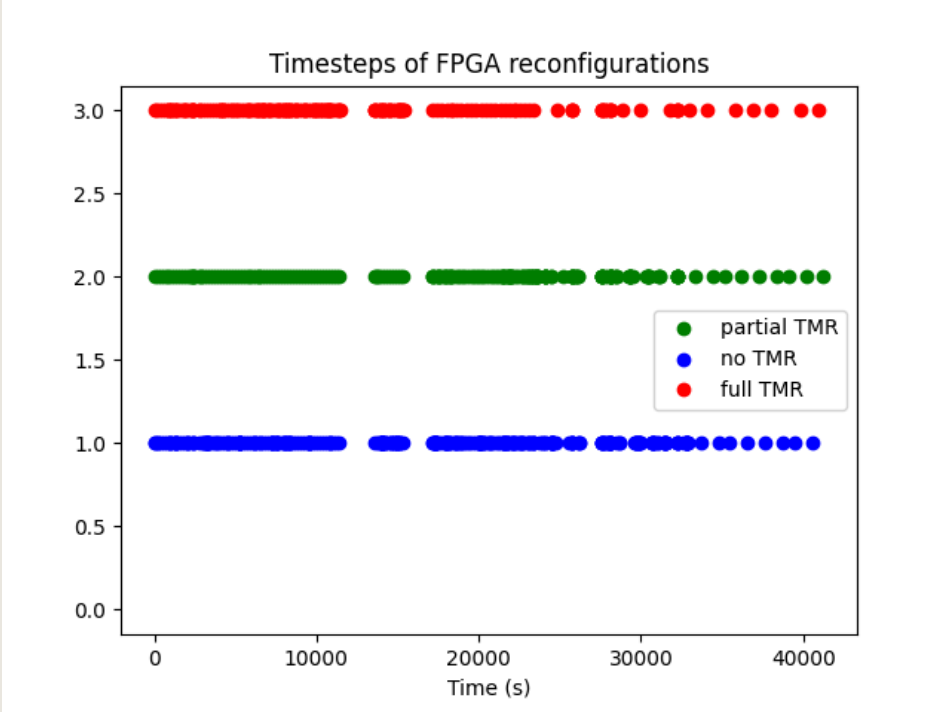


RATE ERROR VS RECONFIGURATION 32%

TIMESTAMPS WHEN ERROR OCCURRED

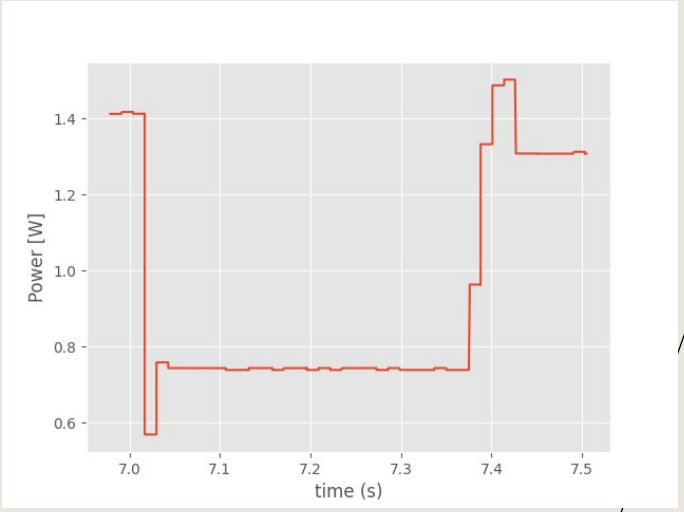


TIMESTAMPS OF RECONFIGURING THE FPGA



POWER CONSUMTION AND LATCH- UPS

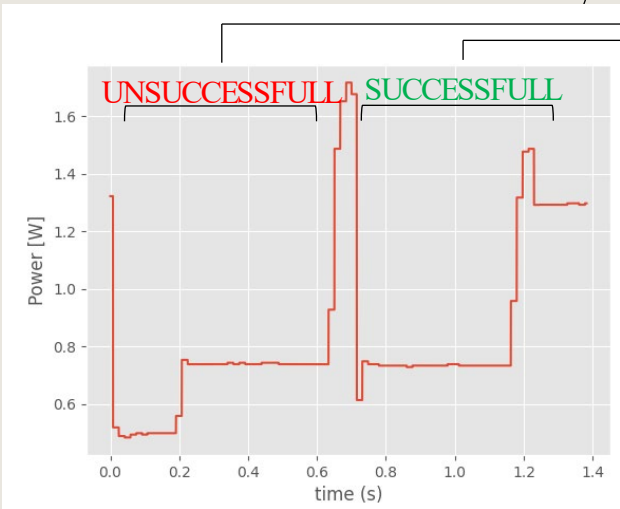
During the irradiation test two events were indicated as Latch-up in DUT



Graph shows the profile of power consumption during reconfiguring the FPGA

Reading image A from NAND flash

Reading image B from NAND flash



Graph shows the profile of power consumption during unsuccessful reconfiguration and followed by successful FPGA reconfiguration.

POWER CONSUMTION	Minimum power [W]	Average power [W]	Maximum power [W]
Configuring FPGA	1.452672	1.52960	1.717592
Normal operation	1.153152	1.31336	1.442977

CONCLUSION

- CHARM IRRADIATION TEST IS COMPLETED AND GAINED TEST DATA PROCESSED.
- PARTIAL TMR MITIGATION TECHNIQUE HAD BETTER PERFORMANCE IN PROTECTING OF RTL FUNCTIONALITY IN FPGA COMPARED TO FULL AND NO APPLIED TMR.
- NAND FLASH MEMORY REQUIRED MORE POWER TO EXECUTE READ COMMAND AFTER LONGER EXPOSURE TO RADIATION PARTICLES.
- DURING IRRADIATION CAMPAIGN, ALL FPGA IMAGES STAYED UNCORRUPTED.
- EXPERIMENT ON TRISAT-R IS STILL ONGOING, AND WE ARE WAITING FOR A TIME SLOT

THANK YOU FOR YOUR TIME