



High-Performance UVM Verification IP for SpaceWire Codec

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- Introduction
- UVM-based SpaceWire Codec Twin Model
- UVM-based Verification Environment Architecture
- Verification Campaign
- UVM-based Approach Advantages
- Results and Conclusions
- Q&A

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Functional Verification of any SpaceWire Codec,
Fully compliant with Universal Verification Methodology (UVM)**

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- Developed by IngeniArs S.r.l.



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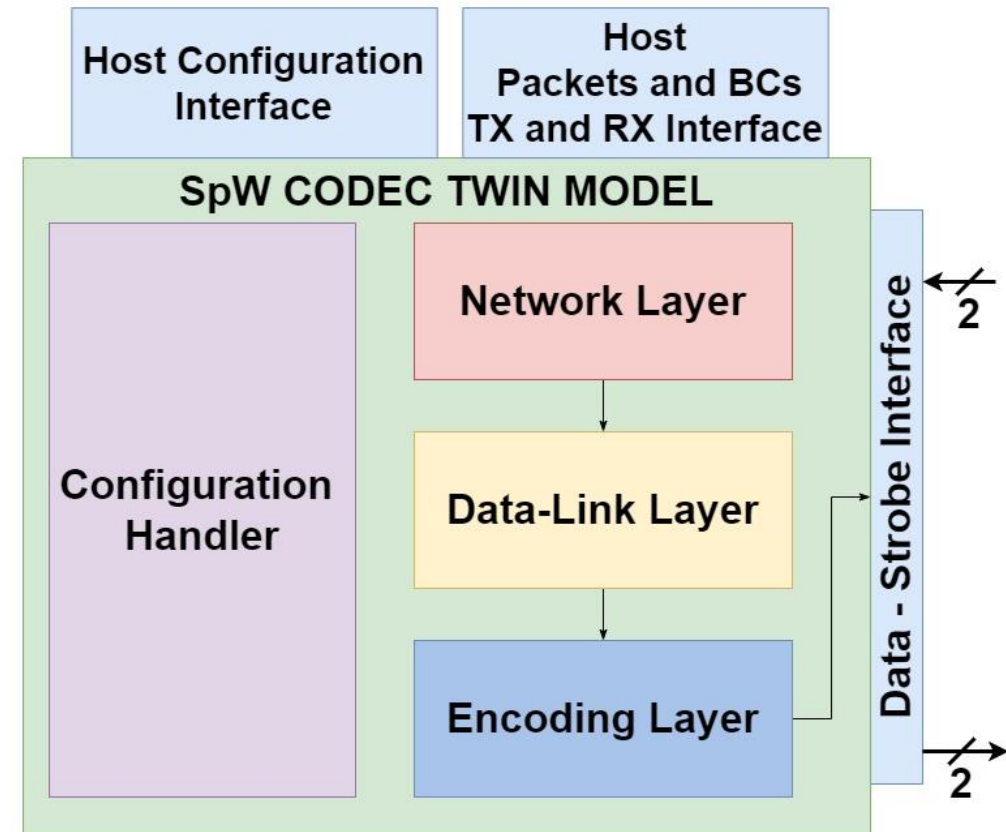
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Promotion of UVM-based Verification Approach

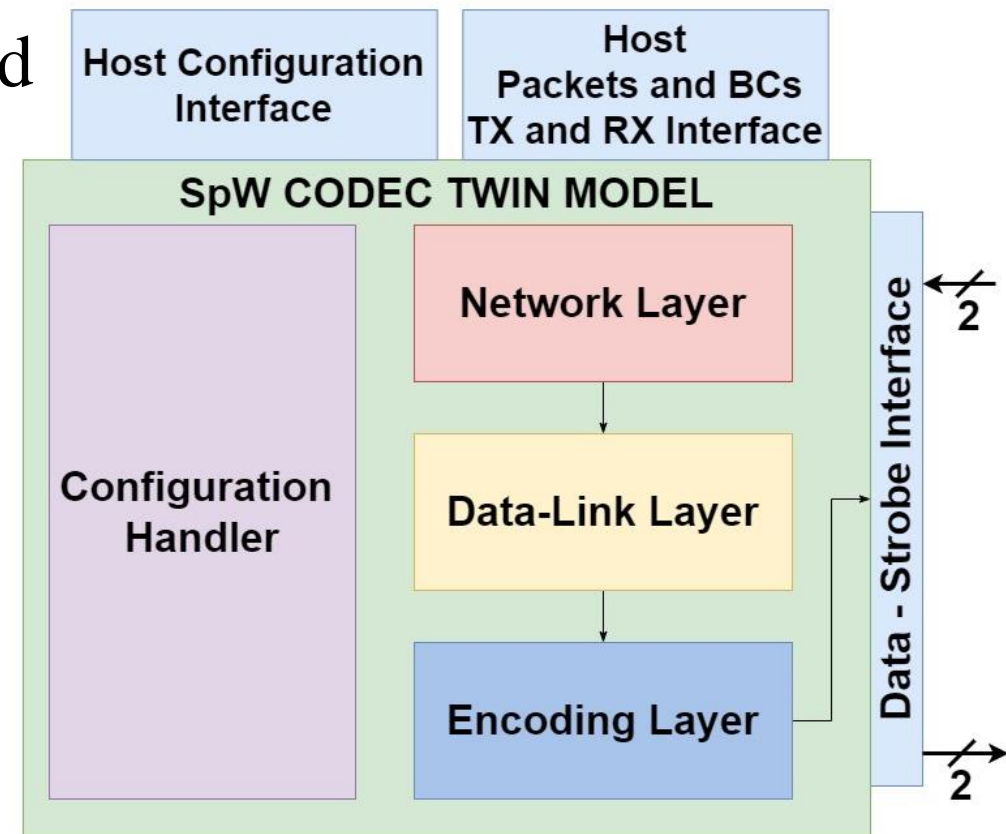
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- Emulates the ideal behavior of a SPW Codec



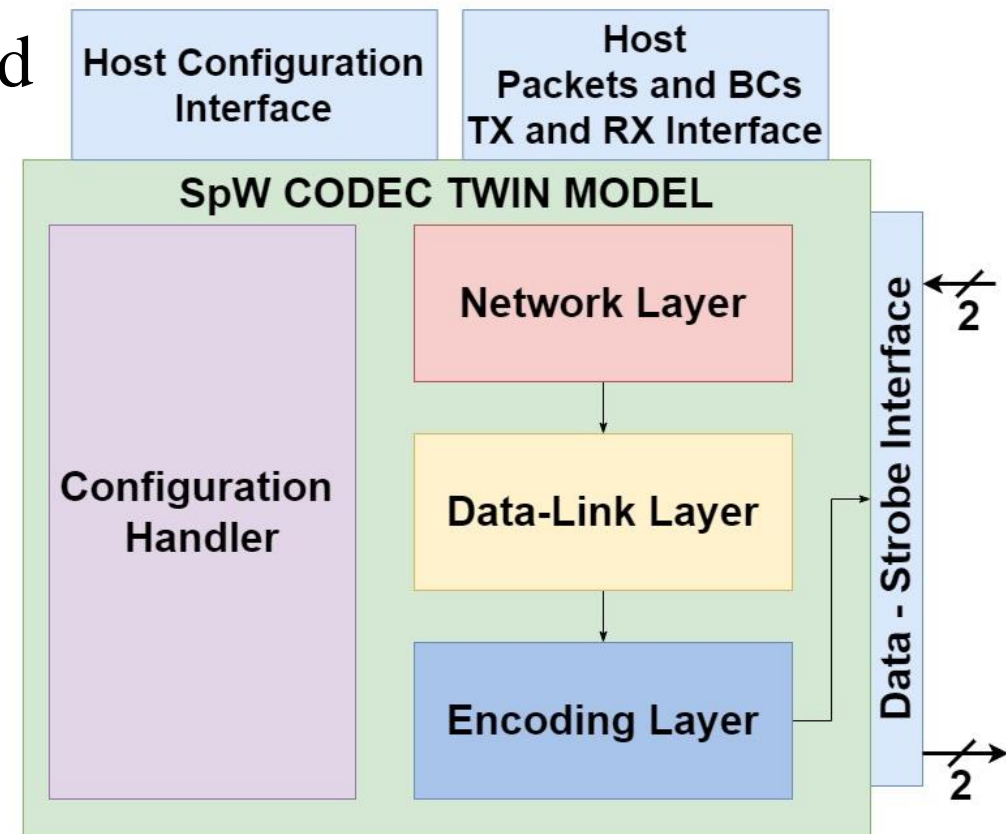
UVM-BASED SPACEWIRE CODEC TWIN MODEL

- Emulates the ideal behavior of a SPW Codec
- Fully compliant with Rev.1 of SpW Standard



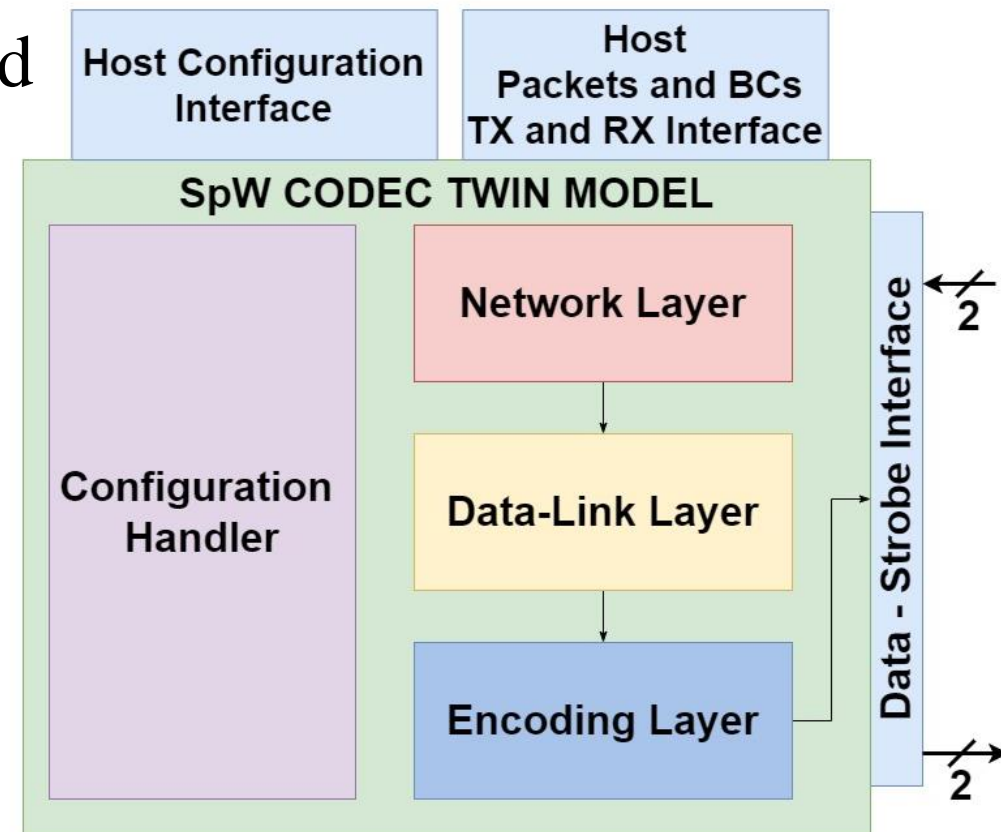
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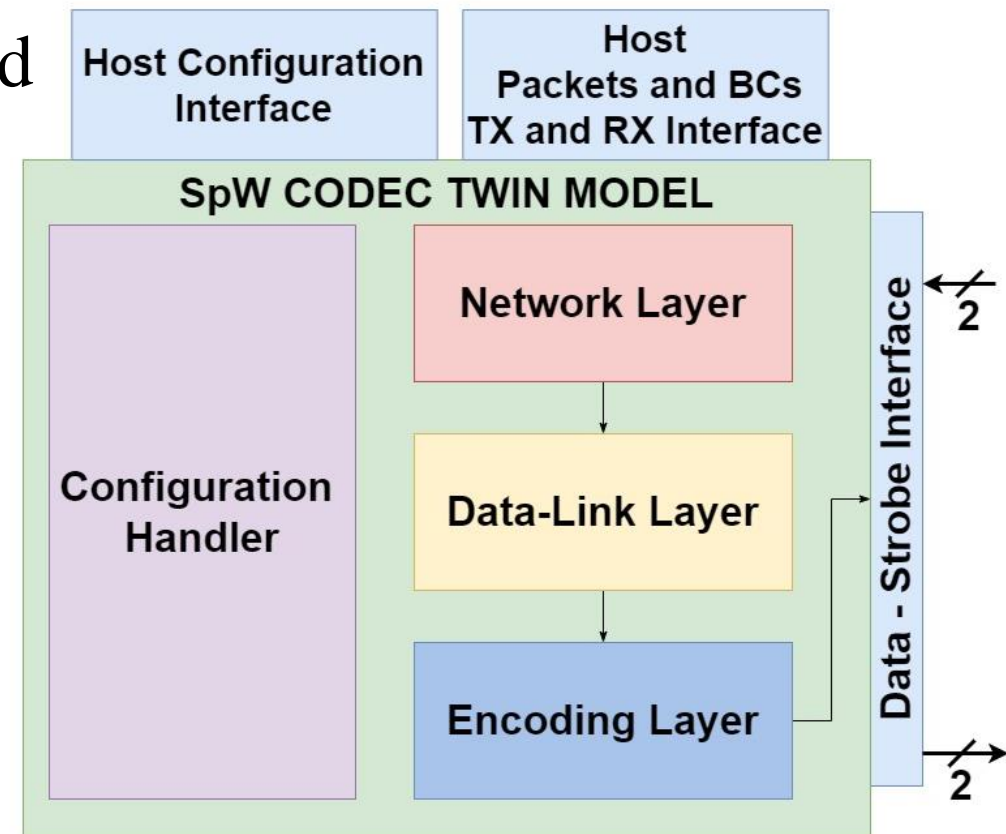
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- Fully compliant with UVM
 - Easily reusable and maintainable



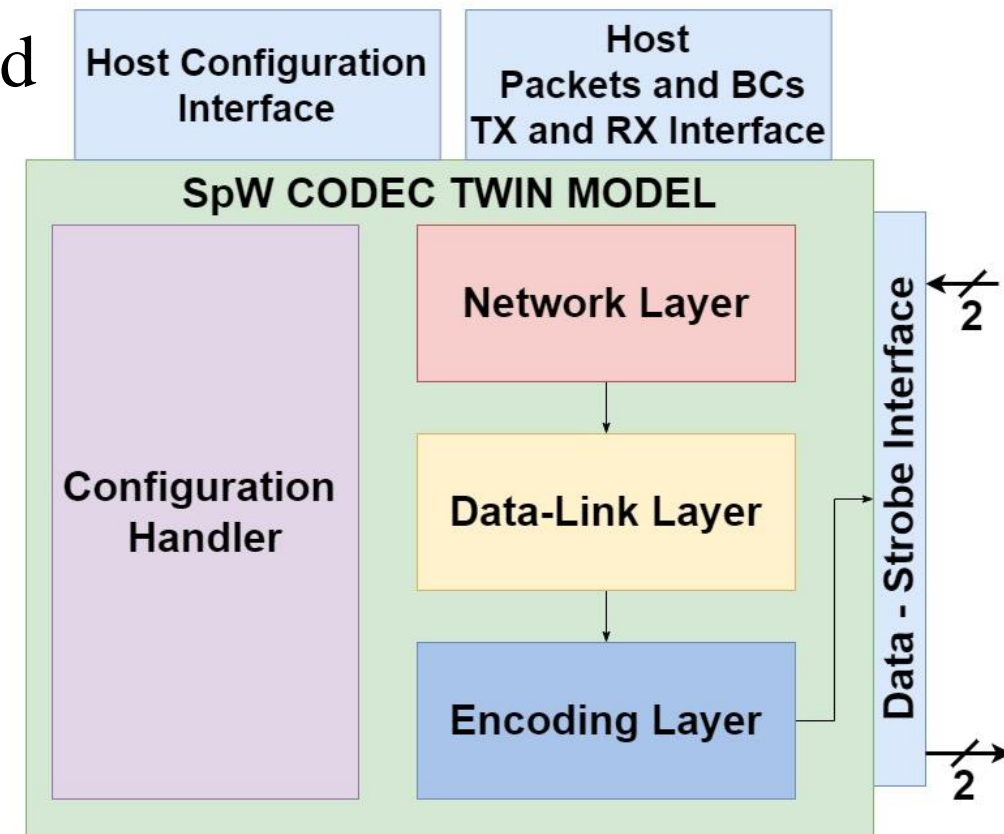
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- Host interface
 - Packets and BC transmission and reception
 - Configuration changes and readings

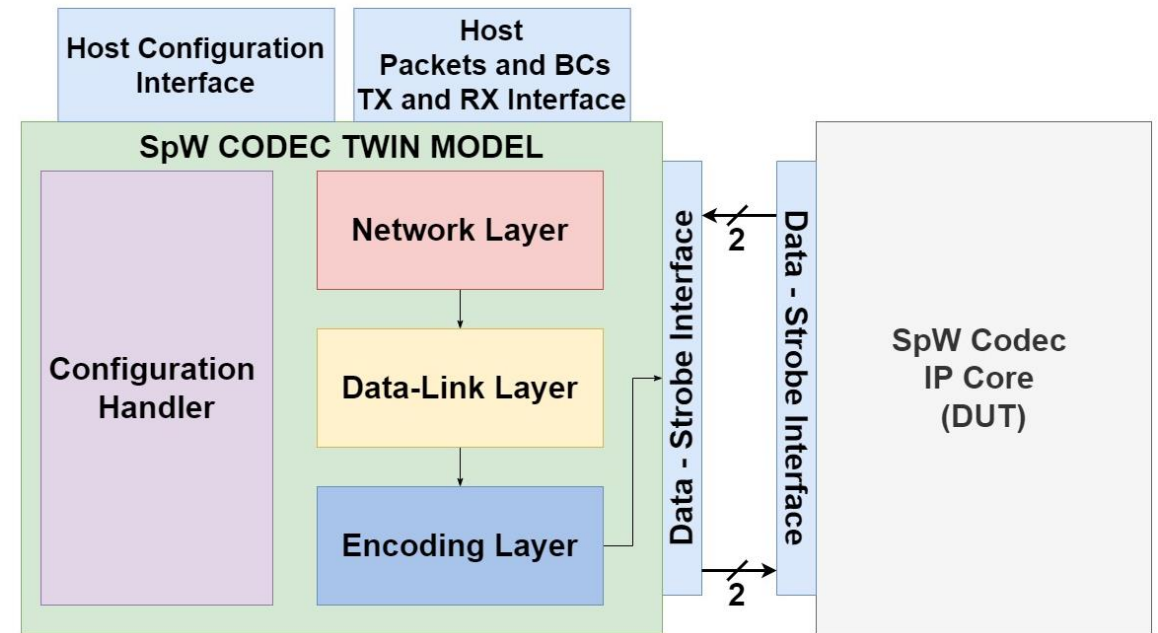


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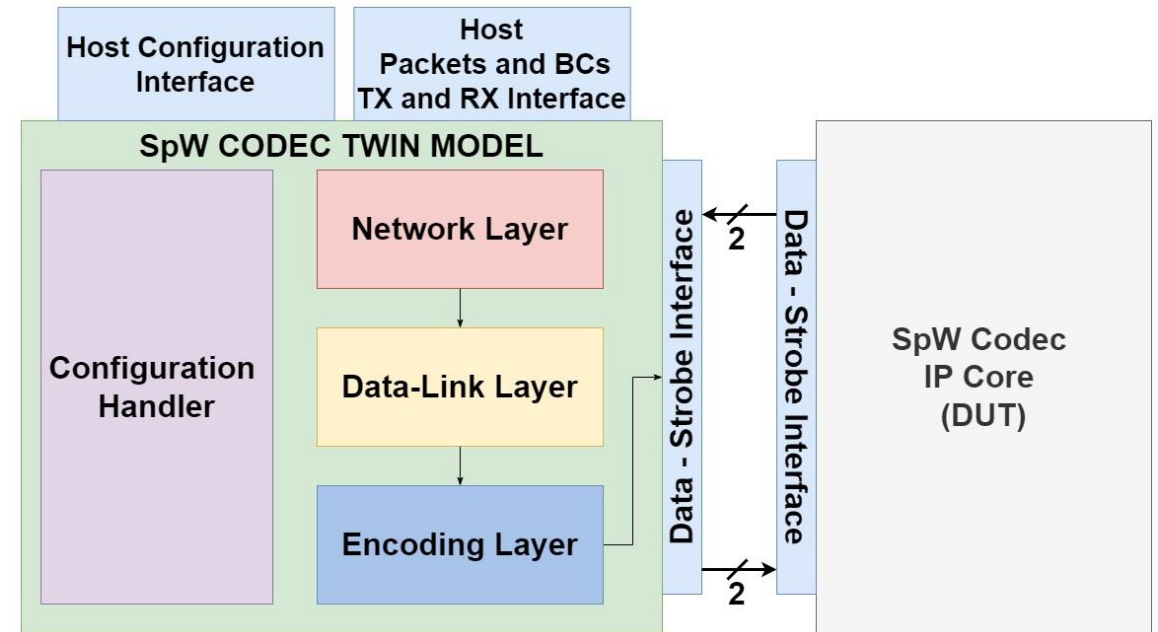
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- Data-Strobe interface
 - Communication with DUT or any system with SpW interface



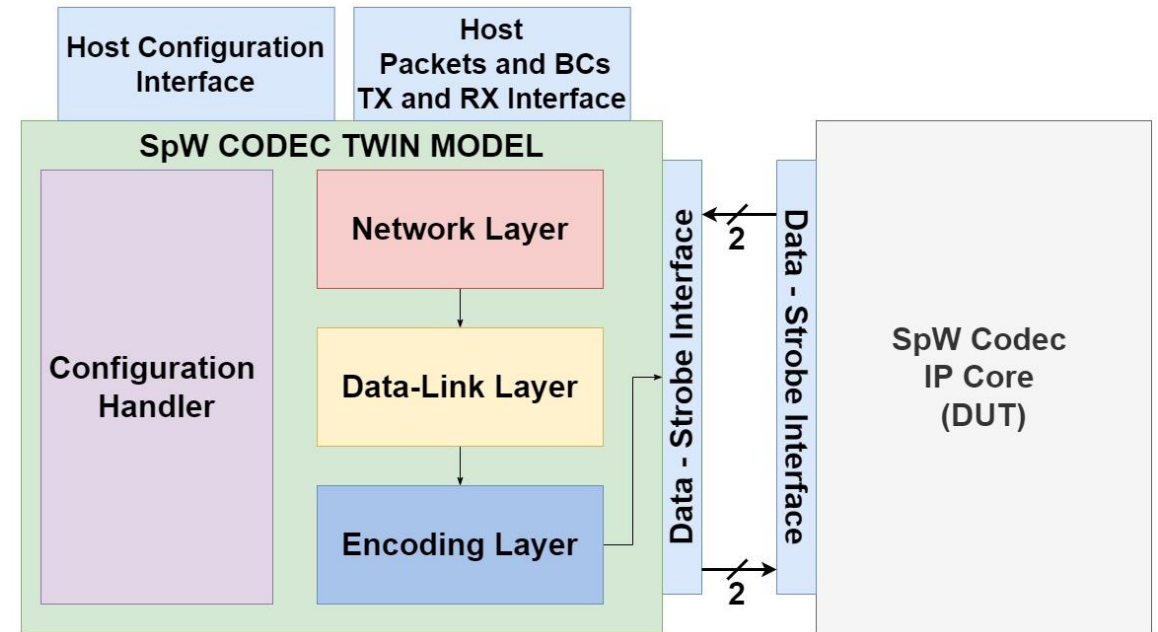
- Direct Communication with DUT



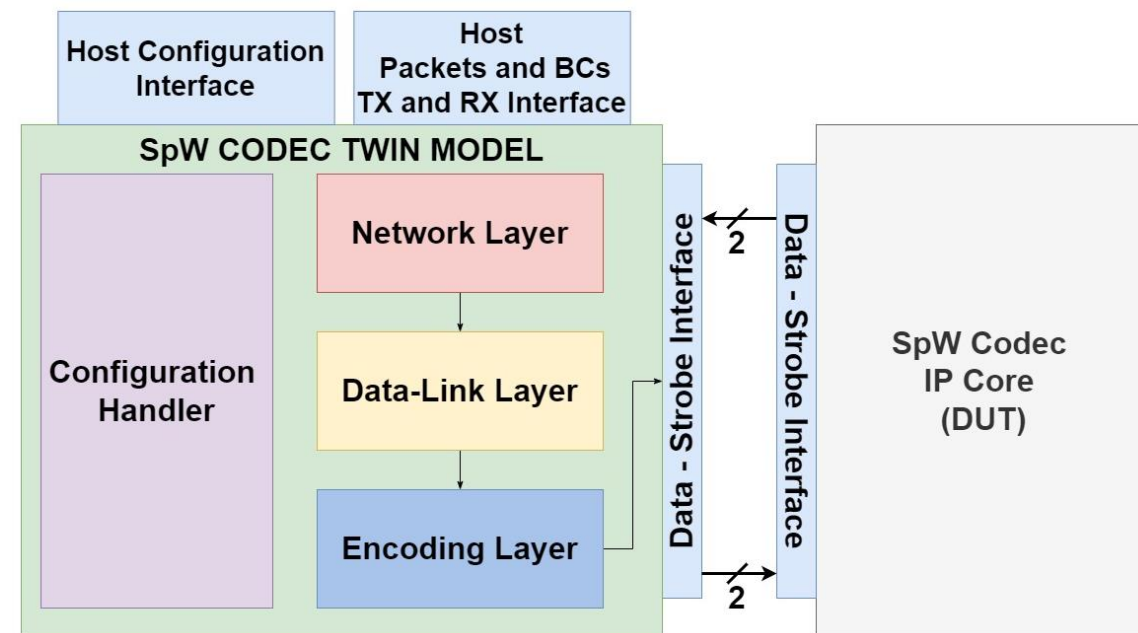
- Direct Communication with DUT
 - Automatic link initialization



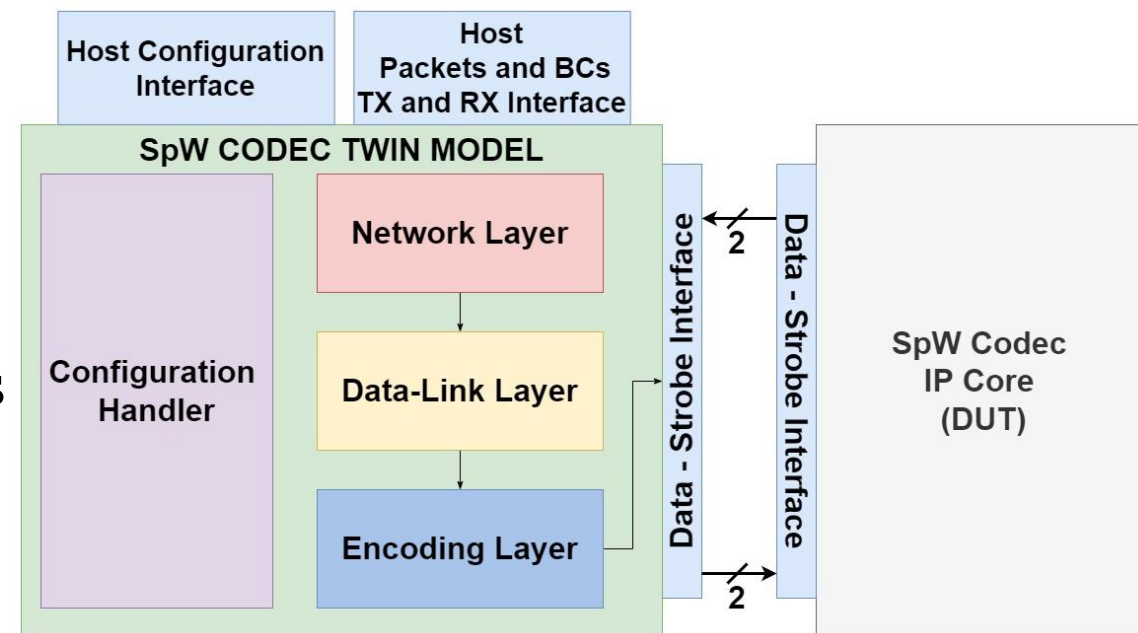
- Direct Communication with DUT
 - Automatic link initialization
 - Automatic TX and RX credit handling



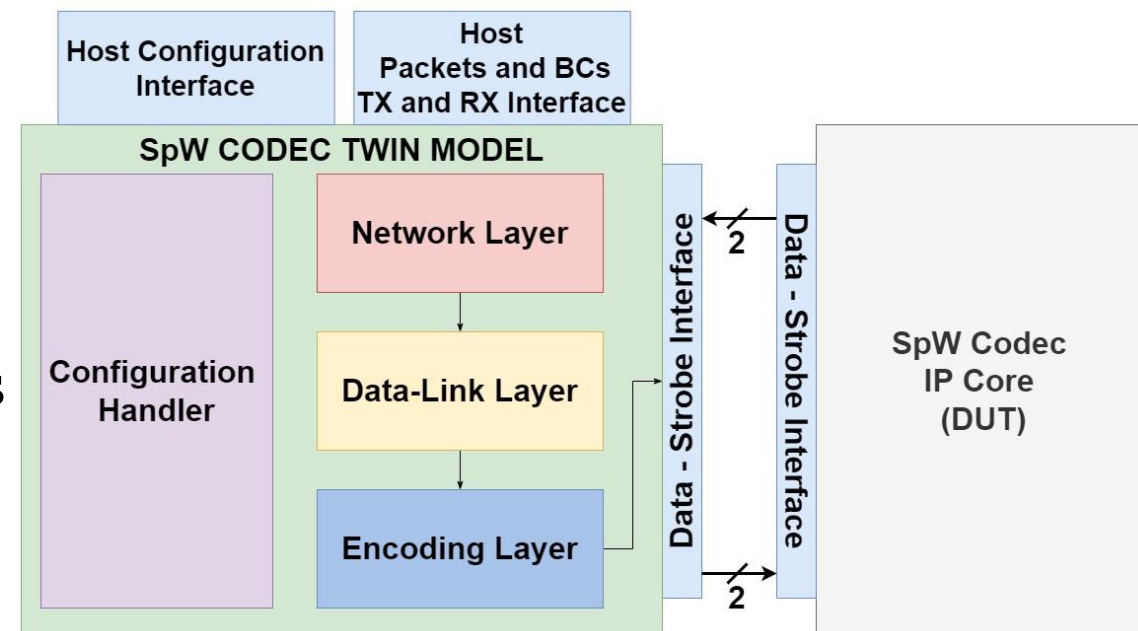
- Direct Communication with DUT
 - Automatic link initialization
 - Automatic TX and RX credit handling
 - Automatic TX of NULLs when needed



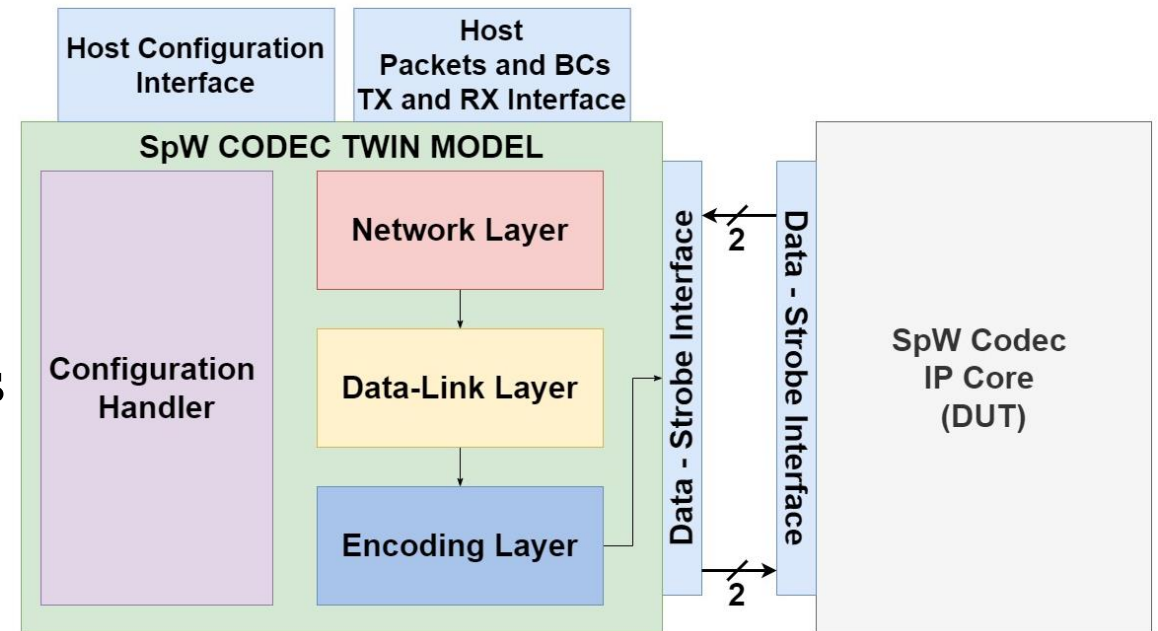
- Direct Communication with DUT
 - Automatic link initialization
 - Automatic TX and RX credit handling
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 - Automatic recognition of all types of errors



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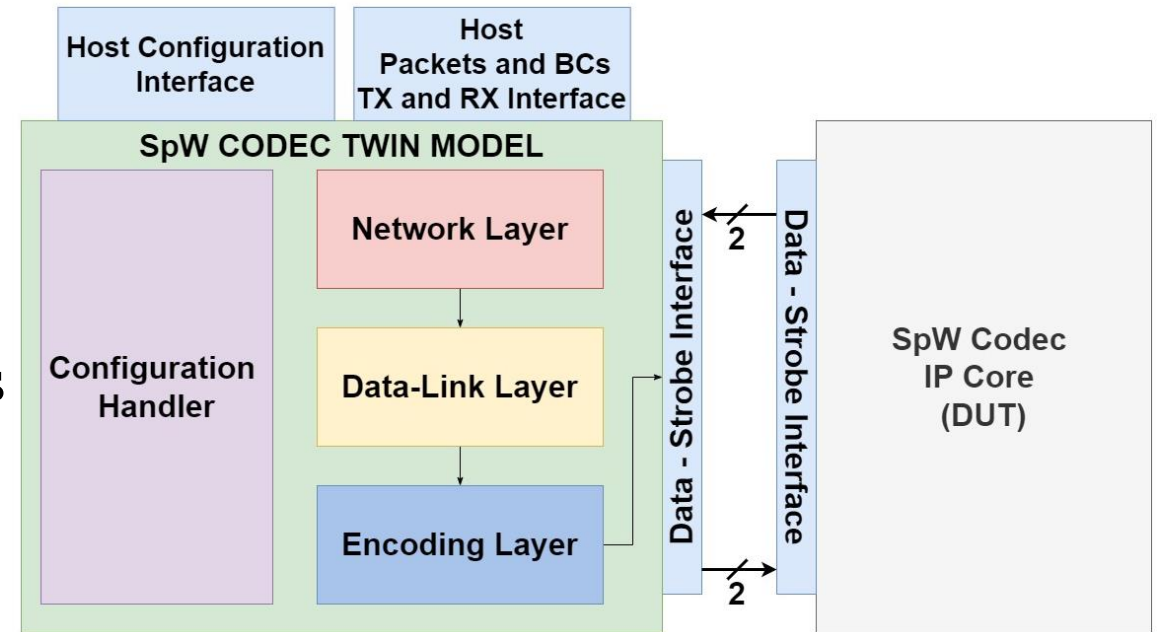


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- Higher level of abstraction
 - Only packets and BCs to be defined



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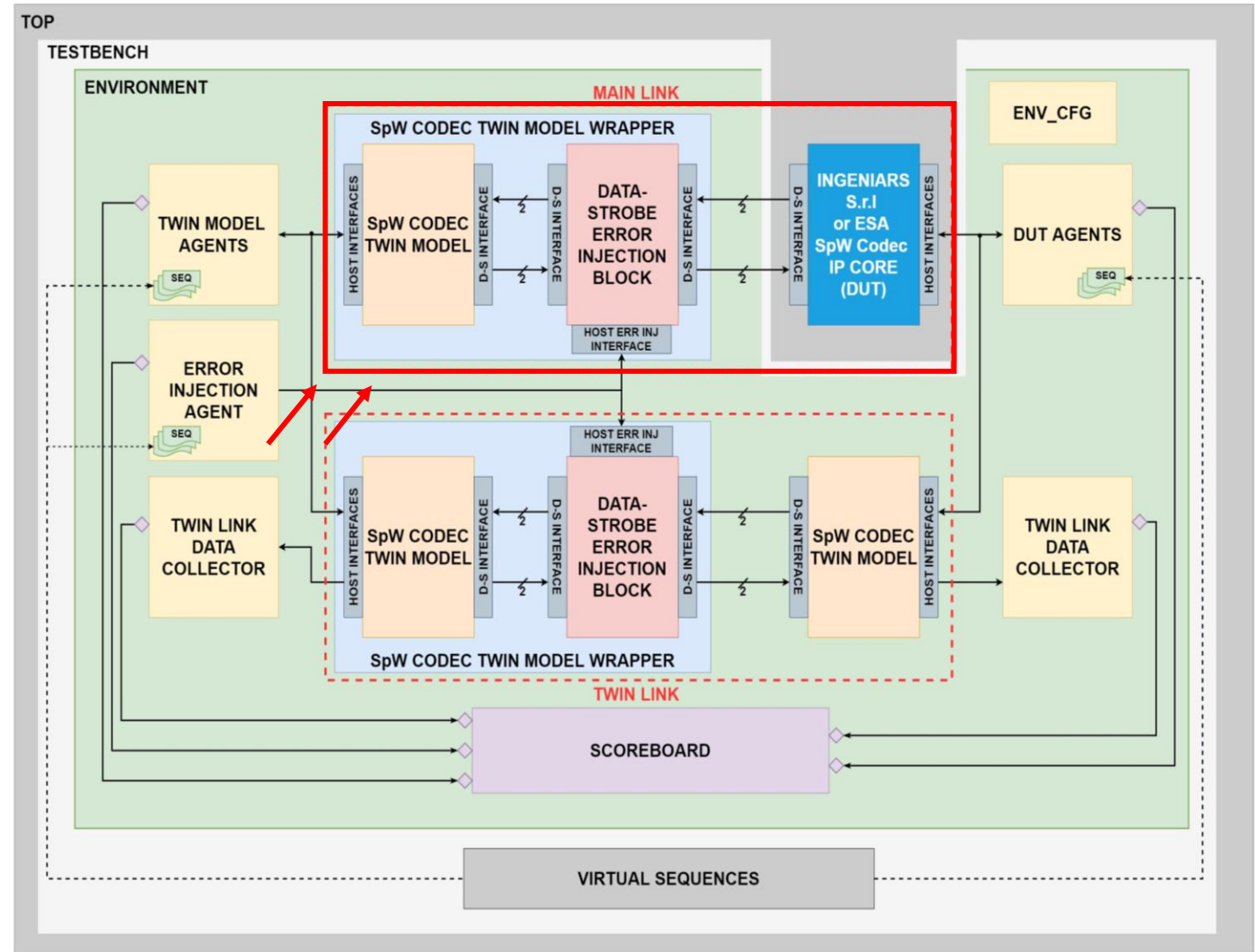


Significant Simplification of the Verification Process
Significant Reduction in Verification Time and Cost

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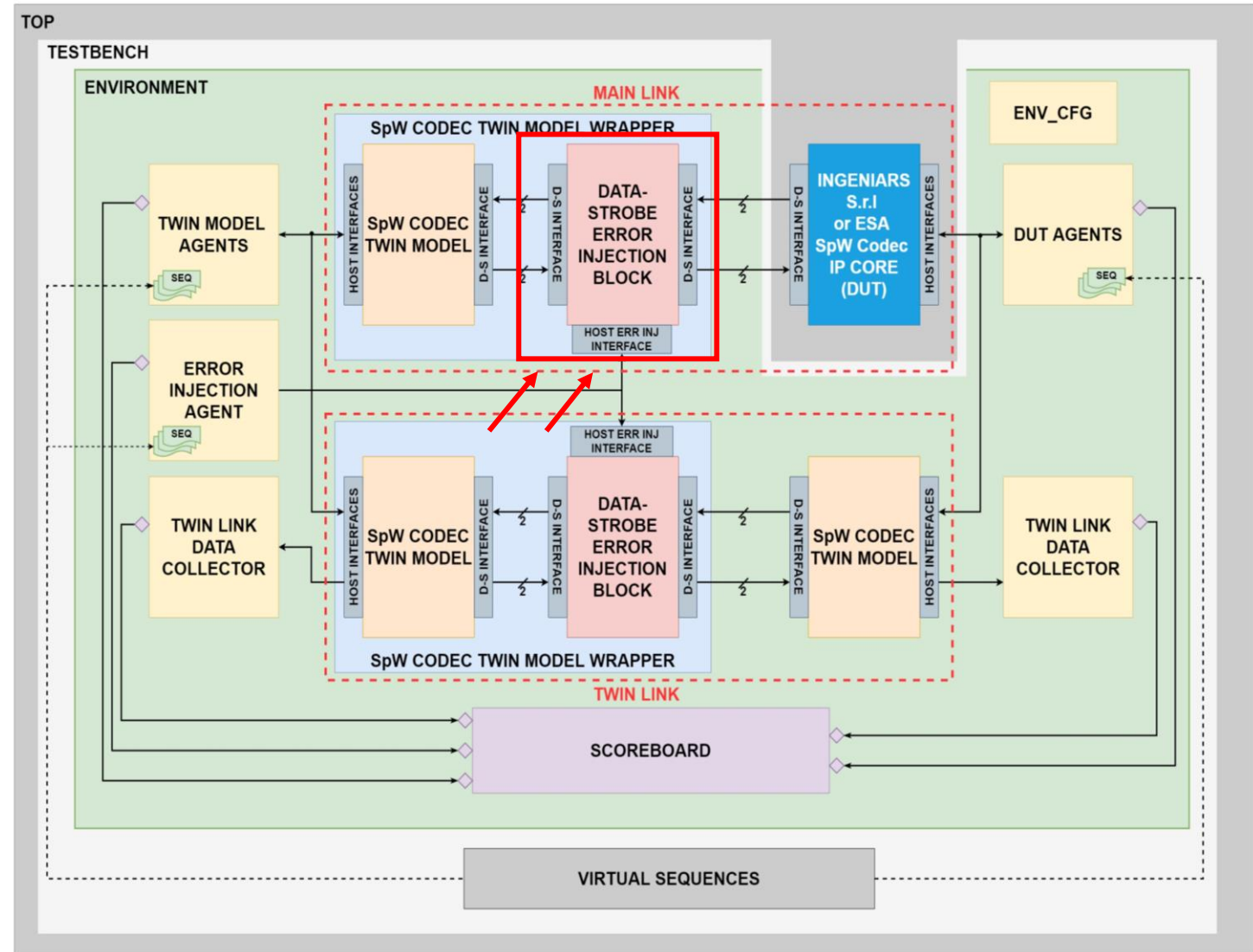
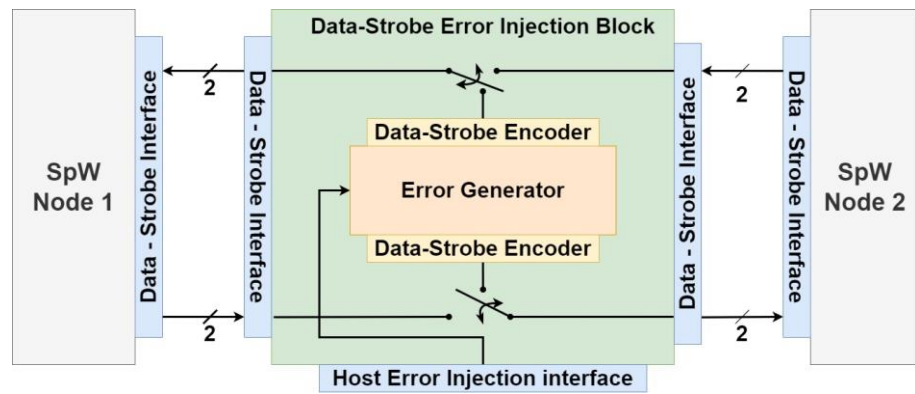
UVM-BASED VERIFICATION ENVIRONMENT ARCHITECTURE

- Main Link
 - Communication between DUT and Twin Model



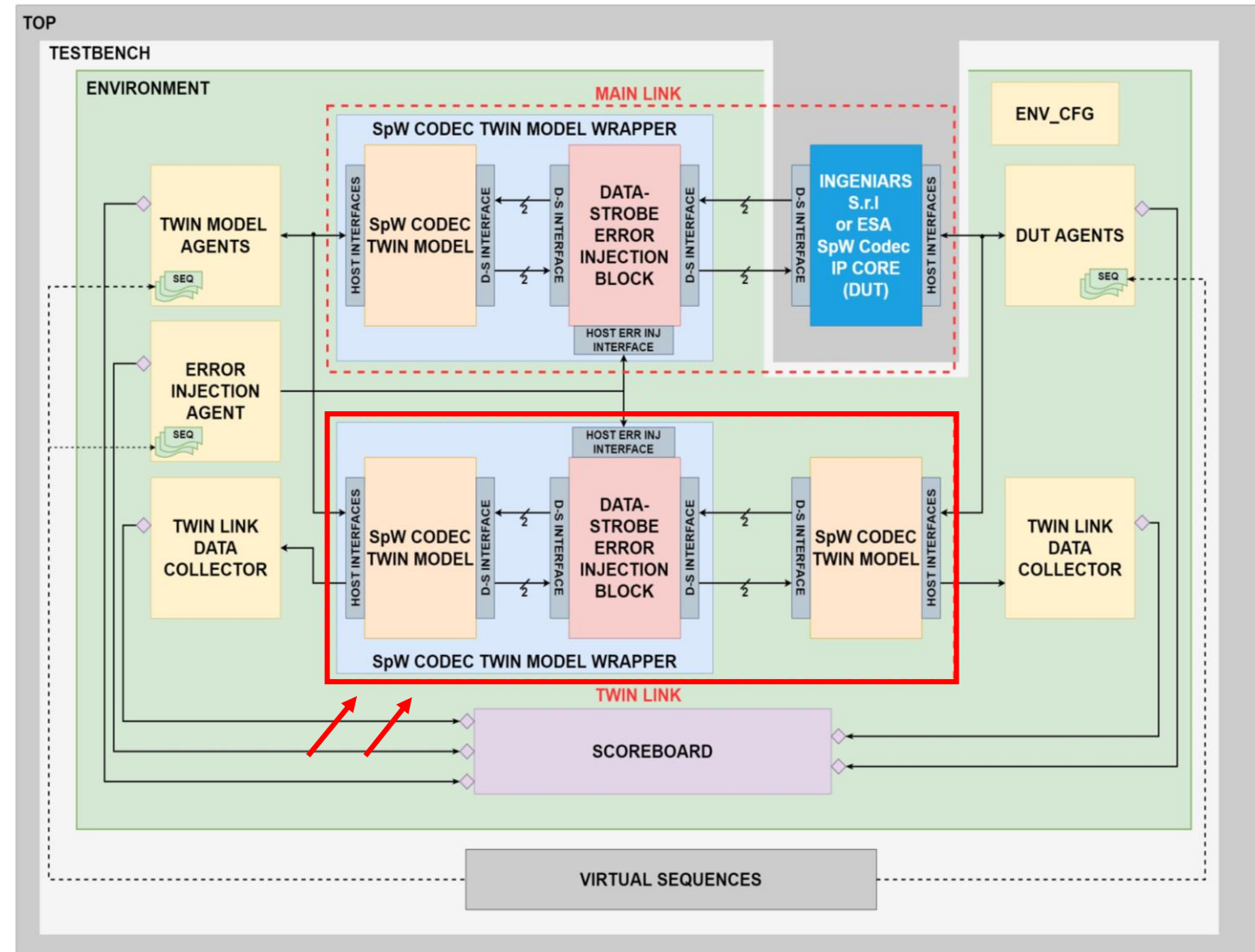
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 - Communication between DUT and Twin Model
 - Data-Strobe Error Injector



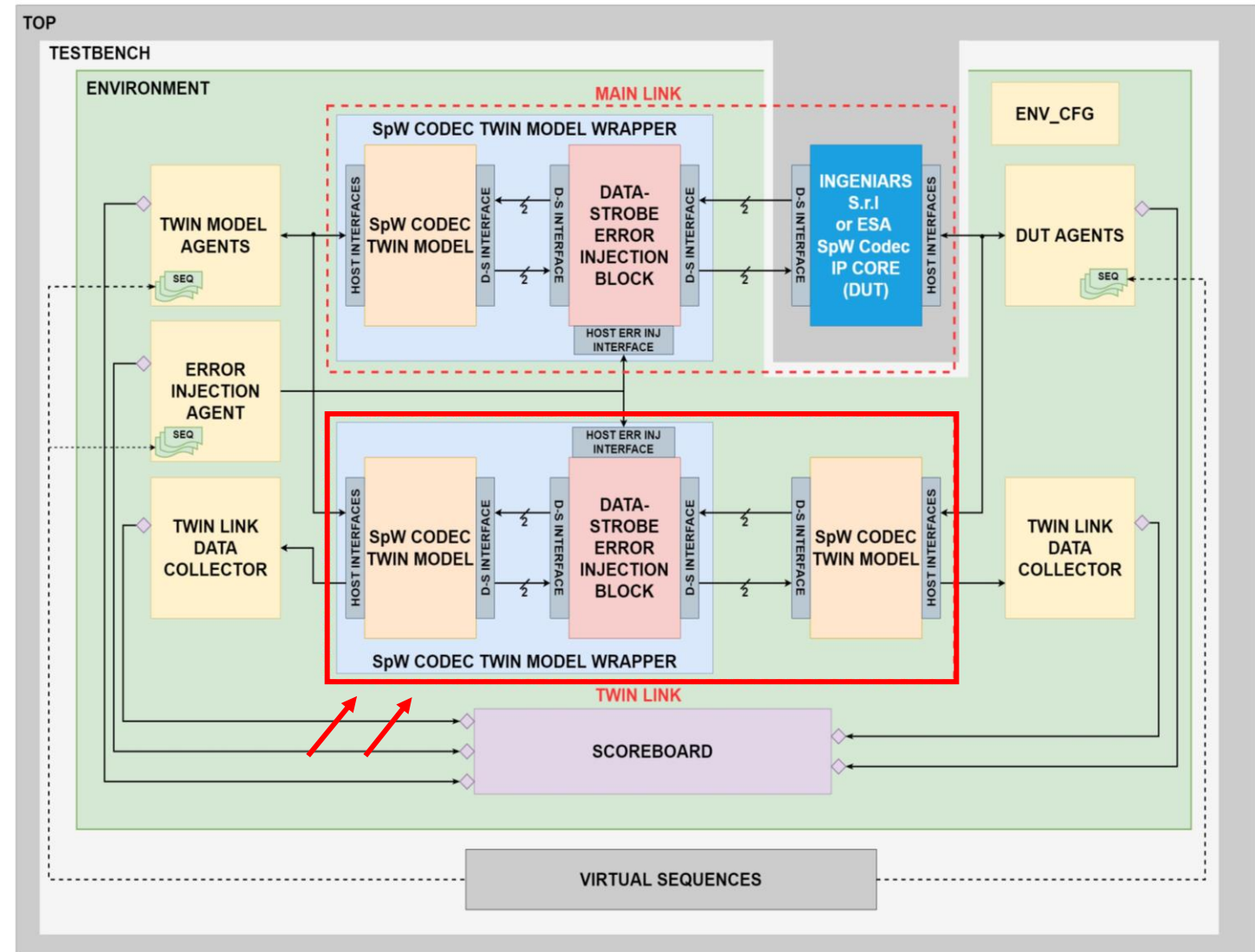
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 - Communication between two Twin Models



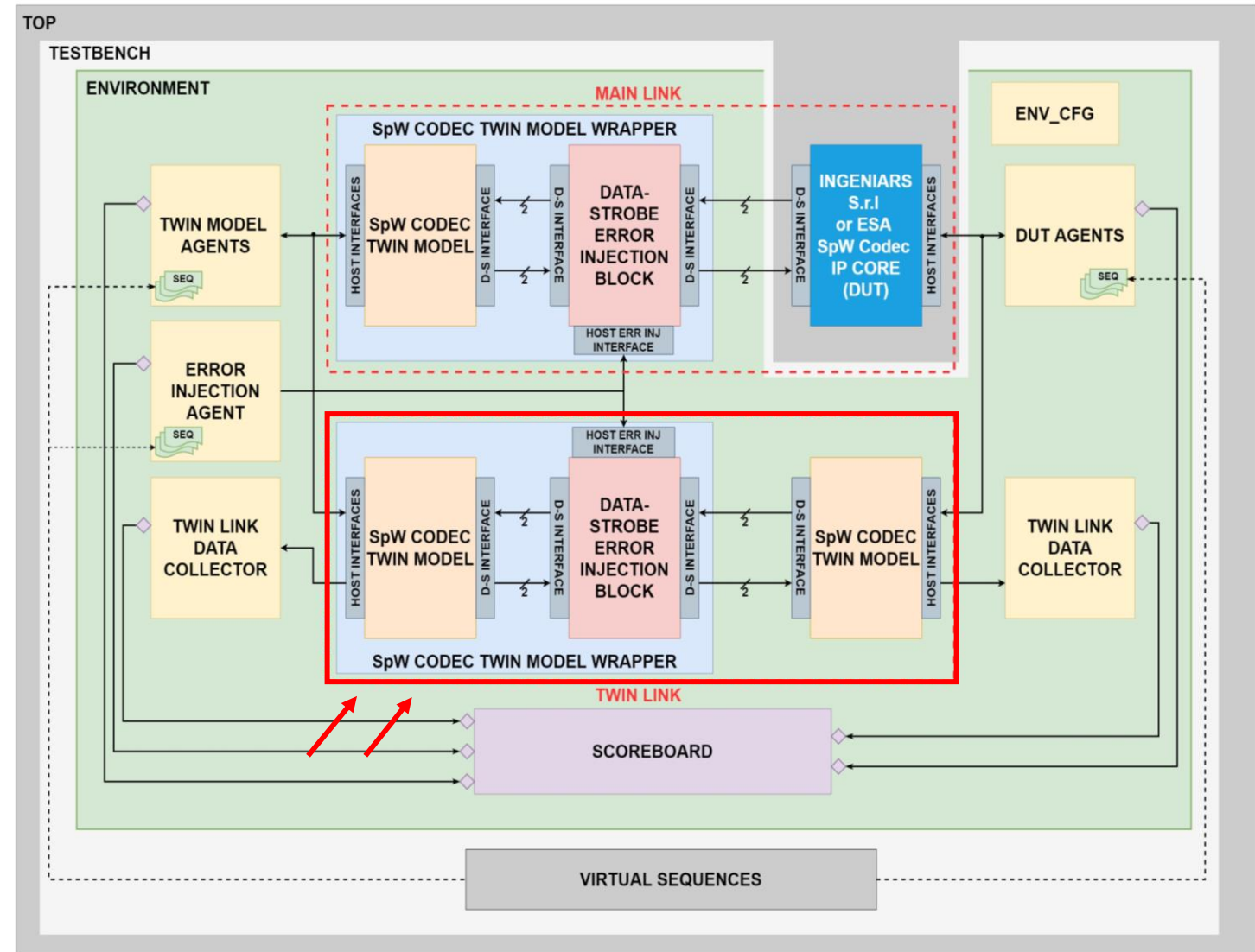
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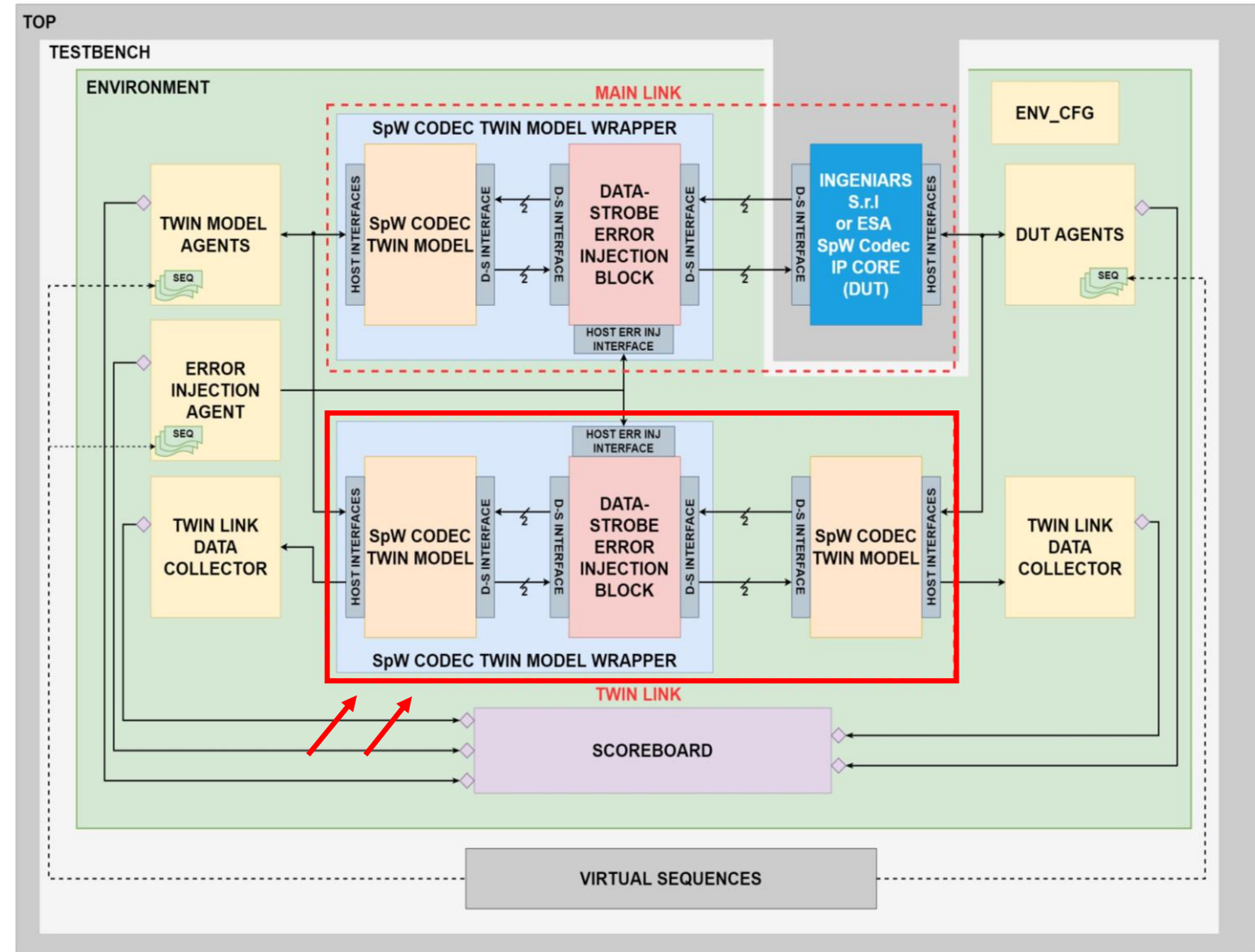
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 - Emulates the ideal behavior of the SpW Link



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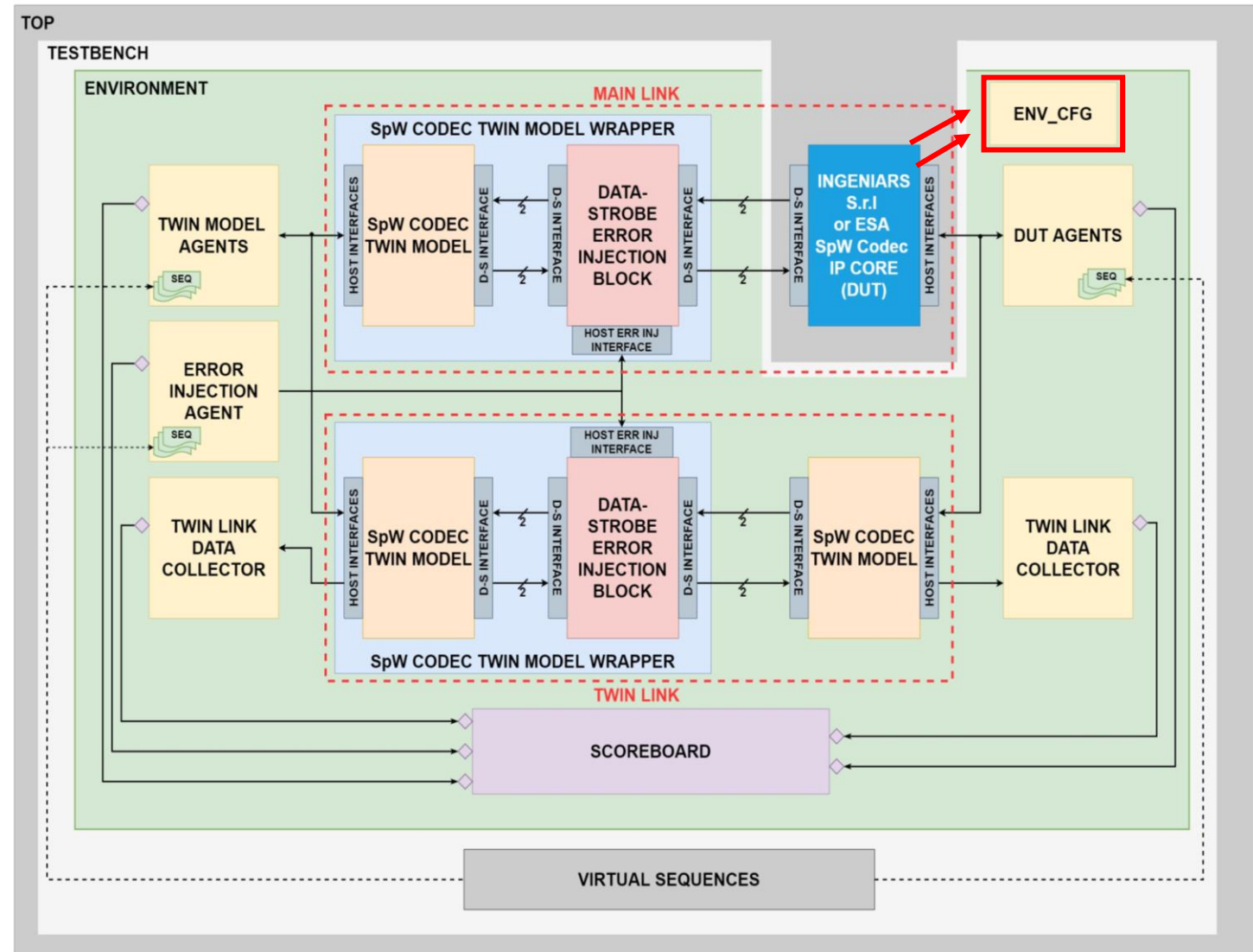
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Support automated verification of all possible simulation scenarios



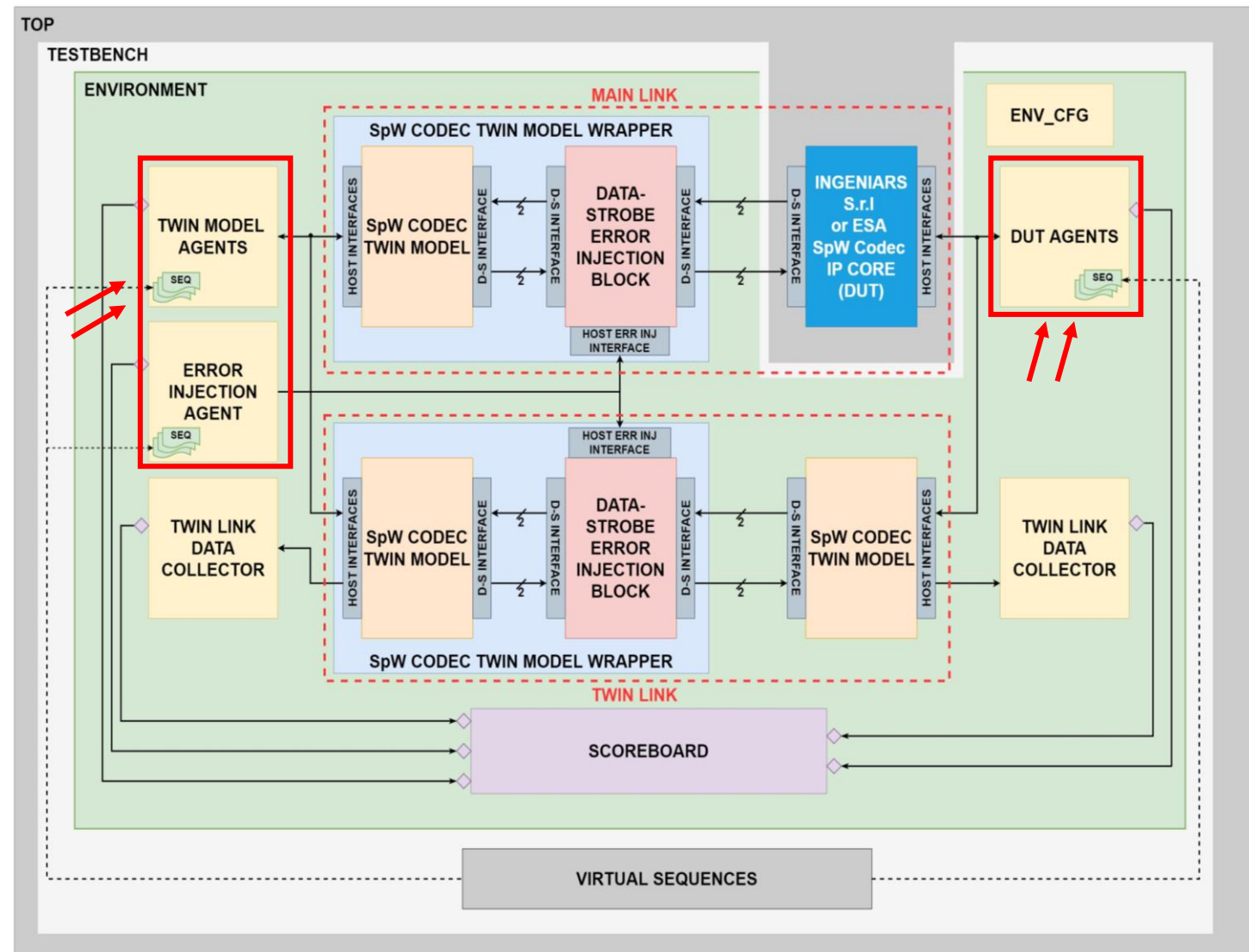
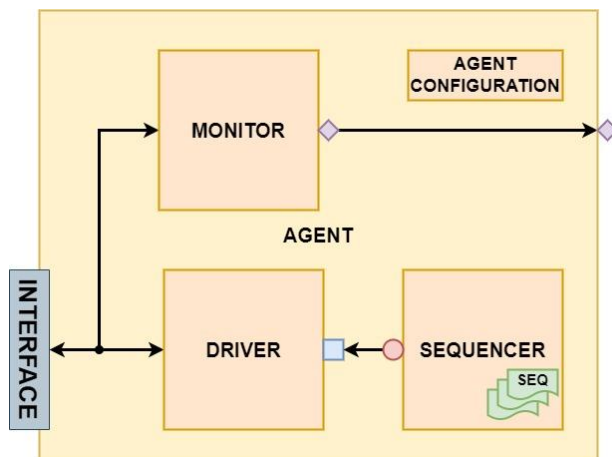
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- Environment Configuration



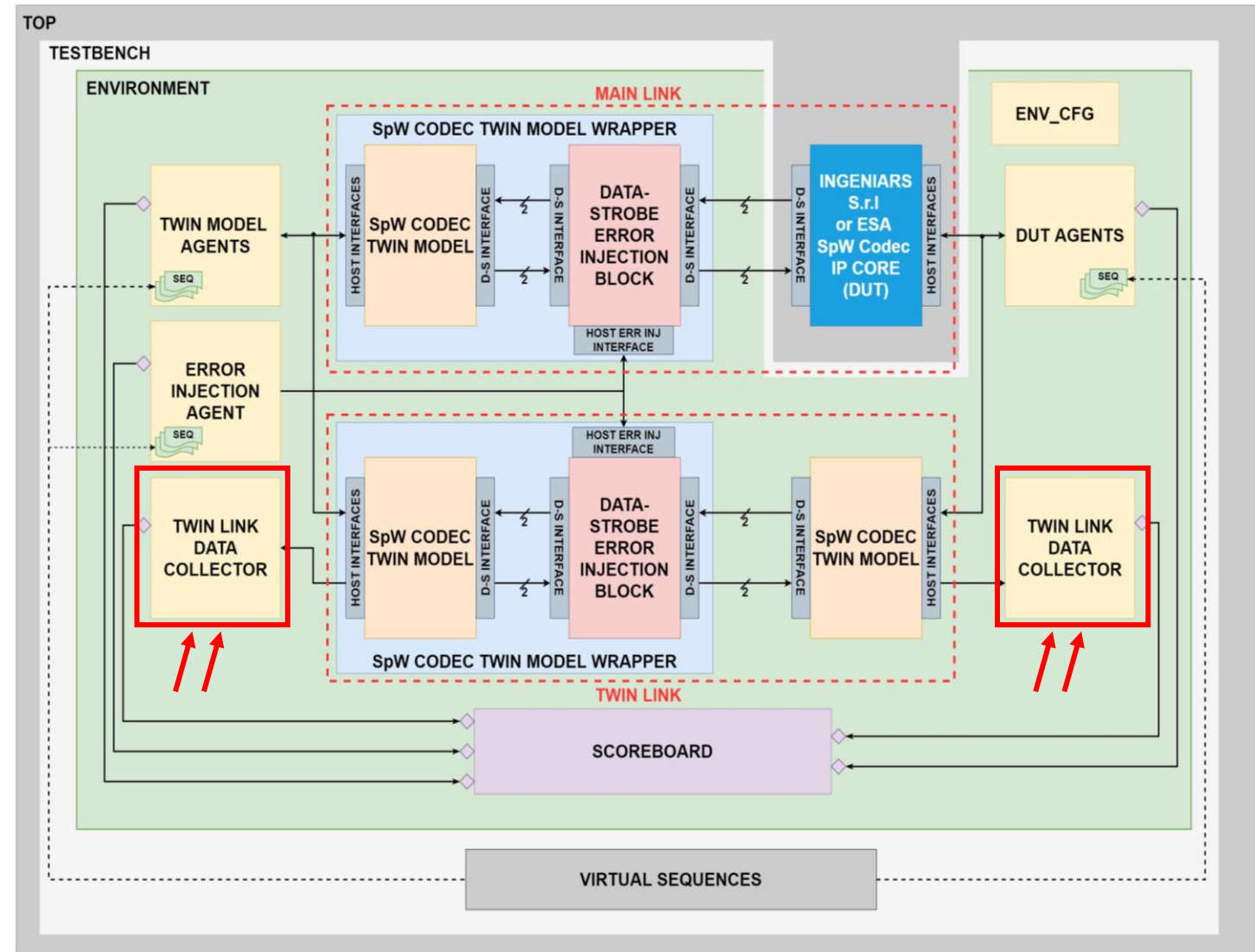
UVM-BASED VERIFICATION ENVIRONMENT ARCHITECTURE

- Environment Configuration
- Agents
 - DUT
 - Twin Model
 - Error Injection



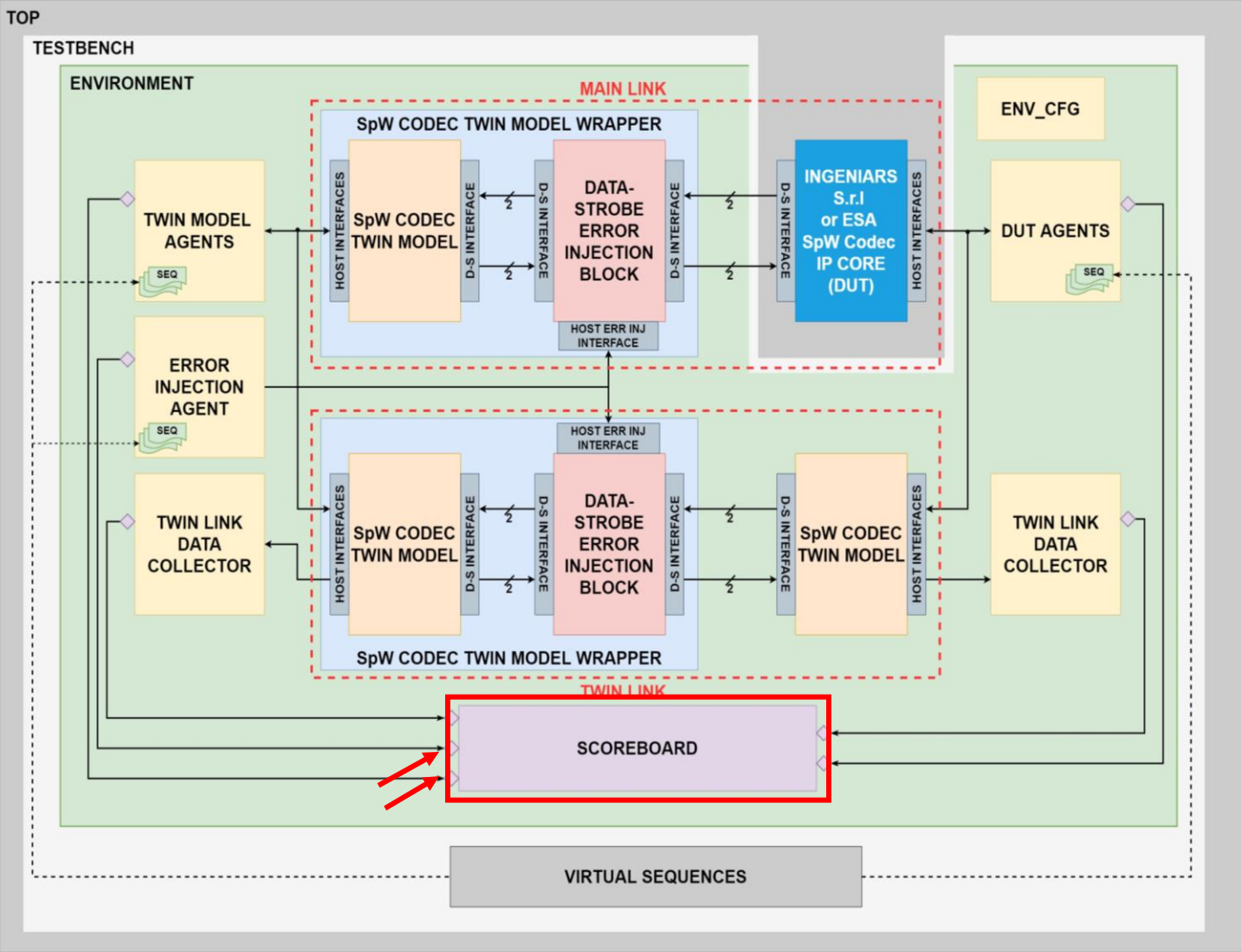
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- Environment Configuration
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 - Error Injection
- Twin Link Data Collectors



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- Scoreboard



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 - Basic VHDL adapter has been developed

VERIFICATION CAMPAIGN

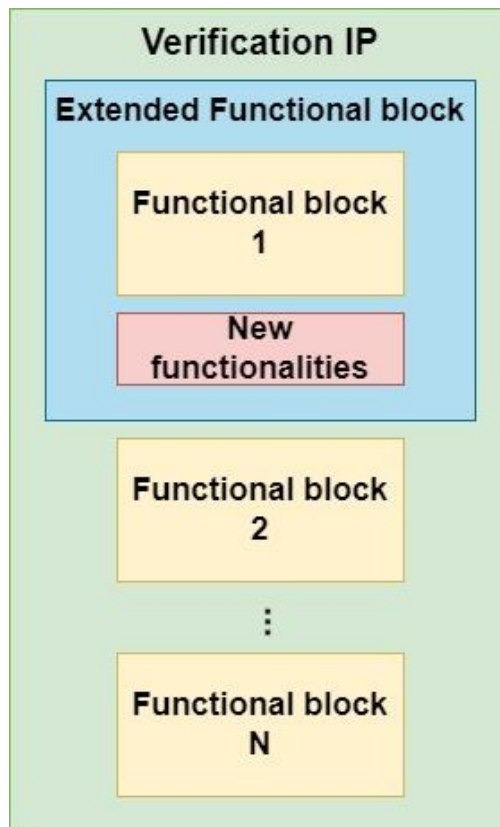
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DUT	Compliance with SpW Standard	Compliance with SpW Standard Rev.1	Code Coverage – Statements	Code Coverage - Branches
IngeniArs S.r.l. SpW Codec IP Core	✓	✓	96.05%	92.08%
ESA SpW Codec IP Core	✓	X	95.24%	91.72%

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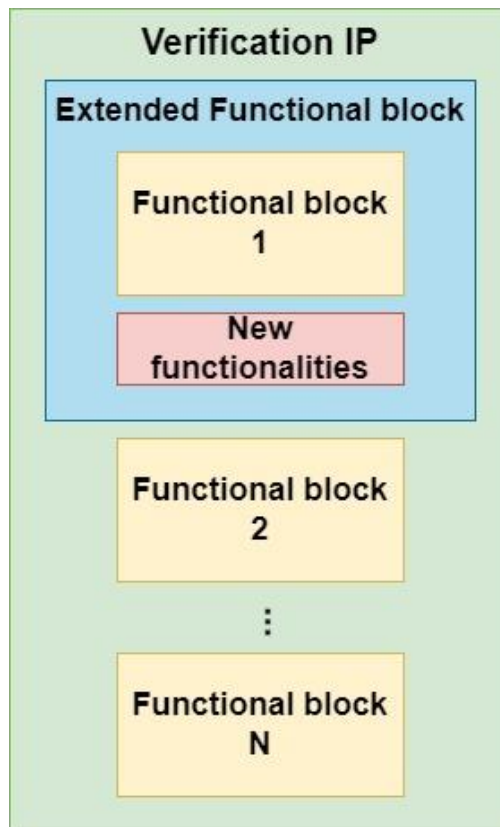
- Maintainability

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 - Add functionalities (extension)

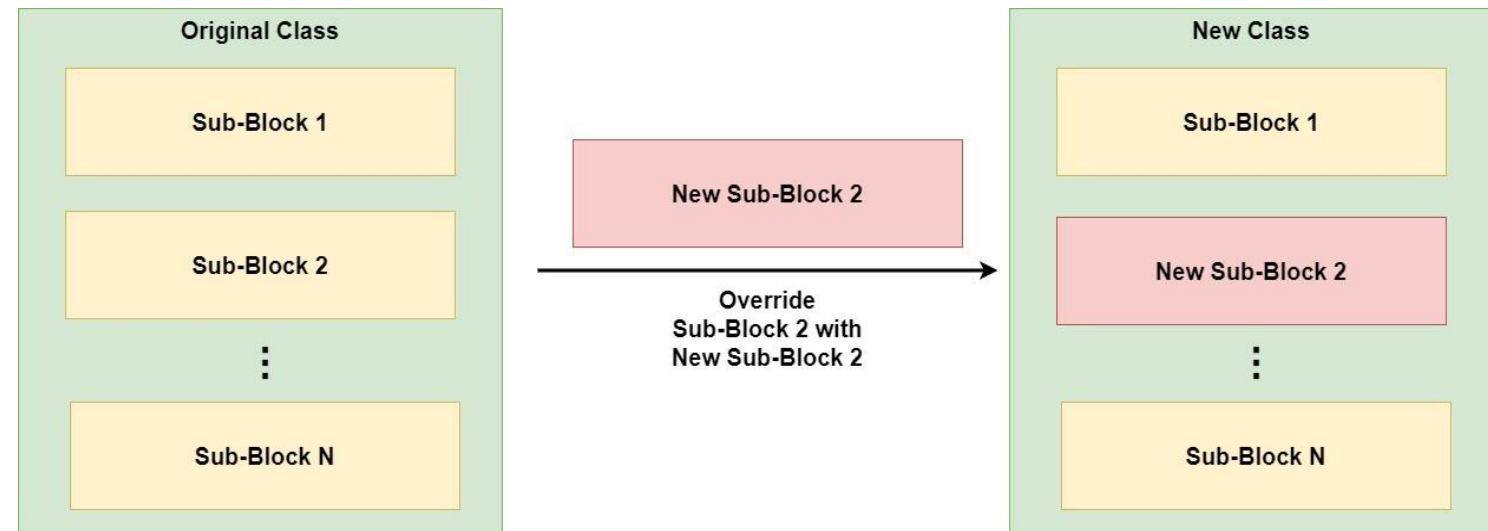


- Maintainability

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- Update functionalities (override)

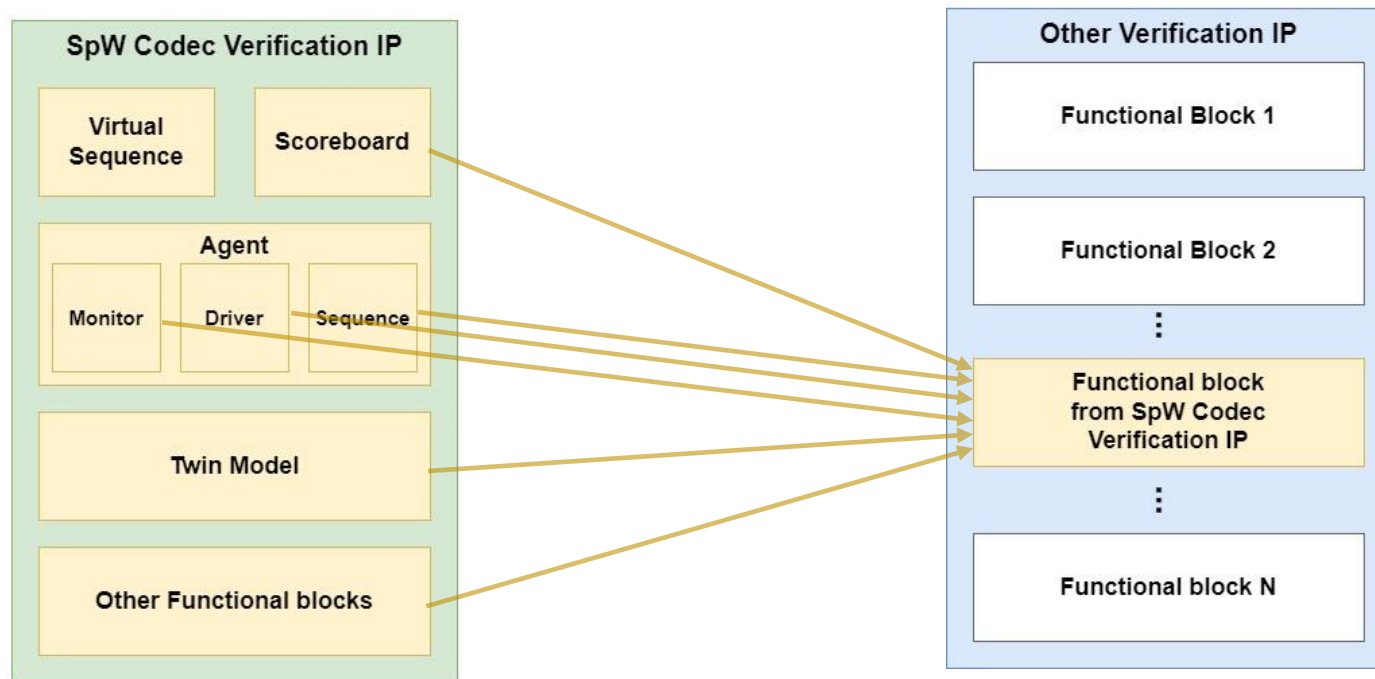


UVM-BASED APPROACH ADVANTAGES

- Maintainability
- Reusability

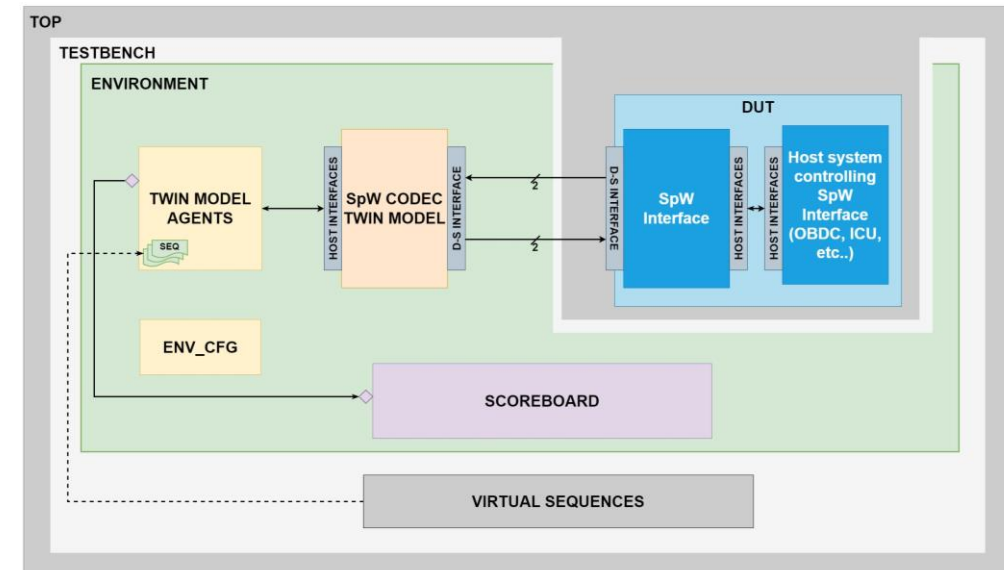
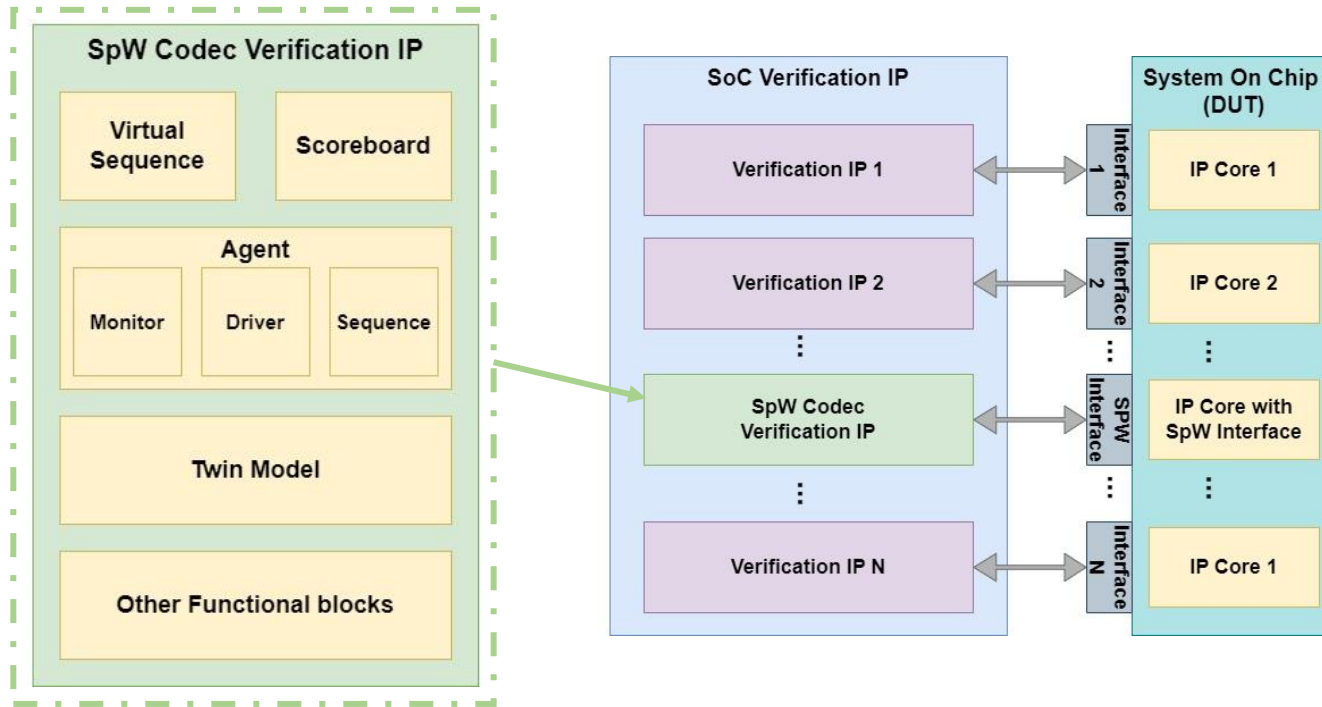
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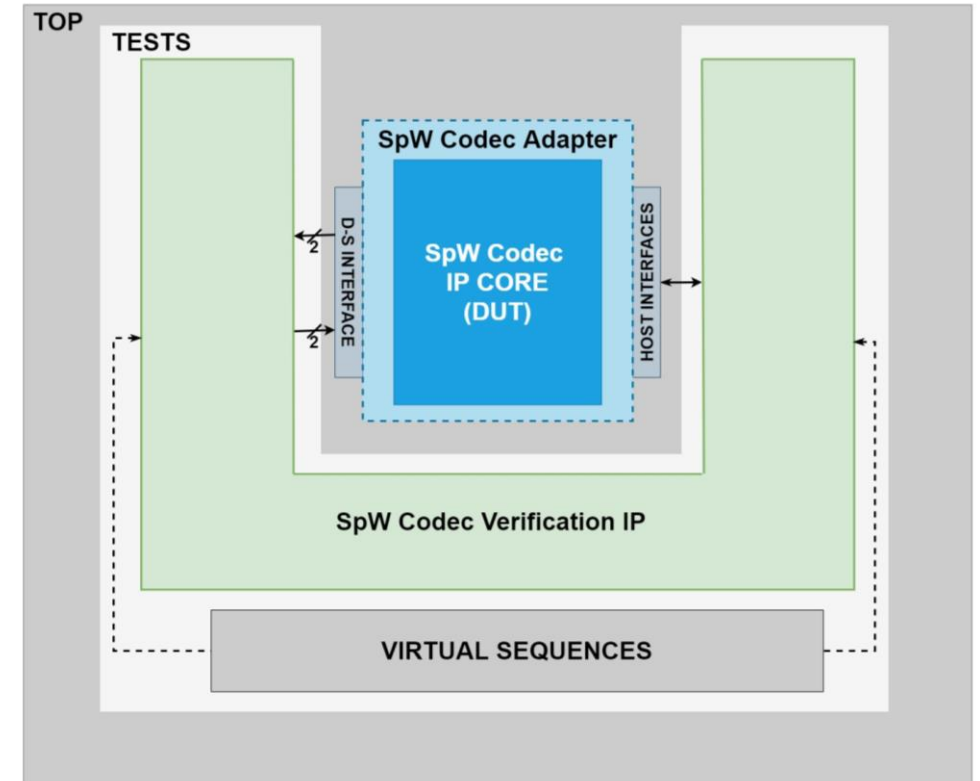
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- Maintainability
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- Separation between Verification IPs developers and users

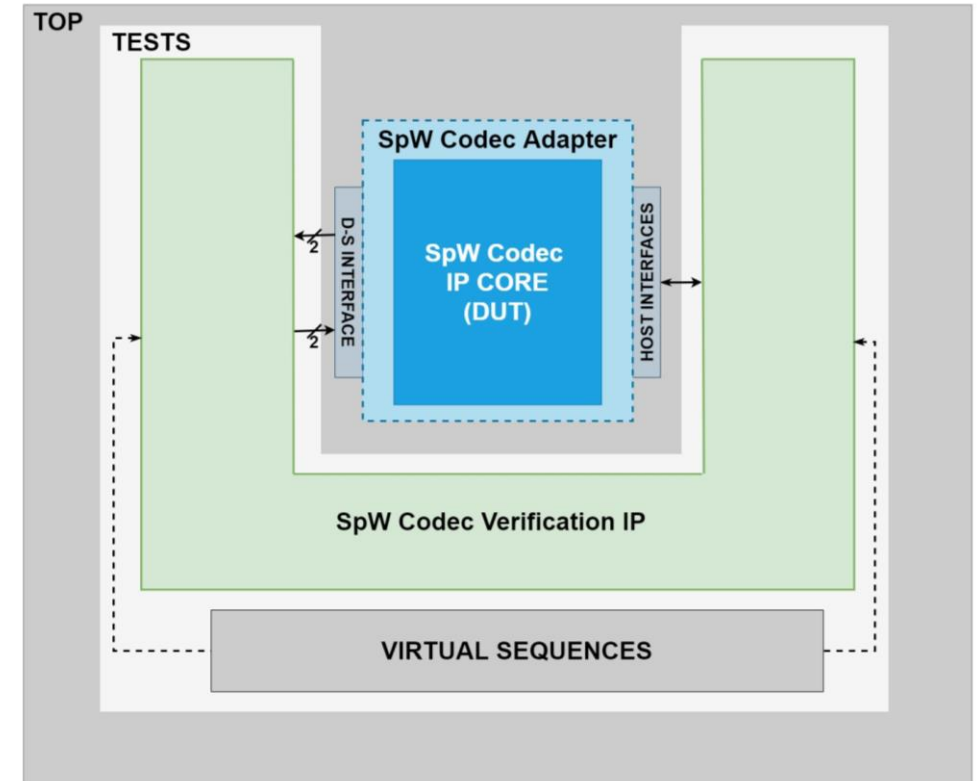
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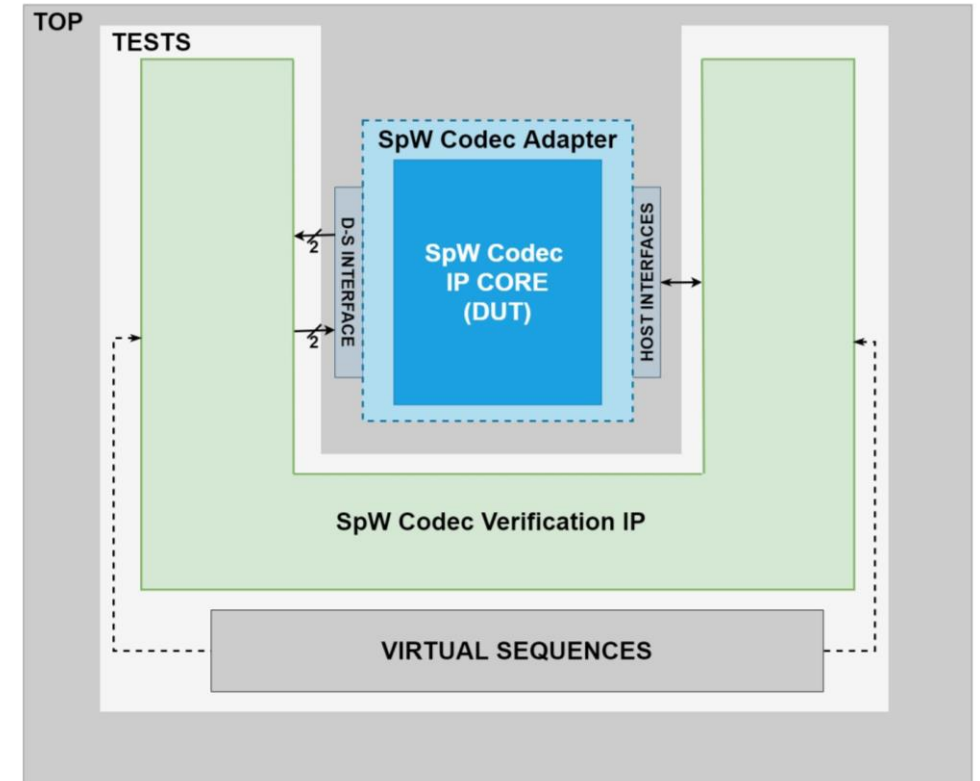
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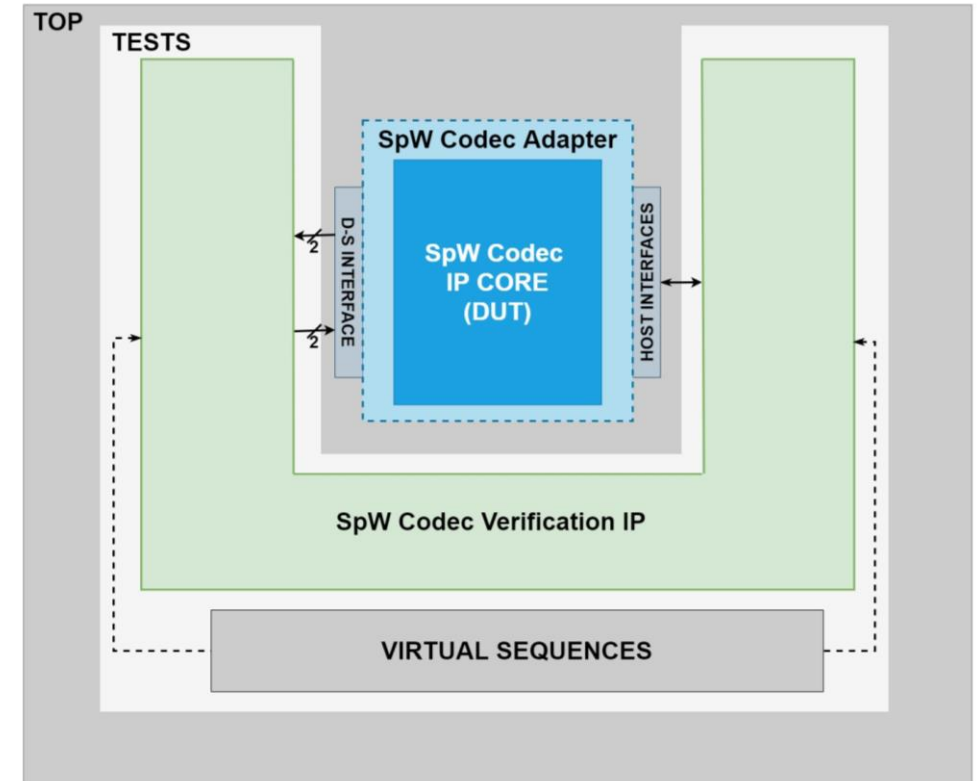
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Significant reduction of verification time and costs
Significant increase of DUTs reliability

Thanks for your attention!

For more information about SpW Codec Verification IP:

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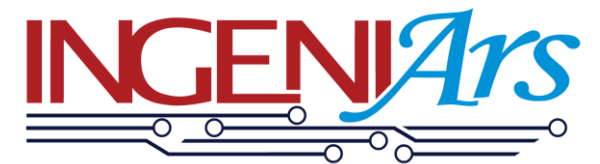
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