

1Gb to 64Gb configuration solutions to boot the last generation of FPGAs

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AGENDA

1. COMBO (COntfiguration Memory Boot Manager)

Up to 64Gb loader / scrubber to boot SRAM based FPGAs

2. MNEMOSYNE (1Gb Configuration Memory)

512Mb – 1Gb RHBD Non-volatile Memory

3. CONCLUSION



1

COMBO

(COnfiguration Memory
Boot Manager)



INTRODUCTION COMBO

Market Needs: Increase Need In Configuration Memory Density

- ◆ Newly released space SRAM FPGAs are requiring larger configuration memories.

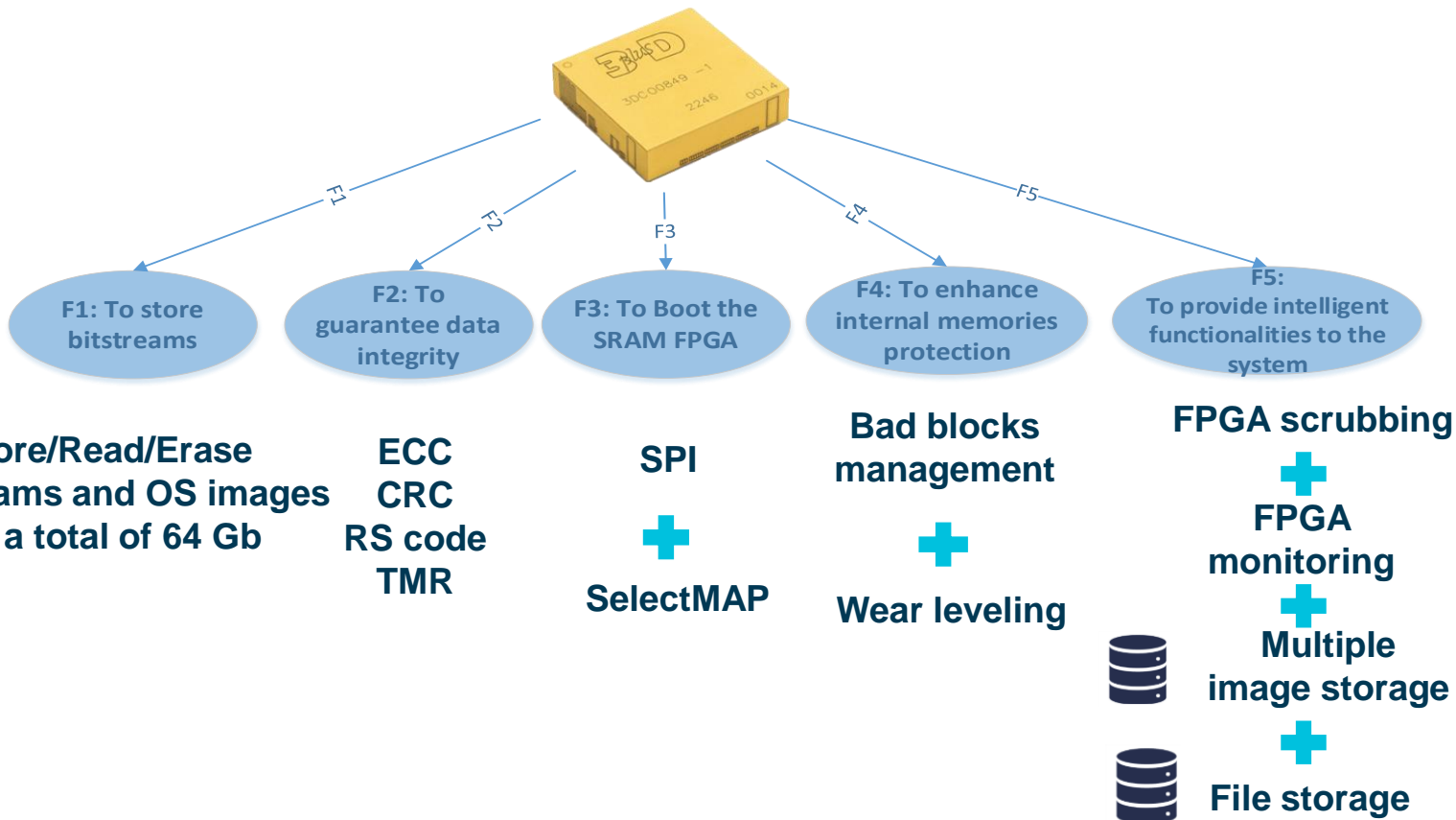
AMD XILINX Space FPGAs	Configuration memory density
Virtex-4QV - XQR4V	64 Mb
Virtex-5QV - XQR5V	64 Mb
RT Kintex Ultrascale - XQRKU060	256 Mb
Zynq Ultrascale+	256 Mb
Versal -XQRV	≥ 1 Gb

- ◆ Nowadays, space applications are requiring :
 - ◆ Multiple bitstream images
 - ◆ In-orbit reconfigurability
 - ◆ Improvement of the overall reliability by scrubbing the memories and FPGAs
- ◆ 3D-PLUS proposes a space grade high density **CO**nfiguration **M**emory **BO**ot manager **COMBO** family to boot and/or scrub SRAM based FPGAs/MPSoC requiring a smart integrated solution.



COMBO FUNCTIONALITIES

What Functionalities Does Combo Family Provide?





COMBO INTERFACES

What Are Combo Interfaces?

On ground, the UART/SPI interface allows to:

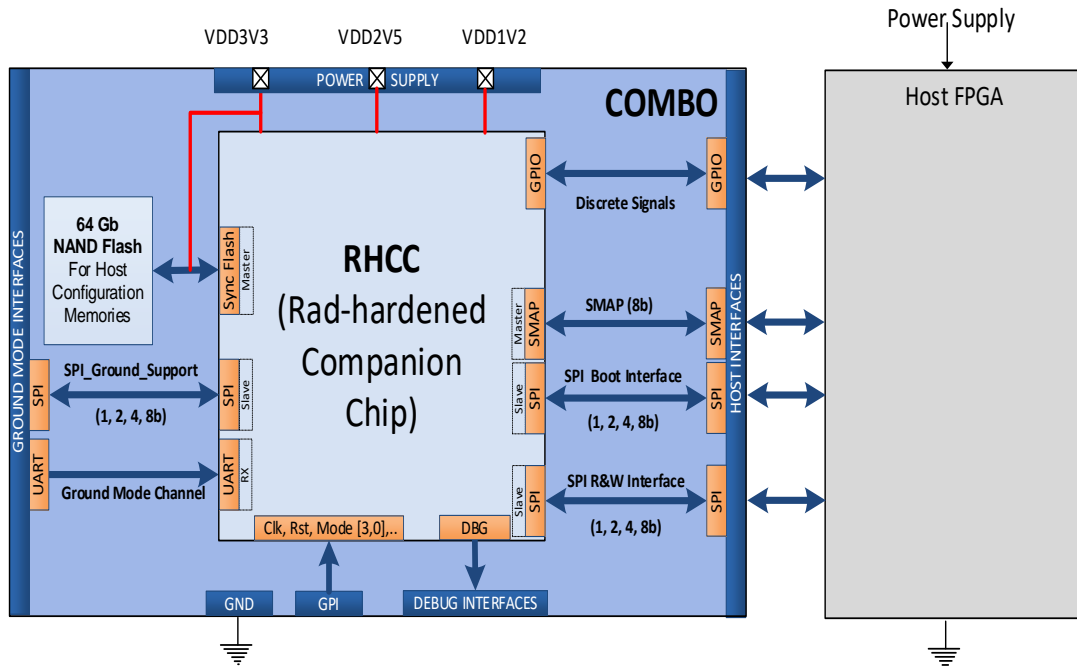
- Read/write/erase files
- Store the Initial file system tables and missions parameters

During the mission, the 2 SPI interfaces can be used to :

- One to boot the SRAM based FPGA
- One to perform read/write files

During the mission, SelectMap interface can be used to :

- Boot the SRAM-based FPGA
- Detect errors on the configuration layer of the FPGA
- Scrubs and monitors the SRAM based FPGA.





COMBO CHARACTERISTICS

Companion For Space Application

Test campaign already performed.

Radiation performances:

- TID > 50 kRad
- SEL LET > 62.5MeV.cm²/mg

Environment Performances:

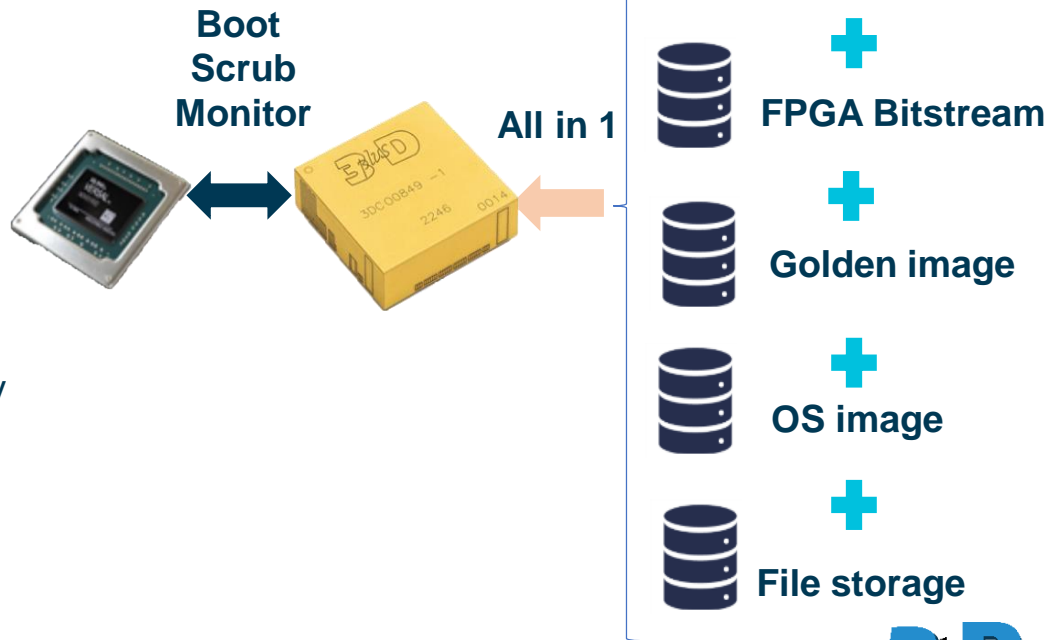
- 40°C to +105°C

Electrical power supply:

- Power Supply: 1.2V, 2.5V, 3.3V

Package

Product footprint : 32x32mm²
 484-ball BGA, pitch: 1,27mm
 Weight: 22g



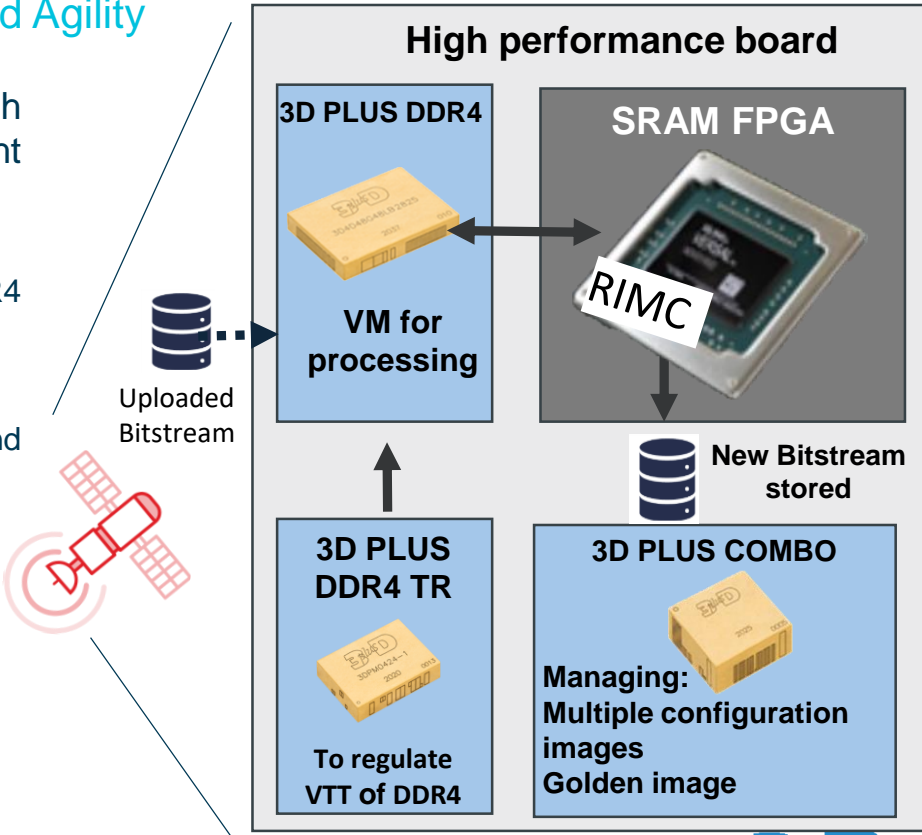


IN-FLIGHT RECONFIGURATION FOR HIGH PERFORMANCE APPLICATIONS

COMBO, A Step-up For More Flexibility And Agility

◆ 3D PLUS offers a complete ecosystem for high performance applications requiring in-flight reconfiguration :

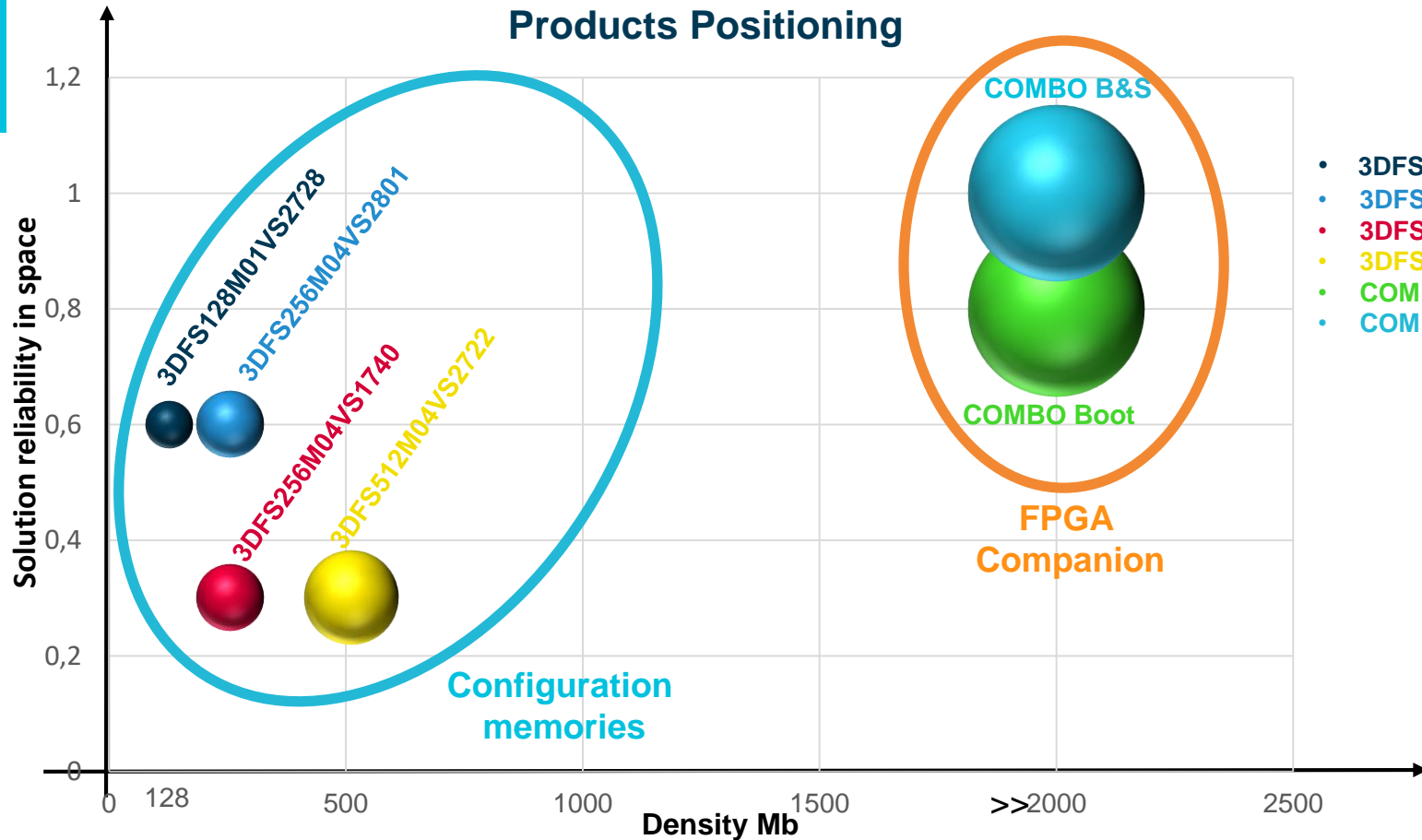
- ◆ **DDR4 memory** to buffer the new bitstream
- ◆ **DDR4 TR** to regulate the VTT of DDR4 memory
- ◆ **RIMC DDR4** to mitigate uploaded bitstream
- ◆ **COMBO** to store multiple FPGA bitstreams and to enable in-flight reconfiguration





3D PLUS HD CONFIGURATION SOLUTIONS POSITIONING

Products Positioning



- 3DFS128M01VS2728
- 3DFS256M04VS2801
- 3DFS256M04VS1740
- 3DFS512M04VS2722
- COMBO Boot
- COMBO Boot&Scrub





MNEMOSYNE

Rad-Hard Non-Volatile Memory





Higher density ROMs required:

- Users applications
- FPGAs/MPSOCs:
 - ZynQ UltraScale + (ZCZU15): ≥ 512 Mb
 - Versal –XQRV : ≥ 1 Gb

Conf. Memory preserves data integrity from start till end of mission

- Data retention
- Non volatile
- SEL immunity
- SEU immunity



MNEMOSYNE INTRODUCTION

The memory goddess



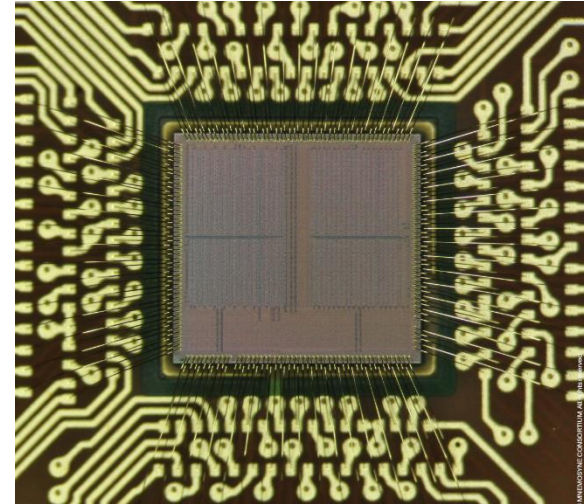
- ❏ **Non volatile memory with SPI interface**
- ❏ **Developped by 3D PLUS**
 - ❏ Within the frame of an European project –H2020
- ❏ STT-MRAM technology provides SEU immunity to memory cells
- ❏ Fully Depleted SOI 22nm process brings SEL immunity

- ❏ **Applications:**
 - ❏ FPGA configuration bitstream storage
 - ❏ Boot code storage for microcontrollers and microprocessors



- Rad hard design techniques on control logic and interfaces

- Redundancy, restricted cell sets on SEU critical parts.
- SET immune on clock and reset trees
- Glitch filters on strategic nodes
- Derating takes into account device aging and TID.
- Leakage reduction (body bias, process)



Test vehicle ASIC



KEY FEATURES

- 512 Mb, 1 Gb density
- Up to 100 MHz
- 1.8 V SPI interface (3.3 V optional)
- SPI, QSPI, OSPI supported
- Embedded ECC
 - ECC flag
 - Error counter
- 100 k P/E cycles
- 20 years data retention
- [-55 °C; +125 °C]: op. temp

RADIATION DATA

- TID > 100 krad(Si)
- SEL > 60 MeV.cm²/mg
- SEU > 60 MeV.cm²/mg
- SET > 60 MeV.cm²/mg
- SEFI > 60 MeV.cm²/mg

Note: The SEE LET threshold would be tested in other facilities with 80 MeV.cm²/mg target

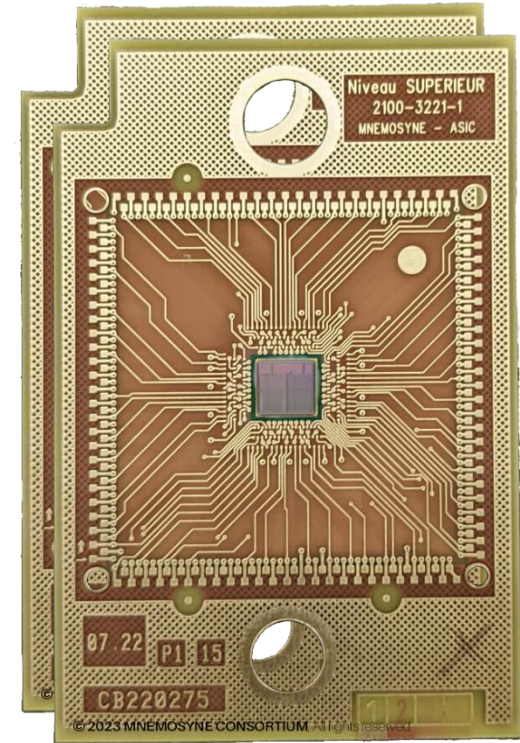


FIRST DESIGN RESULTS

Results summary



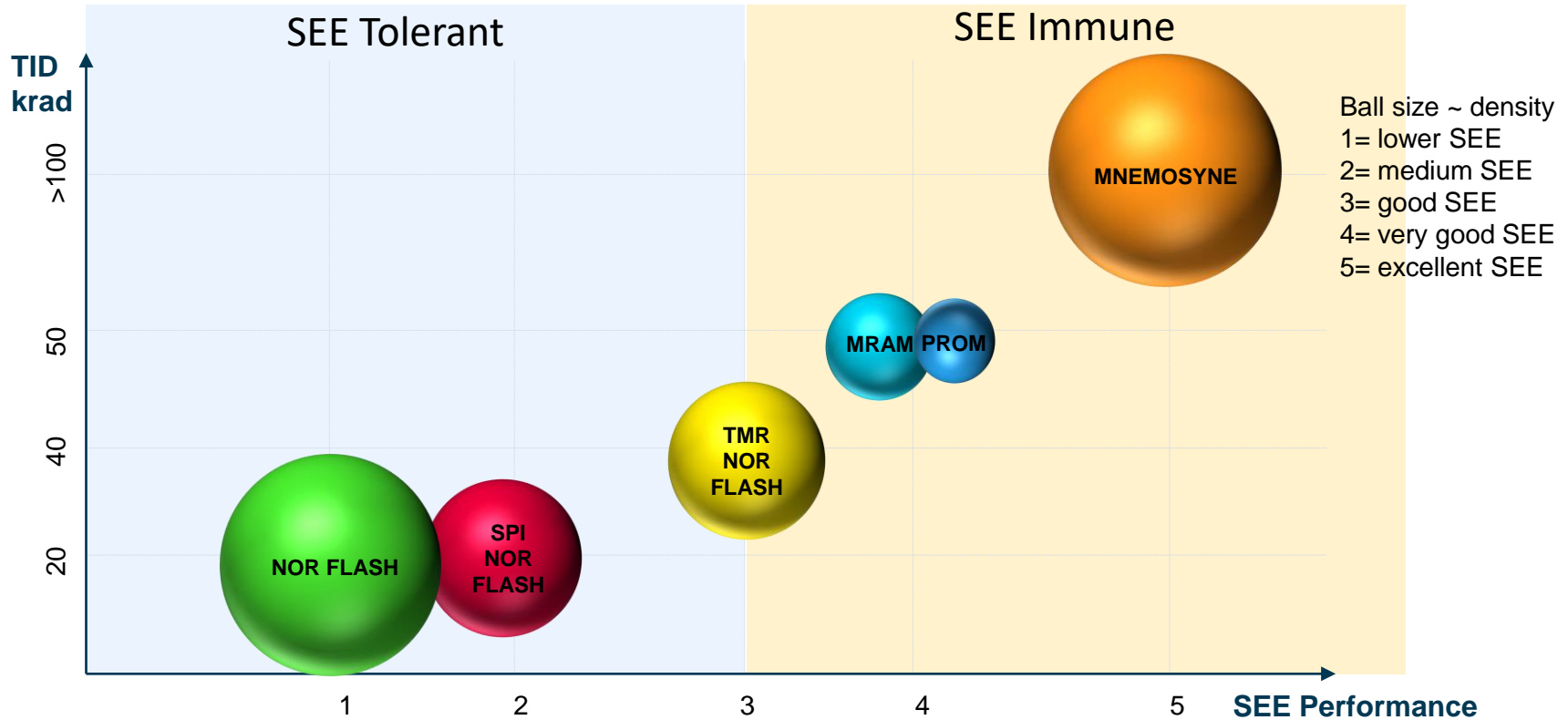
- ❏ TID > 100 krad(Si)
- ❏ SEL/SEU LET_h > 60 MeV.cm²/mg
- ❏ 1000h Life test passed with 3 θ measurements
- ❏ QSPI/SPI interface validated





3D PLUS CONFIGURATION MEMORIES

Portfolio





CONCLUSION

3D PLUS Available Solutions for the last Generation of FPGAs

3D PLUS offers 2 Space grade solutions to boot high-end SRAM based FPGAs

1. COMBO

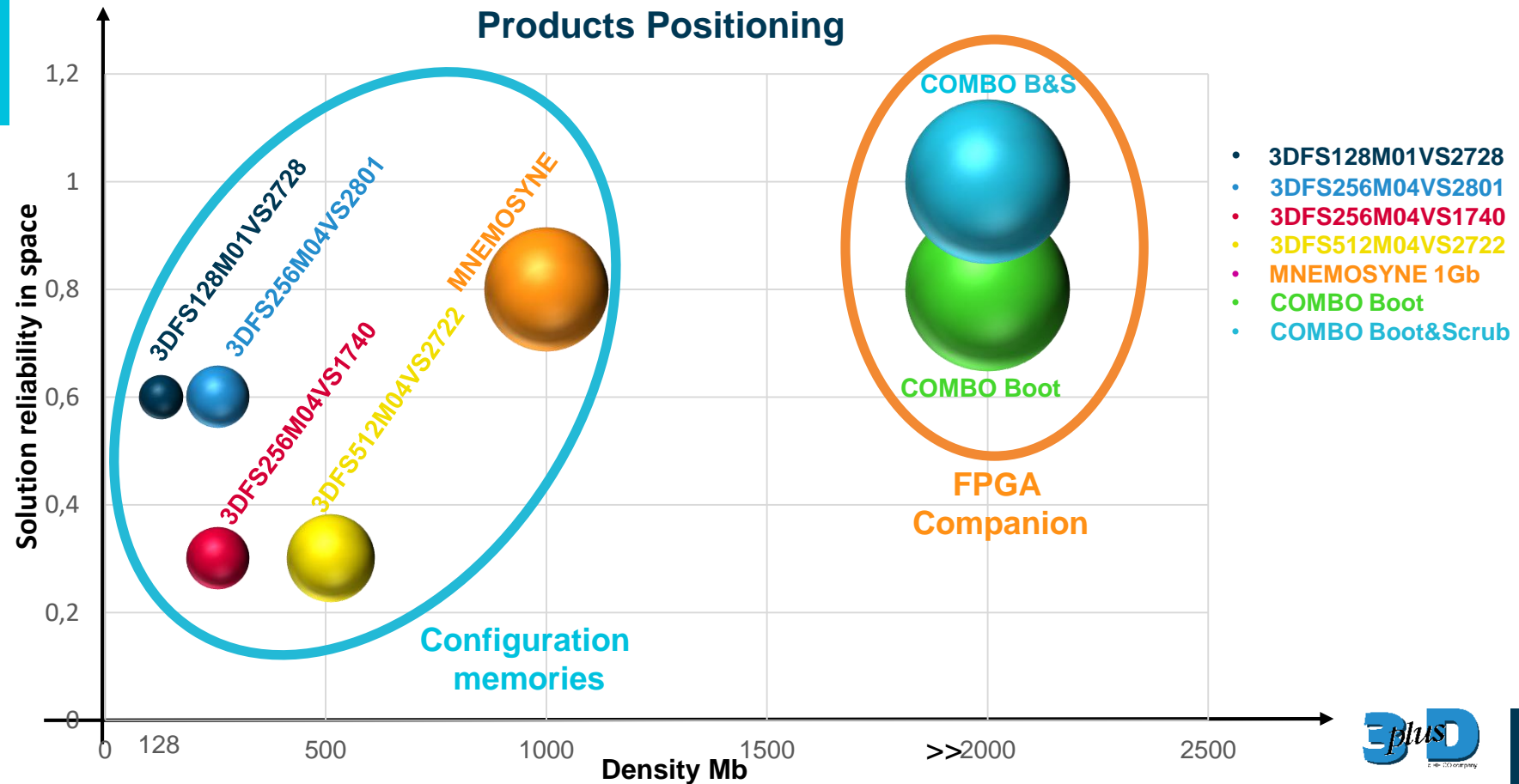
- ◆ **First delivery : October 2023**
- ◆ Full space grade solution to boot different high end SRAM based FPGAs
- ◆ System reliability increased thanks to implemented mechanisms
- ◆ Multiple reliable bitstream images with data integrity
- ◆ Key solution for on-orbit reconfiguration
- ◆ Storage of data during the mission
- ◆ Time and money savings

2. MNEMOSYNE

- ◆ **First delivery : September 2023**
- ◆ Space grade high density configuration memory
- ◆ Best in class regarding reliability (data retention, P/E cycles, radiation)
- ◆ Ease customers life with additional features for error management strategy (ECC_flags, errors counters)
- ◆ Scalability (512 Mbit & 1 Gbit are pin to pin compatible)



3D PLUS HD CONFIGURATION SOLUTIONS POSITIONING



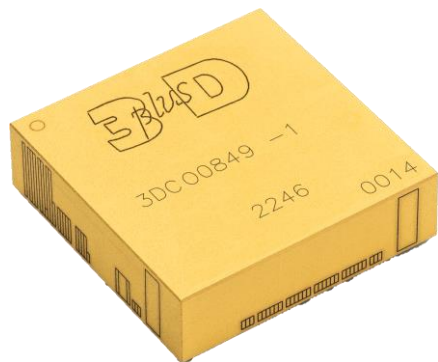


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High density radiation hardened NVM (MNEMOSYNE)



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- ◆ Mnemosyne, together with EFESOS which is another H2020 project led by IMEC focused on RH DARE22 platform (GA 821883), is also developing the 22nm FDSOI RH design



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