SYDERAL POLSKA

ELECTRONICS & SOFTWARE

SpaceFibre and image compression on RTG4 FPGA

Dawid Linowski (presenter), Andrzej A. Wojciechowski, Tomasz Rybak

SEFUW 2023
15th March 2023

Outline

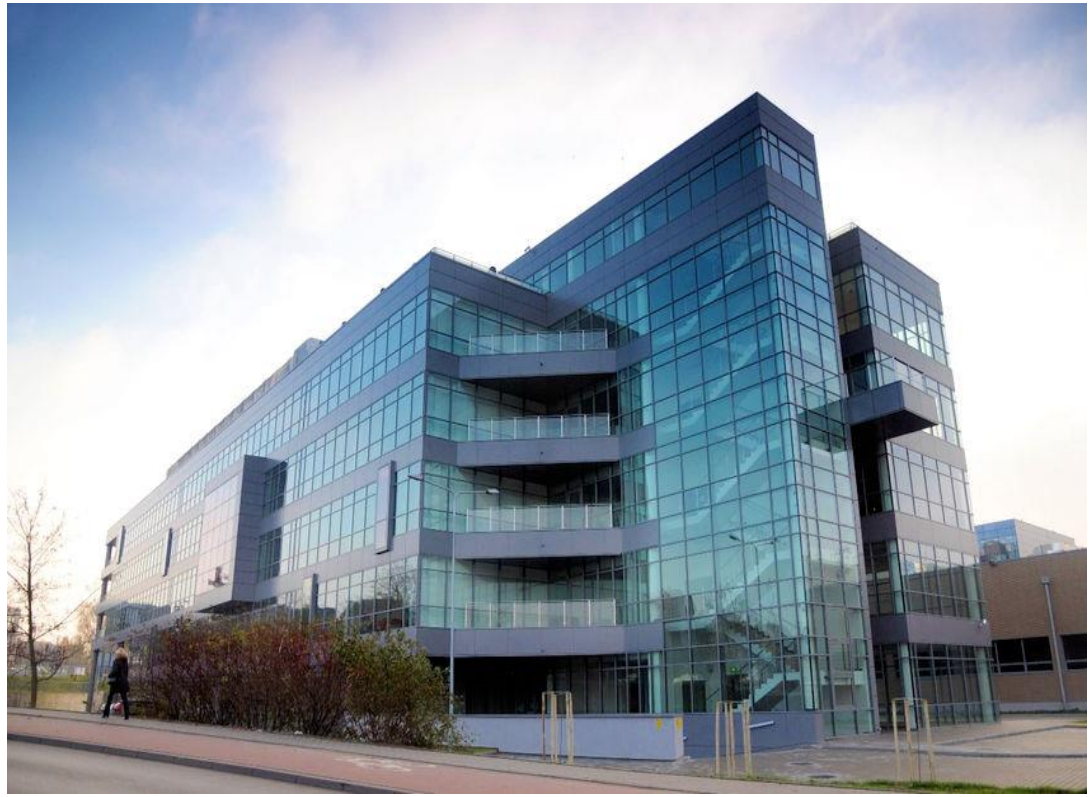
- **Introduction and objectives**
- Requirements
- Design description
- Design verification in simulation
- Design validation in hardware
- Summary

SYDERAL Polska

Established in:
2016

Number of employees:
28

Headquarters:
Gdańsk, Poland



Gdańsk Science and Technology Park - headquarters

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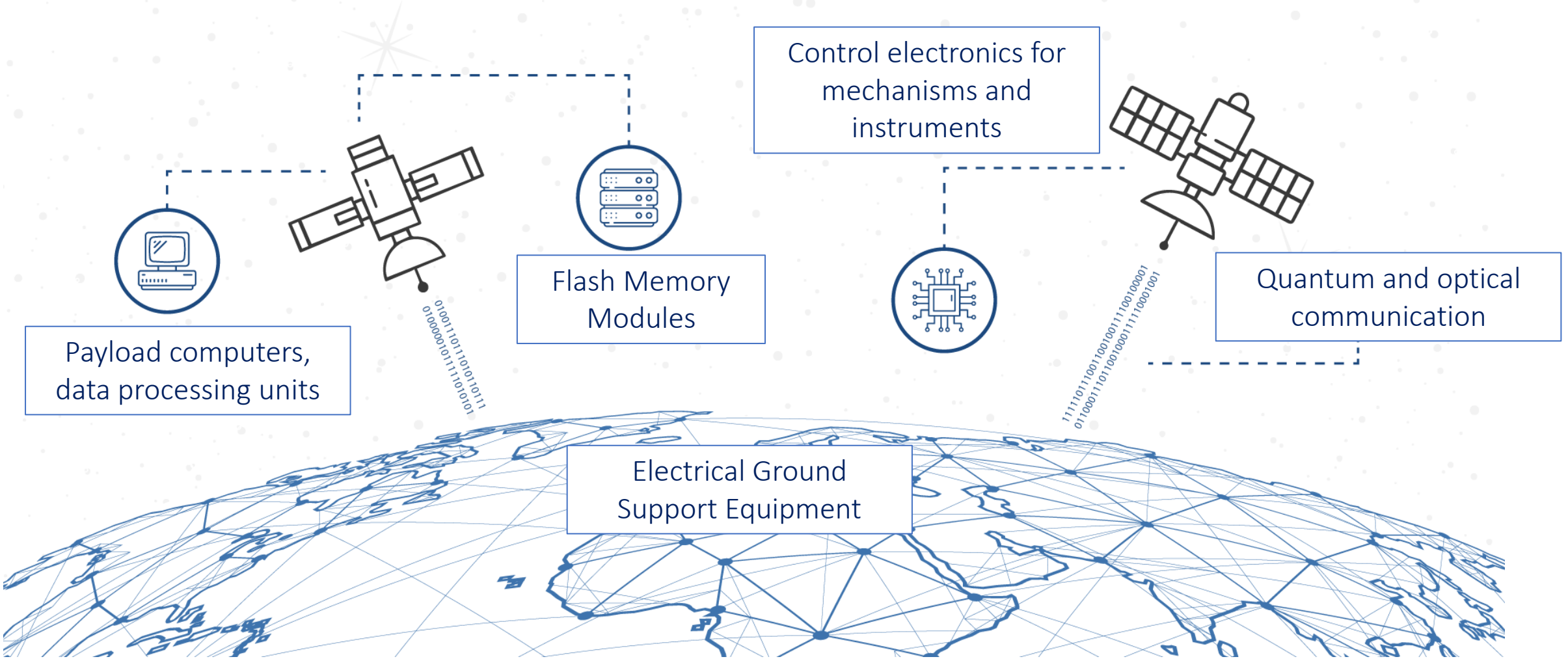
Areas of expertise



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Project’s objectives

Developed in the scope of the Polish Industry Incentive Scheme (PLIIS) as „Demonstration of SpaceFibre Technology Usage for Image Processing Applications” (SFIC).

Goals:

- Demonstration of parallel operation of CCSDS-121 and CCSDS-123 compatible multispectral image compression IP cores on a high-performance FPGA evaluation board.
- Demonstration of combined CCSDS-123 and CCSDS 121 IP cores (SHyLoC IP core), thus serving as a baseline for future developments in this technological area.
- Show the SpaceFibre interface as a high-throughput data transfer interface used to transmit hyperspectral images to the compression cores to realise on-the-fly image compression.

Project's origin

- Continuation of work presented by the team from ULPGC on previous SEFUW in 2018.
- Usage of CCSDS-123 and CCSDS-121 IP cores designed by the team from the same University.

UNIVERSIDAD DE LAS PALMAS DE GRAN CANARIA
Instituto Universitario de Microelectrónica Aplicada

IUMA

Review and comparison of design methodologies and hardware implementations on FPGA technologies.
Case study: CCSDS compression algorithms for multispectral and hyperspectral images

Yúbal Barrios, Antonio Sánchez
Lucana Santos, Sebastián López, Roberto Sarmiento
10th April 2018

SHyLoC IP Core

12/03/2018 4475 VIEWS 13 LIKES

ESA / Enabling & Support / Space Engineering & Technology / Microelectronics

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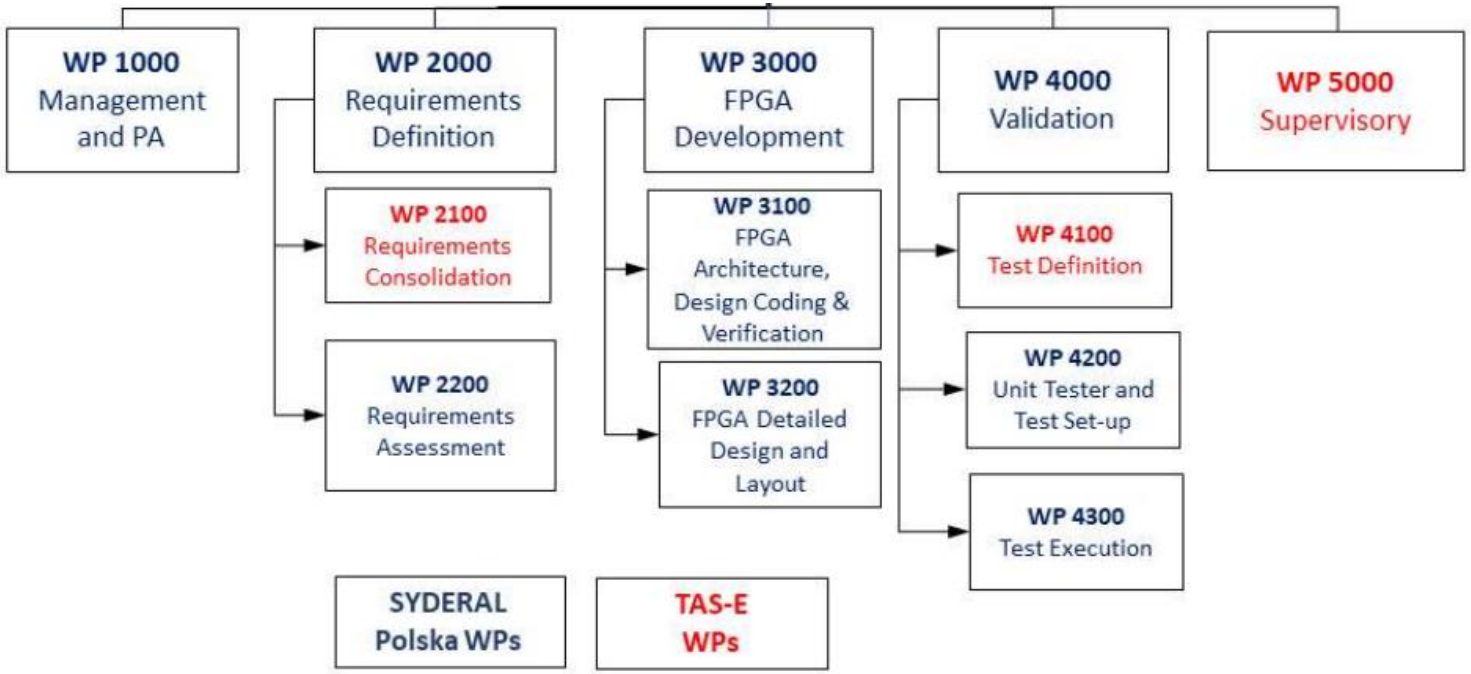
Workplan

Project duration :
17.07.2019 - 11.05.2021

Consortium consistsed of:

Syderal Polska, Poland – main contractor

Thales Alenia Space – España, Spain - subcontractor



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Requirements overview

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- The requirements for this project have been prepared by TAS-E engineering team, having large experience in on-board data processing projects, as well as image compression.
- The set of requirements was also in line with the ones that ESA is requiring for future architectures in their ITTs.

Requirements - interfaces

- Receive hyperspectral images to be compressed through **SpaceFibre interface (2.5 Gbps).**
- Send back compressed image through **SpaceFibre interface**.
- Images in Band Interleaved by Pixel format (BIP).
- Use different SpaceFibre virtual channels for both compression cores (VC1 and VC2).
- Allow configuration of compression IP cores through **SpaceWire RMAP (100 Mbps) or SpaceFibre VC0 interface (with RMAP protocol)**.
- Allow debugging through UART interface.

Requirements - compression cores

- Compress the images with one of two compression cores:
  - Compression Core 1
    Configured to perform the function of both CCSDS-123 (preprocessor) and CCSDS-121 (block adaptive encoding) – creating SHyLoC. Runtime configurable. Initial configuration for AVIRIS dataset.
  - Compression Core 2
    Configured to perform the function of CCSDS-123 (pre-processor + sample-adaptive encoding). Pre-configured for LANDSAT dataset.
- Allow simultaneous online compression using both compression cores.

Requirements - compression modes

Online mode (on-the-fly)

Image data received through the SpFi interface, **compressed data is send back on the same SpFi virtual channel**.

Offline mode

Image for compression is stored in **external DDR memory** first. On request, this image is being transfered to the selected compression core and the resulting compresed image is **stored back in the DDR memory**. It can be later retrieved with SpW or SpFi VC0 (RMAP).

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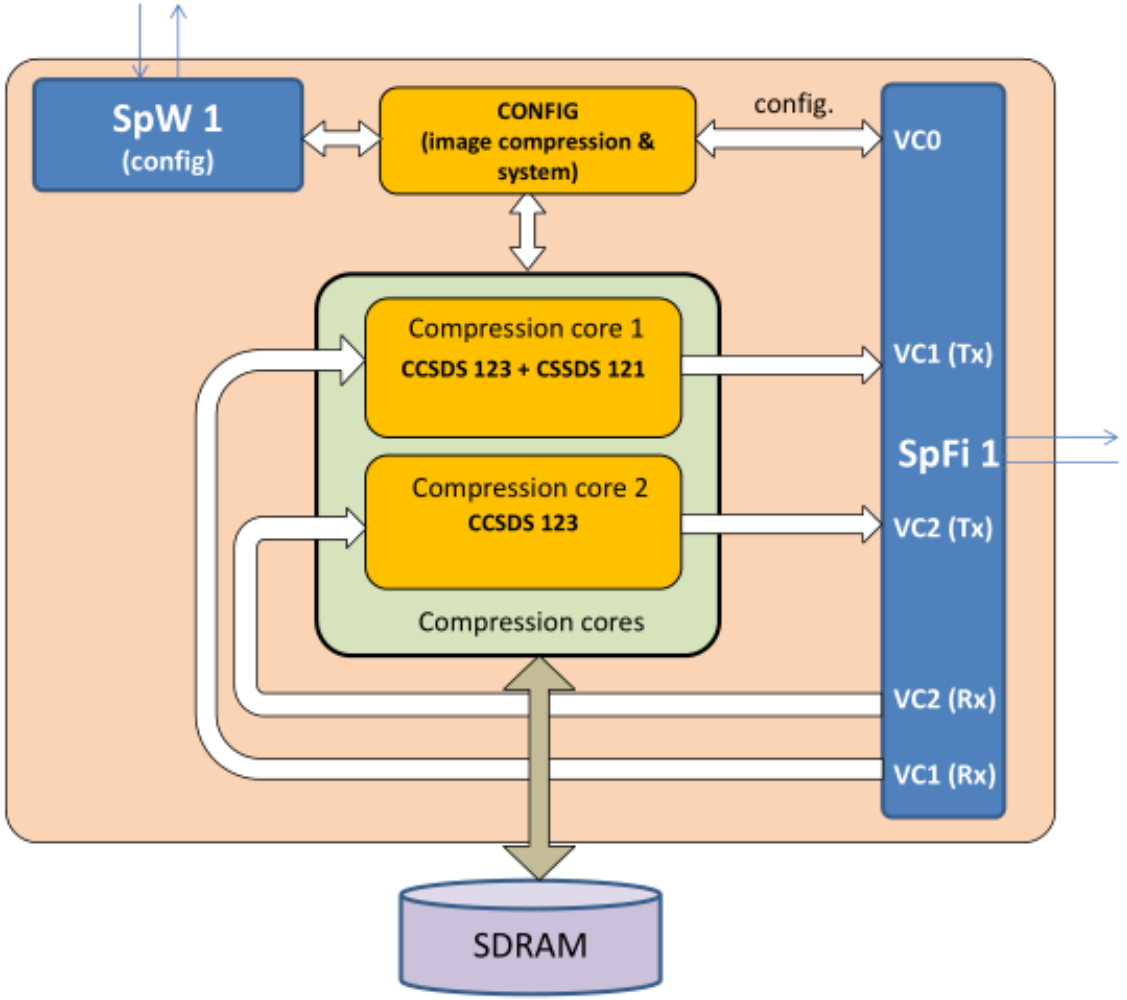
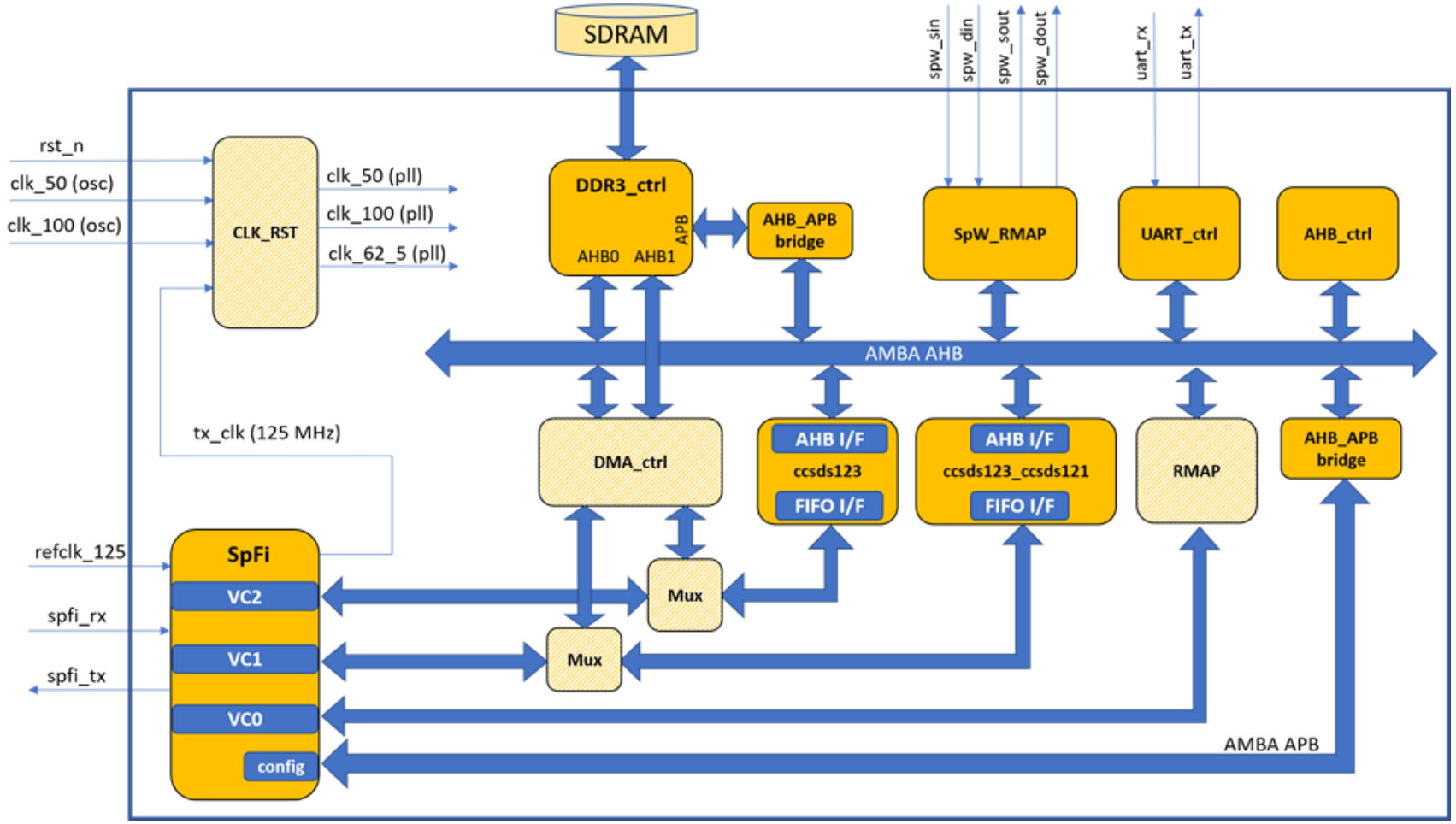
General architecture



FPGA architecture



FPGA modules development/reuse

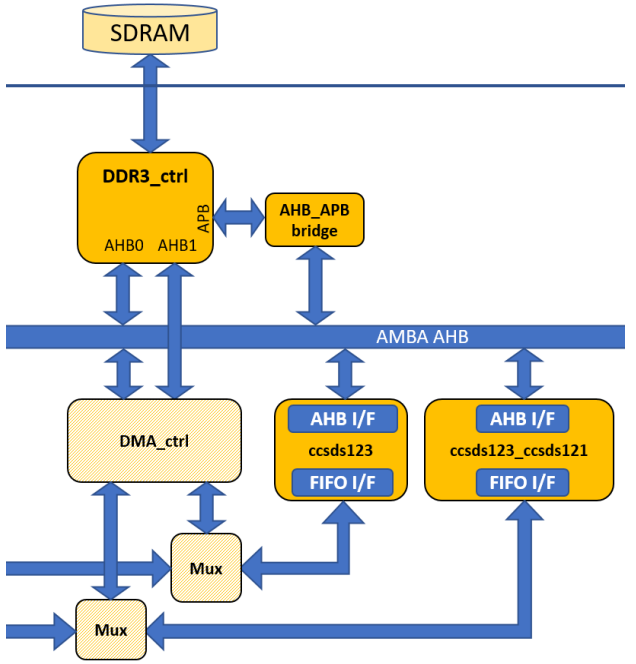
Module	Generated with Microsemi Libero SoC	External IP core	Fully developed in-house
CLK_RST	X		
DDR3_ctrl	X		
UART_ctrl	X		
AHB_ctrl	X		
AHB_APB bridge	X		
SpFi		X	
SpW RMAP		X	
ccsds123		X	
ccsds123_ccsds121		X	
RMAP			X
DMA_ctrl			X

DMA_ctrl

DMA controller manages offline compression.

Responsible for:

- Reading image data from SDRAM and providing this data to the appropriate compression core.
- Reading compression output from the compression core and saving this data in SDRAM for future readout.



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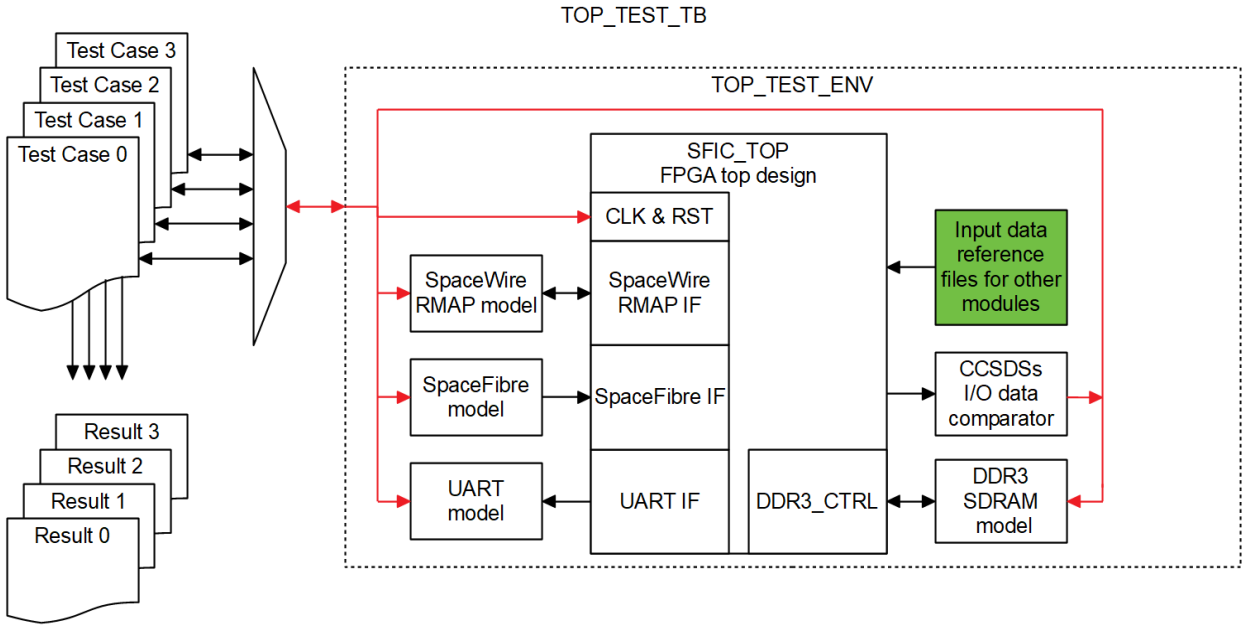
Verification environment



Verification environment:

- Top of representative FPGA used for hardware validation.
- Environment composed by FPGA interface models as well as both CCSDS blocks input/output data comparator with written/read data via SpaceWire/SpaceFibre IF.
- All Test Cases, defined in the FPGA Verification Plan, used to verify the FPGA compliance to the FPGA specification.

Compression parameters for simulation

No.	Parameter	Core		
		CCSDS123	Embedded CCSDS123	Embedded CCSDS121
Predictor constants				
1	Number of bands used for prediction **P**	3	3	3
2	Prediction mode	full	full	full
3	Local sum type	neighbour oriented	neighbour oriented	neighbour oriented
4	Weight component resolution **Omega**	10	10	10
5	Register size **R**	32	32	32
6	Weight update scaling exponent final parameter **v_max**	3	3	3
7	Weight update scaling exponent initial parameter **v_min**	-1	-1	-1
8	Weight update factor change interval **t_inc**	4	4	4
9	Weight initialization mode	default	default	default
Sample-adaptive encoder constants				
10	Initial count exponent **gamma_0**	1	1	1
11	Accumulator initialization type	constants	constants	constants
12	Accumulator initialization constant **k**	3	3	3
13	Rescaling counter size **gamma***	6	6	6
14	Unary length limit **Umax**	16	16	16
Block-adaptive encoder constants				
15	Block size **J**	-	-	16
16	Reference sample interval **r**	-	-	32
17	Code option	-	-	basic

Reference file generation

- Image files for simulation prepared with a Python script – all files containing samples with incremental values, starting from 0x00.
- Compressed reference files prepared with the Compressor tool distributed as a part of the WhiteDwarf Data Compression Evaluation Tool available at ESA website.
- Compressed output generated by compression cores is compared with prepared reference files at the end of the simulation.

Verification results

Passed.

On document	PLIIS-SYDPL-SFIC-PL-0002_is1A FPGA Verification Plan					
Last modification Date/time	15.04.2021					
Environment Version	SFIC_DB_0003					
Test ID	**Status**	**Type**	**Operator**	**Version**	**Run date**	**Comment**
TAG-IC-TP-FPGA-0201	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.4
TAG-IC-TP-FPGA-0202	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.5
TAG-IC-TP-FPGA-0203	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.6
TAG-IC-TP-FPGA-0204	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.7
TAG-IC-TP-FPGA-0205	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.8
TAG-IC-TP-FPGA-0206	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.9
TAG-IC-TP-FPGA-0207	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.10
TAG-IC-TP-FPGA-0208	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.11
TAG-IC-TP-FPGA-0209	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.12
TAG-IC-TP-FPGA-0210	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.13
TAG-IC-TP-FPGA-0211	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.14
TAG-IC-TP-FPGA-0212	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.15
TAG-IC-TP-FPGA-0213	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.16
TAG-IC-TP-FPGA-0214	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.17
TAG-IC-TP-FPGA-0215	CLOSED	Simulation	D. LINOWSKI	SFIC_DB_0003	14.04.2021	Refer to §8.18
Legend:						
Status = CLOSED if test is passed and successful on configured item, OPEN otherwise.						
Status, Operator, Version and Run date are mandatory for any CLOSED Test ID.						

Synthesis and layout

Entire design has been synthesised with Synplify Pro tool(Q-2020.03M-SP1) and implemented with Libero SoC (v12.6) for the following device:

- Family: RTG4
- Device: RT4G150
- Package: 1657 CG
- Speed grade: -1

Resource Usage

Type	Used	Total	Percentage
4LUT	47791	151824	31.48
DFF	29470	151824	19.41
I/O Register	0	2151	0.00
User I/O	114	717	15.90
-- Single-ended I/O	92	717	12.83
-- Differential I/O Pairs	11	358	3.07
RAM64x18	116	210	55.24
RAM1K18	166	209	79.43
MACC	27	462	5.84
H-Chip Globals	16	48	33.33
CCC	2	8	25.00
RCOSC_50MHZ	0	1	0.00
SYSRESET	1	1	100.00
SERDESIF Blocks	1	6	16.67
FDDR	1	2	50.00
GRESET	1	1	100.00
RGRESET	24	206	11.65

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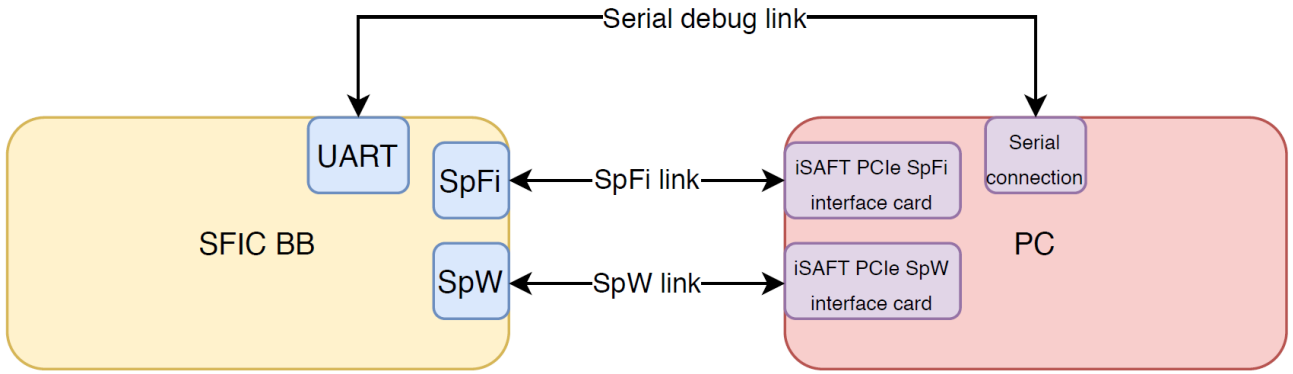
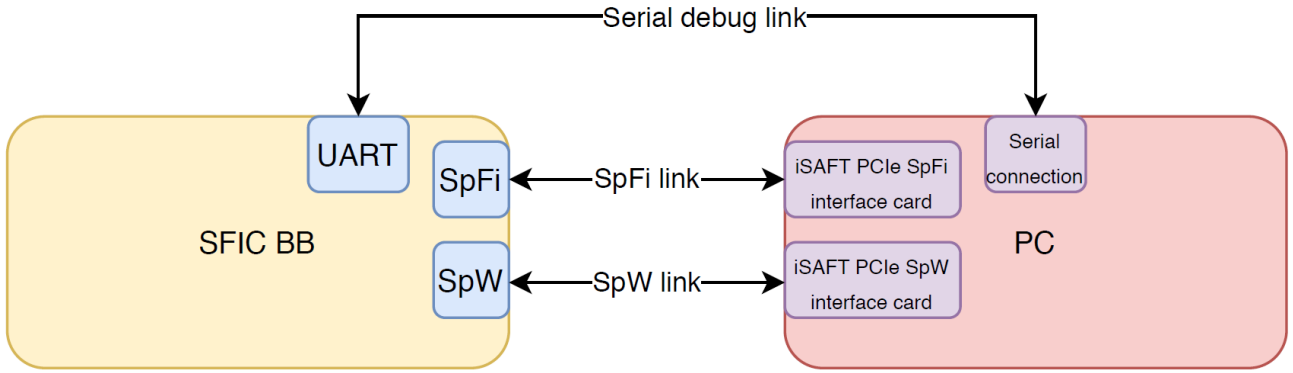
General HW test setup #1



The Breadboard Model of the SFIC (SFIC BB) consists of:

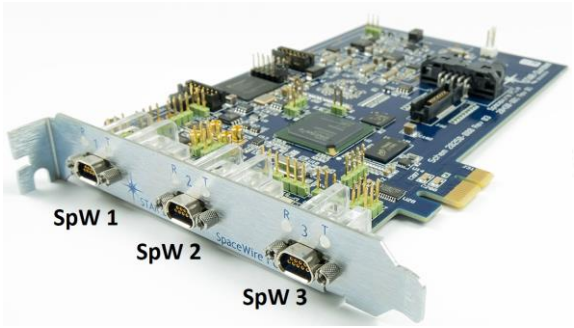
- Microsemi RTG4 development kit,
- FMC SpaceWire/SpaceFibre Board from STAR-Dundee.

General HW test setup #2



The test-PC incorporates 2 PCIe boards offering SpaceWire and SpaceFibre interfaces:

- STAR-Dundee SpaceWire PCI Express
- Teletel iSAFT Quad SpaceFibre PCIe



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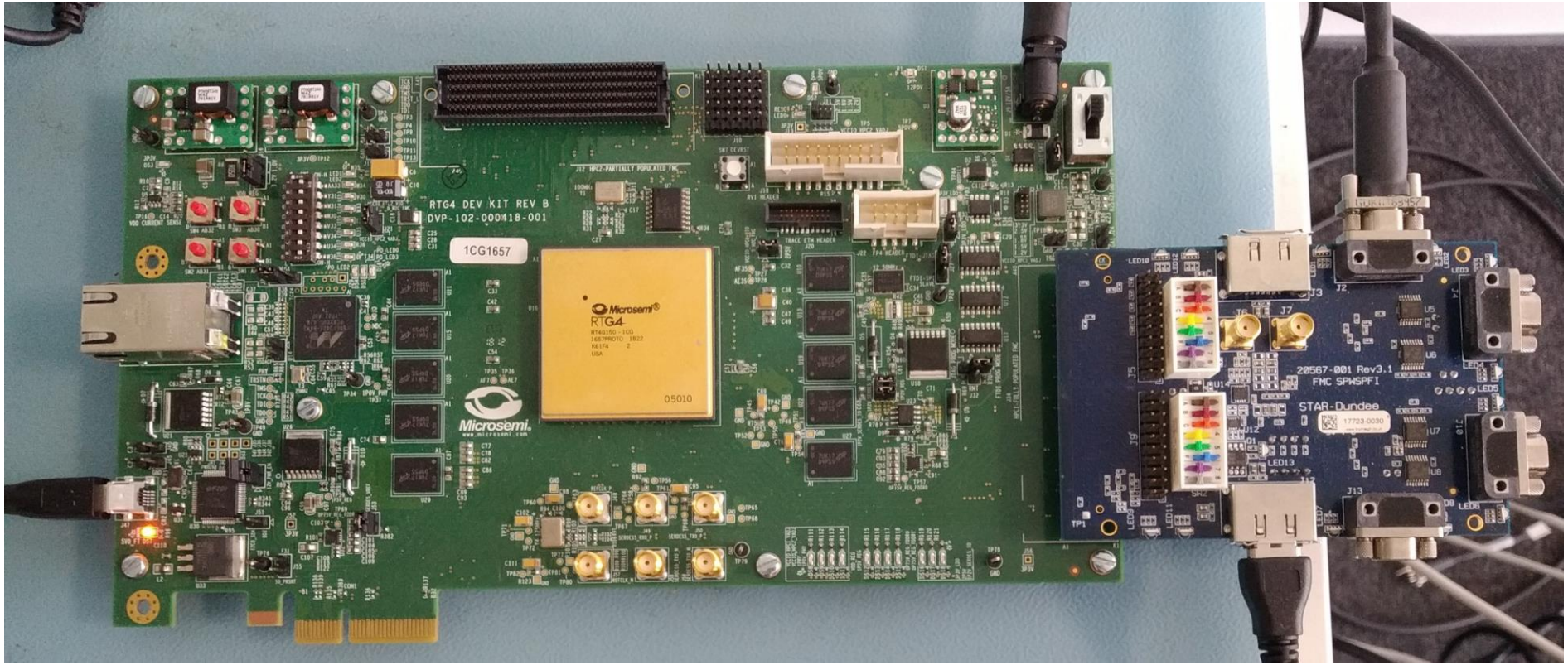
Actual view from the lab

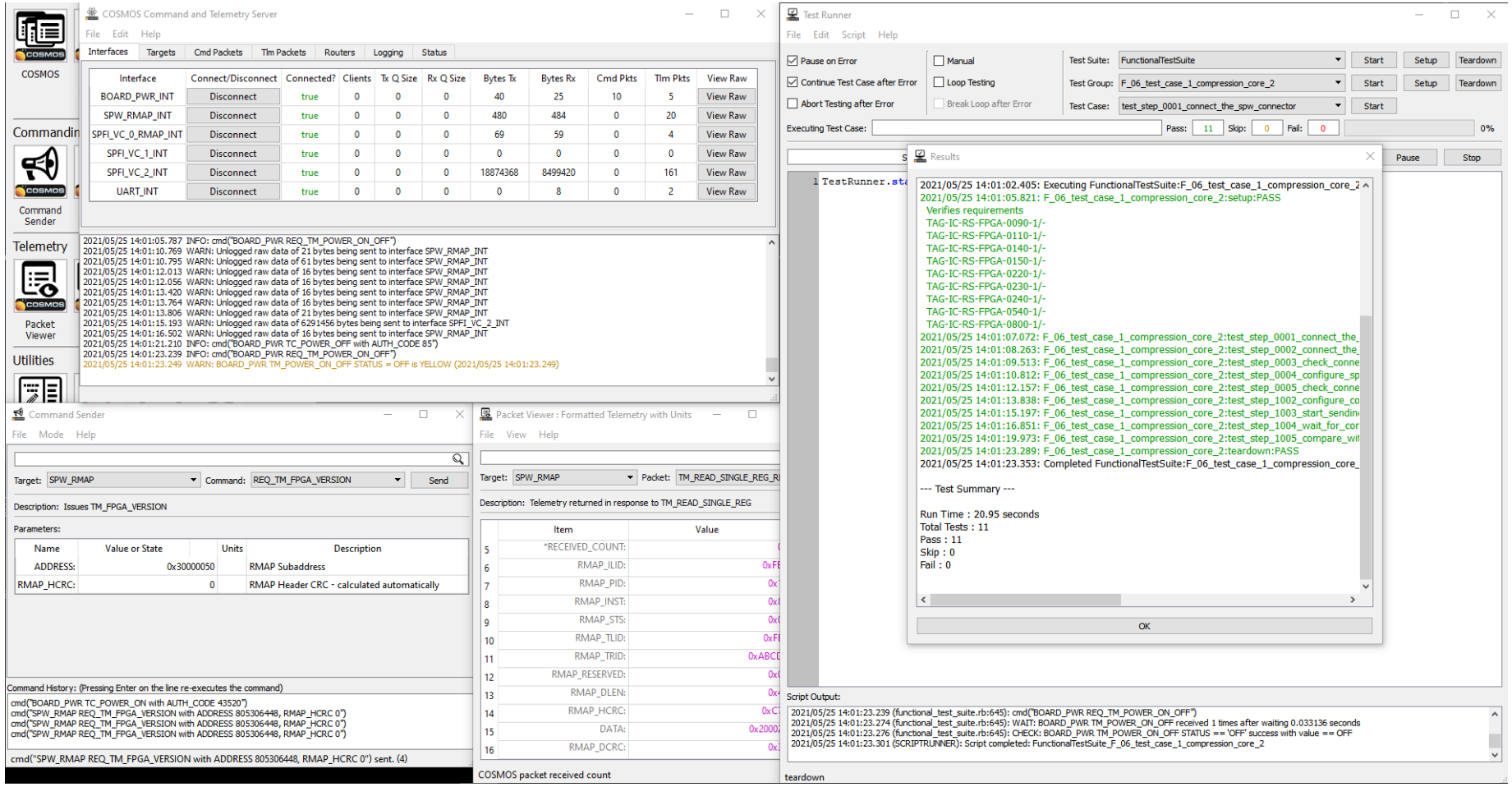


Software used

Ball Aerospace COSMOS software suite can be used to control a set of embedded systems. These systems can be anything from test equipment to development boards and satellites.

In SFIC, it has been used on the test PC to orchestrate overall tests execution by controlling all used communication interfaces.

Software used



Reference file generation

Actual multi- and hyperspectral satellite images have been used (for AVIRIS and LANDSAT) as an input for compression.

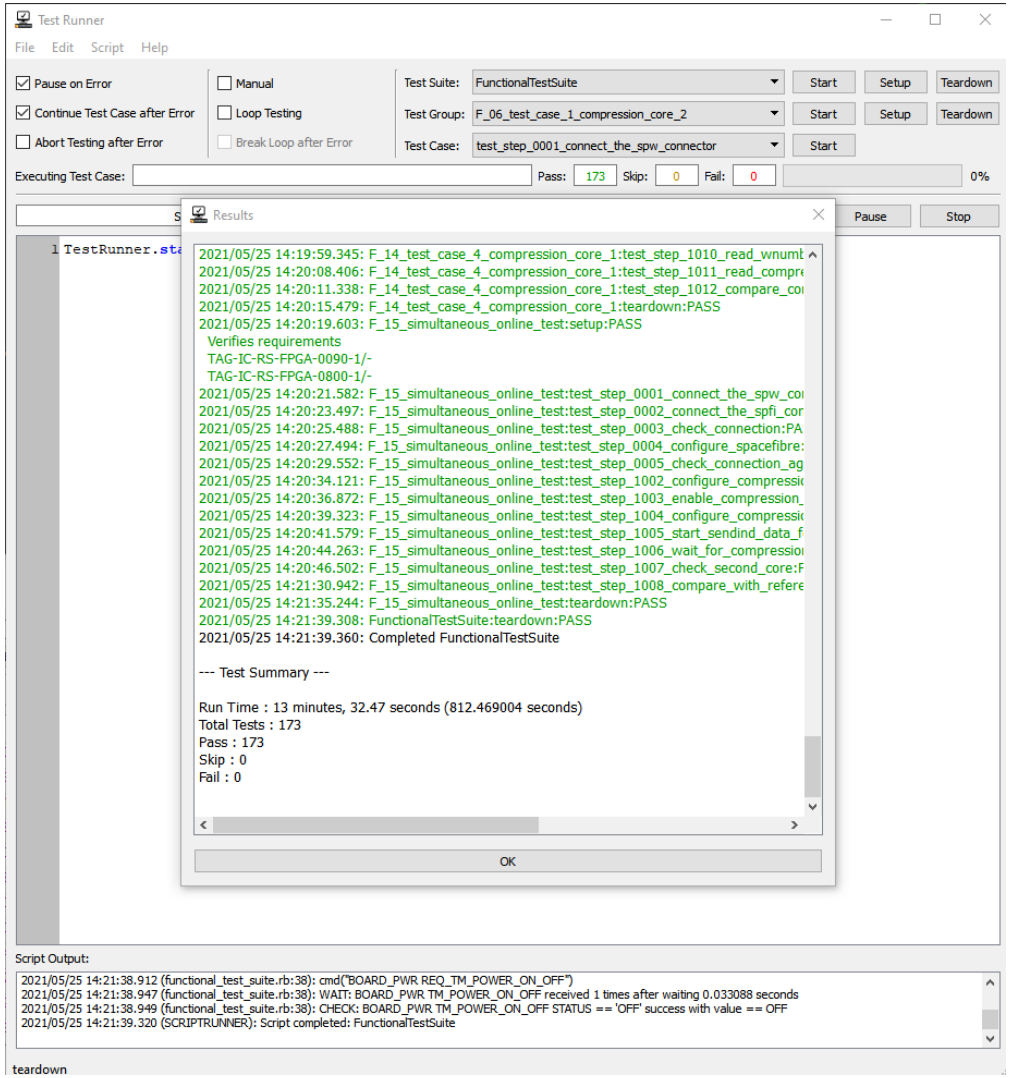
Compressed reference files have been prepared in the same manner as for simulation.

Total: 15 Functional Test Cases and 4 Performance Test cases.

No.	Name	Dataset	Nx	Ny	Nz	D	Sign	Endianness
1	aviris_crop_raw_h512w512n224_uint16_be	AVIRIS	512	512	224	16	signed	big endian
2	aviris_crop_raw_h128w256n224_uint16_be	AVIRIS	256	128	224	16	signed	big endian
3	aviris_crop_raw_h64w128n224_uint16_be	AVIRIS	128	64	224	16	signed	big endian
4	landsat_h1024w1024b6_uint8	LANDSAT	1024	1024	6	8	unsigned	little endian

HW validation results

Passed.



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Performance results

Each compression core throughput has been calculated by dividing amount of transmitted data by the core compression time measured inside the FPGA.

Core frequency: 50 MHz

AHB frequency: 50 MHz

Maximum throughput reached for compression core 1 (SHyLoC) **~763 Mbps (~0.745 Gbps)**

Parameter	Core 1 [Mbps]	Core 2 [Mbps]
Online mode core throughput	**762.809**	228.881
Offline mode core throughput	186.440	173.966

Summary

- SYDERAL Polska presented a demonstrator of SpaceFibre technology usage for image processing applications on the high-performance RTG4 FPGA based development board.
- CCSDS-123 and CCSDS-121 IP cores were used both as a standalone modules and together as SHyLoC.
- AVIRIS and LANDSAT dataset images compression was performed both in online and offline modes.
- SHyLoC (Compression core 1) parameters were possible to be updated in run-time.
- It was possible to use both compression cores simultaneously.
- Throughput of ~763 Mbps using SpaceFibre interface has been achieved for SHyLoC.

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Thank you for your attention!