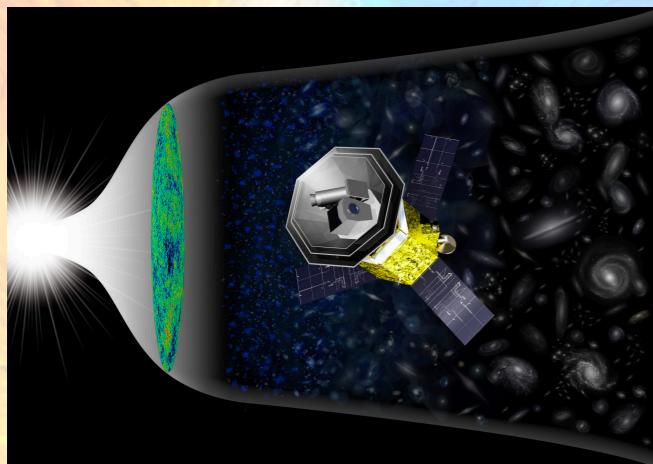


# FPGAs usage in some science projects at IRAP

Stéphan Maestre ( CNRS ), Jérémy Guillermand ( Alten )  
Damien Rambaud ( CNRS ), Bruno Moutounaick ( CNRS )





IRAP is a joined lab of the French National Research Organization CNRS and of the University Paul Sabatier (UPS) in Toulouse. IRAP is also part of the Observatoire Midi-Pyrénées (OMP), an organization federating 6 laboratories working in the field of Earth and Space Sciences.

Instrumental IRAP contributions to various space missions

Key numbers :

- 300 persons
- 110 researchers,
- 70 engineers ( permanent staff )
- 15 visitors
- 40 PhD
- 20 Post-docs

Scientific themes	Past missions	Missions under study / dev.
First Universe Big Structures, Galaxy	Planck (ESA)	ATHENA (ESA) LITEBIRD (JAXA)
HE, Compact Objects, Explosive Systems	Integral (ESA) XMM (ESA)	ATHENA (ESA) SVOM (CNSA)
IMS, Astro Chemistry, Dust/ Gaz/Molecules	Herschel (ESA) Planck(ESA)	LITEBIRD (JAXA)
Sun, space plasmas	Double Star (CNSA) Taranis (CNES)	Solar orbiter (ESA)
Planetary Objects, Surface and Environnements	MSL (NASA) Bepi Colombo (ESA) Maven (NASA) JUNO (NASA) Mars2020 (NASA)	JUICE (ESA) DORN ( CNES )

# Outline

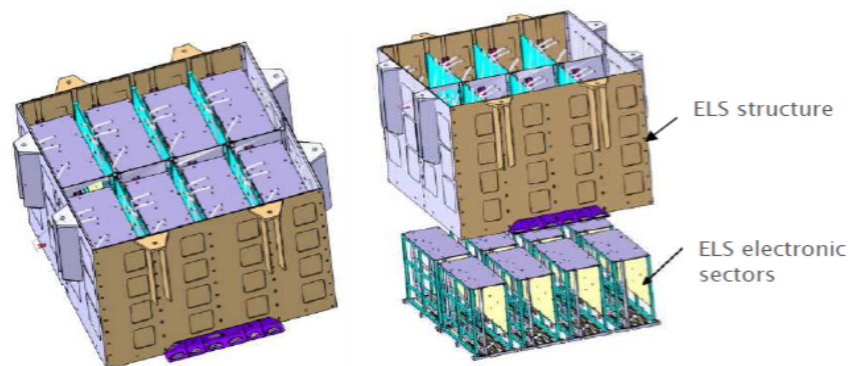
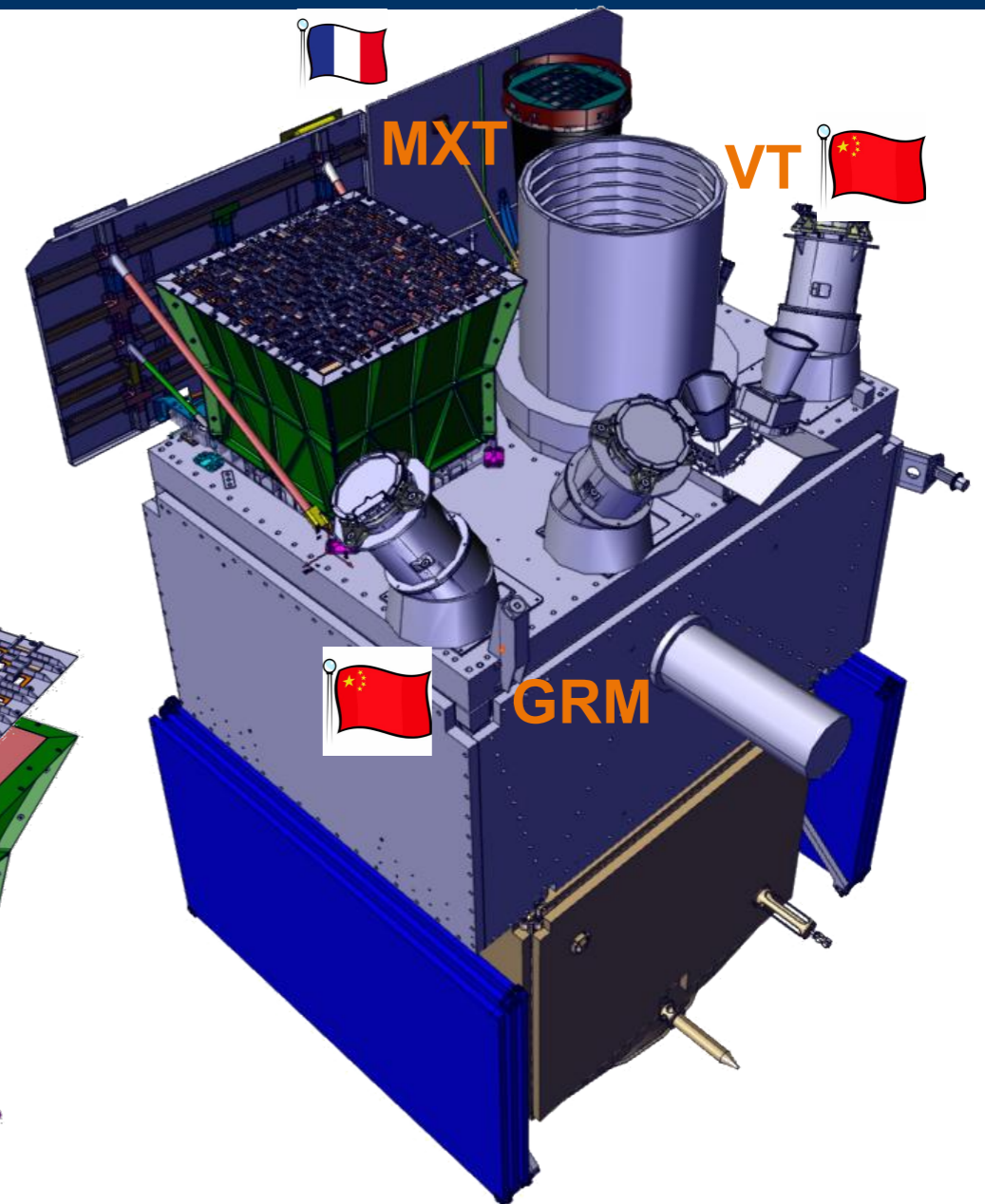
- Radtolerant FPGAs use cases :
  - SVOM / Eclairs
  - DORN
  - Comet Interceptor
  - Litebird

# SVOM / Eclairs



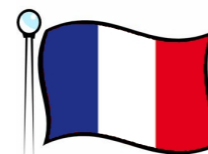
SVOM is a French-Chinese astronomy mission to detect gamma-ray bursts generated by the explosion of massive stars or the merger of neutron stars or black holes.

- IRAP is in charge of the detection plane, Front-end and digital readout electronic of the Eclairs instrument
- The instrument will measure energy between 4 and 150KeV.
- 1000 cm<sup>2</sup> detection plane
- 6400 CdTe detectors



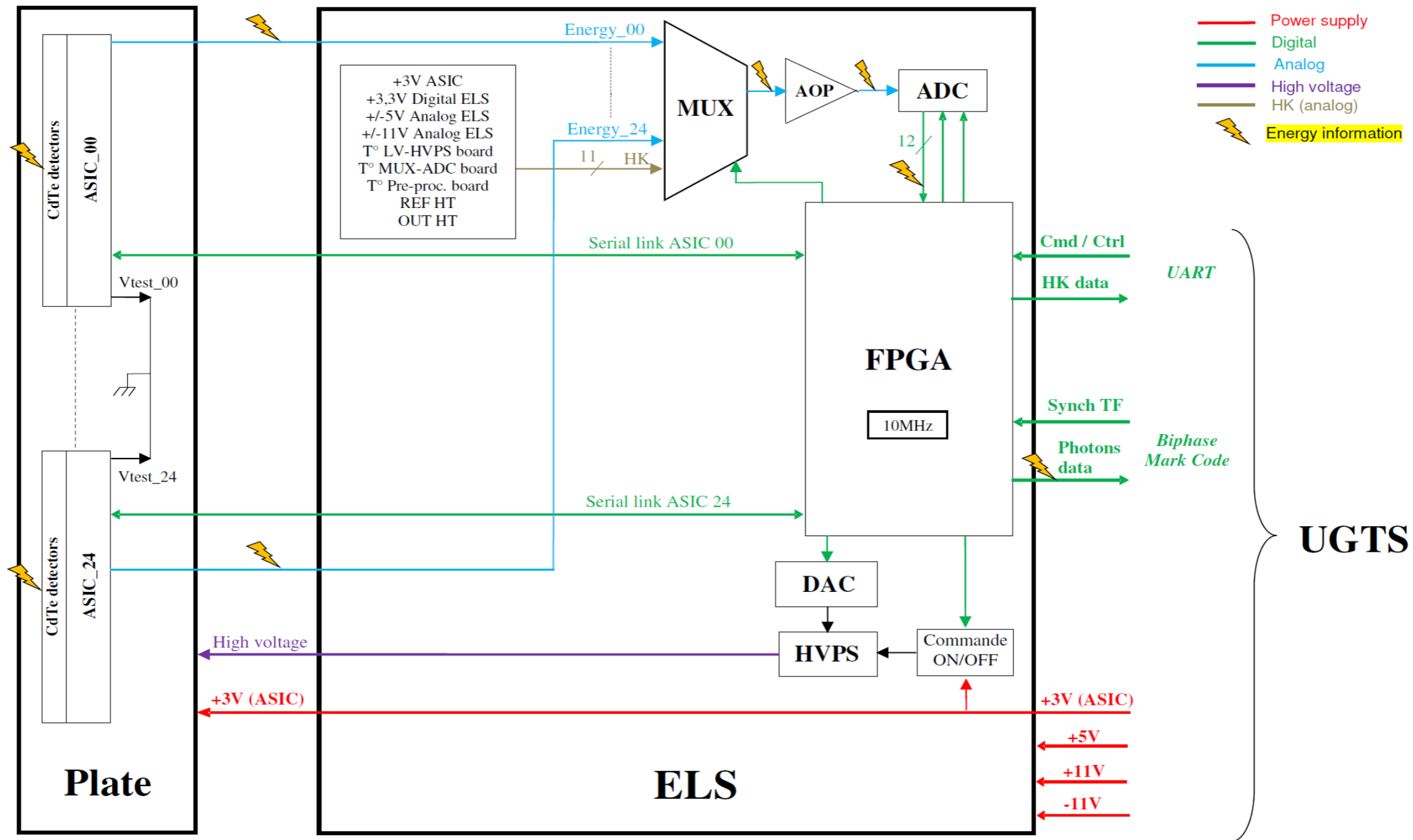
## ECLAIRs

- One of the 4 instruments of the SVOM Mission
- Developed and provided by French teams
- Dedicated to GRBs detection and early alert



200 Asics managed by 8 NG-Medium FPGAs

# SVOM / Eclairs



# SVOM / Eclairs

This design runs at 10MHz. It was originally implemented on an atmel ATF280.

The synthesis process on the ATF280 was not possible with Figaro tool.

On this project NG-Medium has been selected because :

- It was the only ITAR-Free component available to replace the ATF280
- Synthesis was powerful enough to be able to route the design

	Xilinx (ProtoDpix) Spartan 6	ATMEL ATF280	NanoXplore brave NG-MEDIUM
Taux d'occupation Post-routage	6%	70% with 70% of features	44%
Bitstream generation time	20 min	4 h	7 min
Real life test	yes	yes	yes
Power supplies	-	3.3V, 1.8V	3.3V, 2.5V, 1.2V
Packaging	-	QPF352	QPF352

Reporting instances

4-LUT	DFP	XLUT	Carry	Register file block	Cross domain clock	Clock Buffer	Clock switch	Digital signal processor	Memory block	WFG	PLL
7497/32256 (24%)	4021/32256 (13%)	0/2016 (0%)	1978/8064 (25%)	0/168 (0%)	0/0	0	0/336 (0%)	0/112 (0%)	7/56 (13%)	5/32 (16%)	1/4 (25%)

**Launch 12/2023 from China**

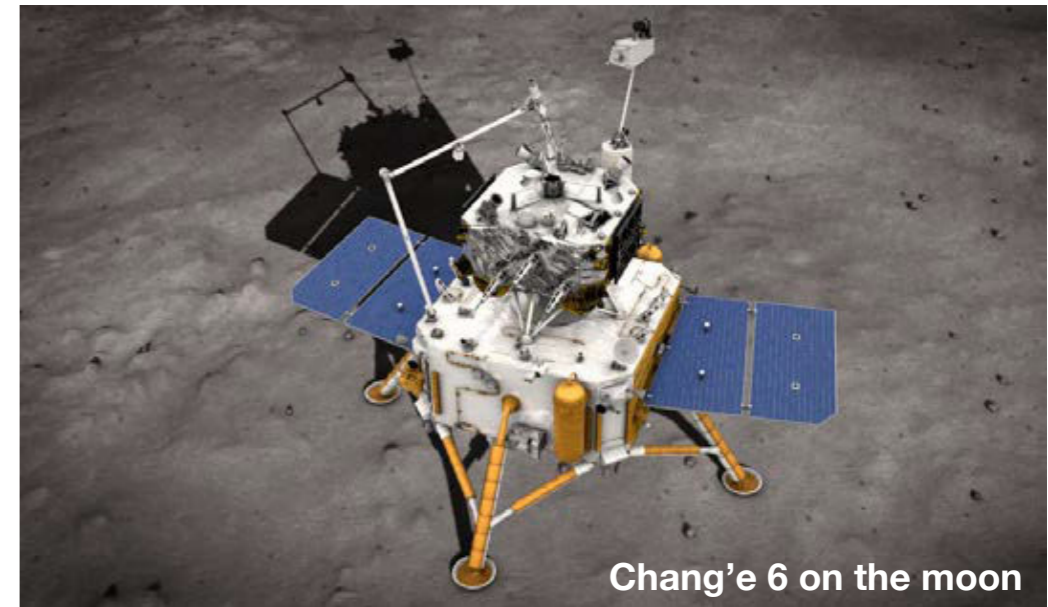
Configuration bits report		
Total count	6189616	100 %
Total used	2732564	44.14 %
Total critical	226499	3.65 %

**Eclairs leaving CNES for delivery !**

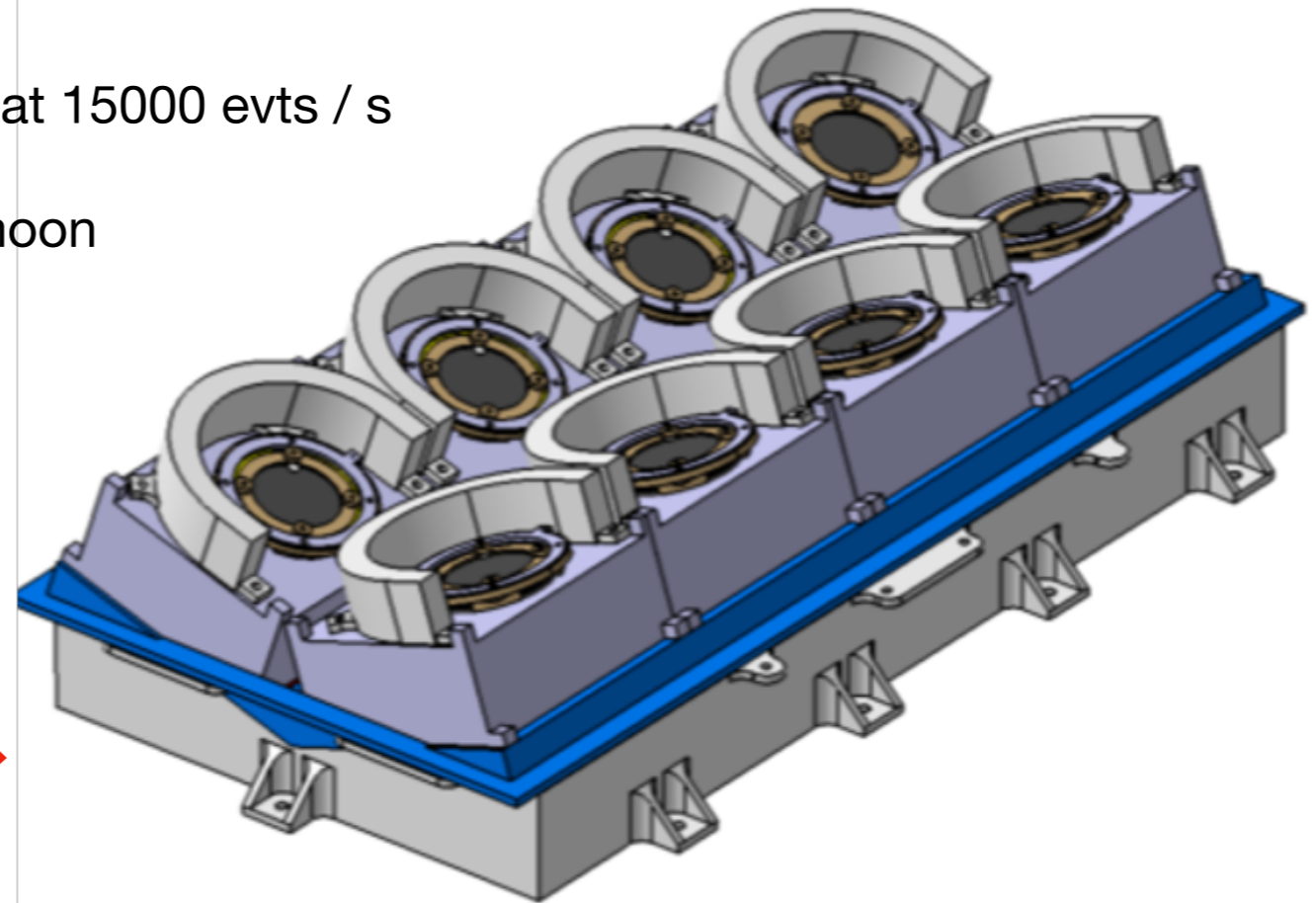


DORN is dedicated to measuring radon on the moon.

Objectives: to study the degassing of the regolith but also the transport of this radioactive gas in the exosphere of the Moon with possible extrapolations to other species such as water.



- ✓ Acquisition of radon spectra by 8 detection heads at 15000 evts / s
- ✓ Mission duration : 110 hours cruise, 36 hours on moon
- ✓ Project started in 2020
- ✓ Delivery June 2023 for a flight in 2024

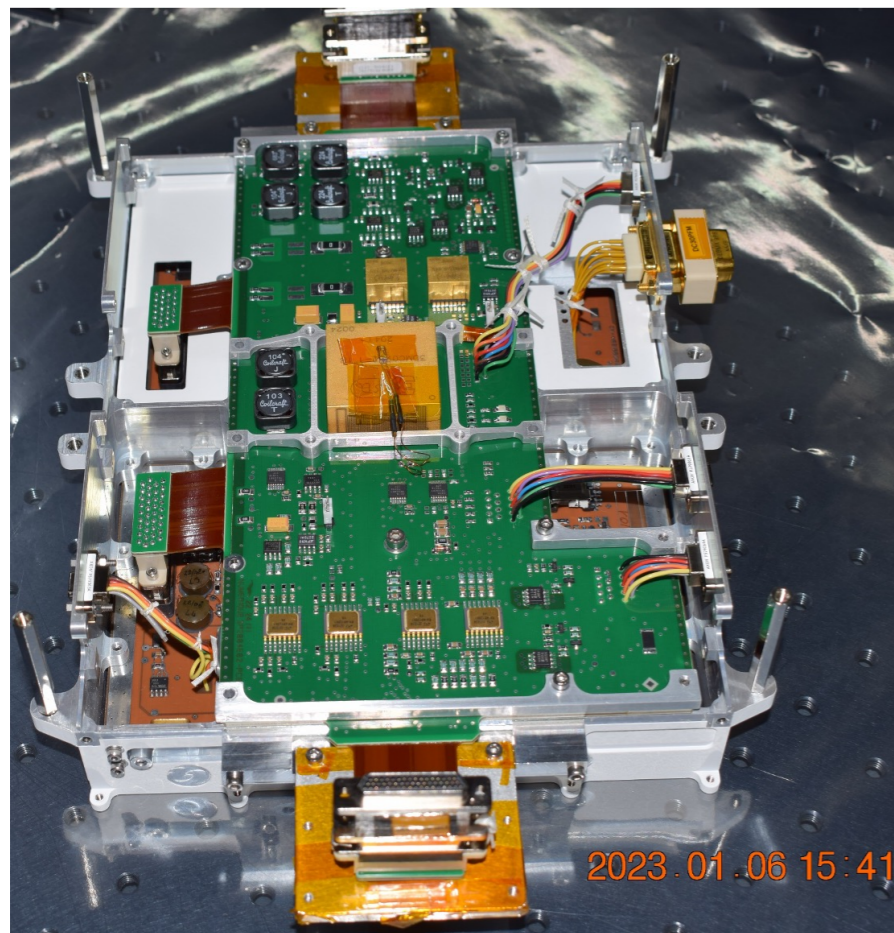


Launch 2024  
from China

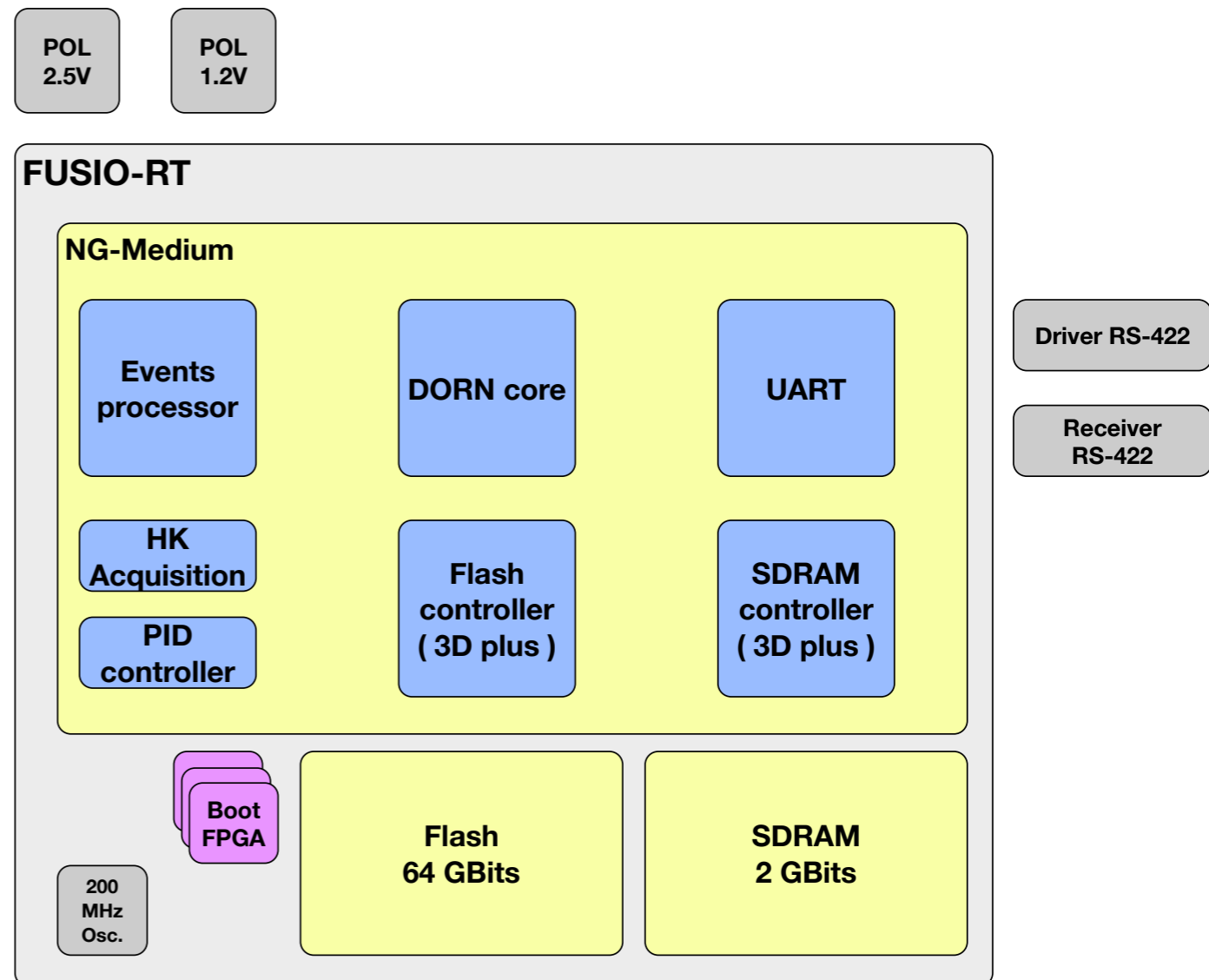
On this project, we use a FUSIO-RT @ 100MHz.

The FUSIO component is in charge of :

- TM/TC management
- HK acquisition
- Flash Control on AXI bus
- SDRam control on AXI bus
- Science signal processing
- Science products generation



DORN FPGA board electrical model





# DORN FPGA selection drivers and synthesis



## The DORN project constraints are the following :

- Fast project ( 3 years ) : for this reason FUSIO-RT is a good choice because it avoids the implementation of SDRAM and Flash on a PCB.
- Volume constraints : the instrument volume is rather small and the use of the FUSIO-RT allows a compact design.
- China export : FUSIO export to China is made easier by the use of ITAR free components.

## Challenges in the synthesis process

- High resources usage, the FPGA is almost full : we had to optimize the space by sharing resources ( multiple FIFOs implemented within one SRAM block for example ).
- Three clock domains ( 25, 50 and 100 MHz )
- The internal oscillator frequency of the NG-MEDIUM is different from chip to chip

## Synthesis results

```

+-----+
| Configuration bits report |
+-----+-----+-----+
| Total count | 6189616 | 100 % |
| Total used  | 5038695 | 81.4 % |
| Total critical | 456494 | 7.37 % |
+-----+-----+-----+
| Total Size | 5.20Mbits |
+-----+-----+-----+
    
```

### Reporting instances

4-LUT	DFF	XLUT	1 - bit Carry	Register file block	Cross domain clock	Clock Buffer	Clock switch	Digital signal processor	Memory block	WFG	PLL
16630/32256 (52%)	9268/32256 (29%)	0/2016 (0%)	4532/8064 (57%)	25/168 (15%)	0/0	0	0/336 (0%)	1/112 (1%)	37/56 (67%)	4/32 (13%)	1/4 (25%)

Estimated FE occupancy is 25474/32256 (79%)

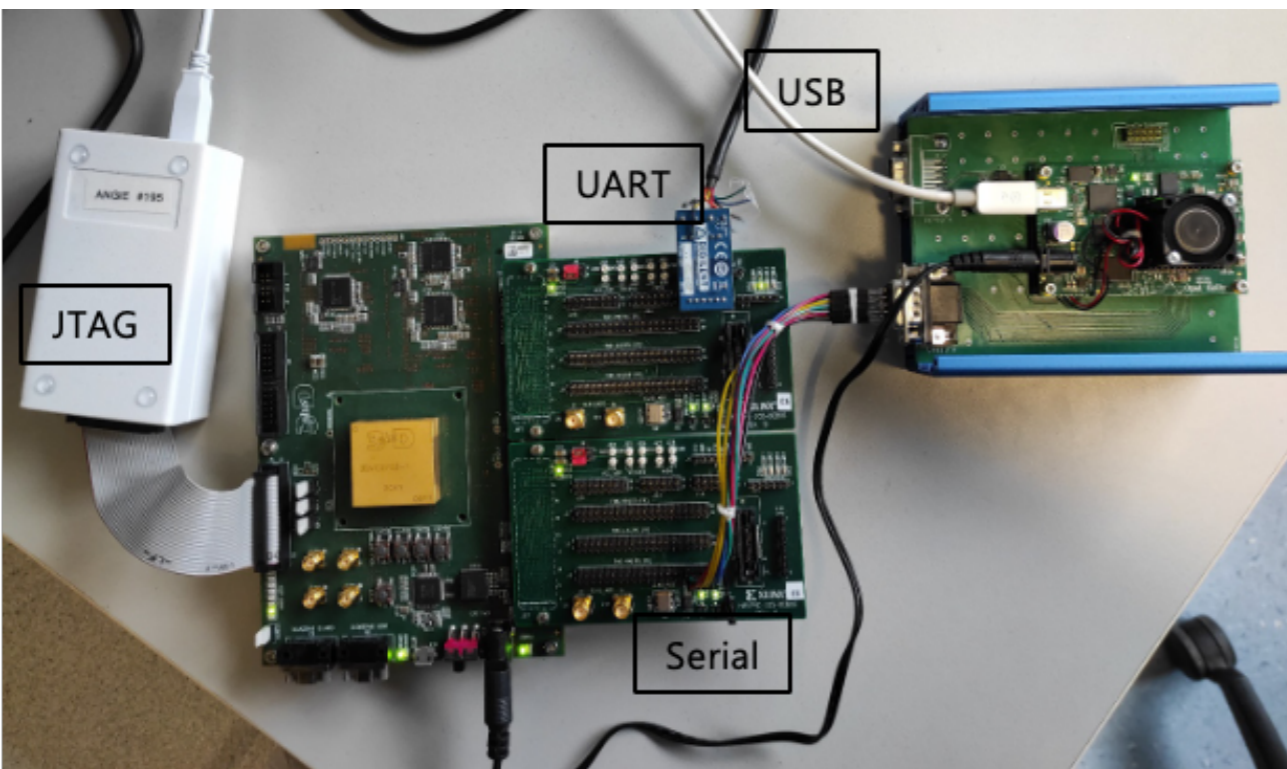
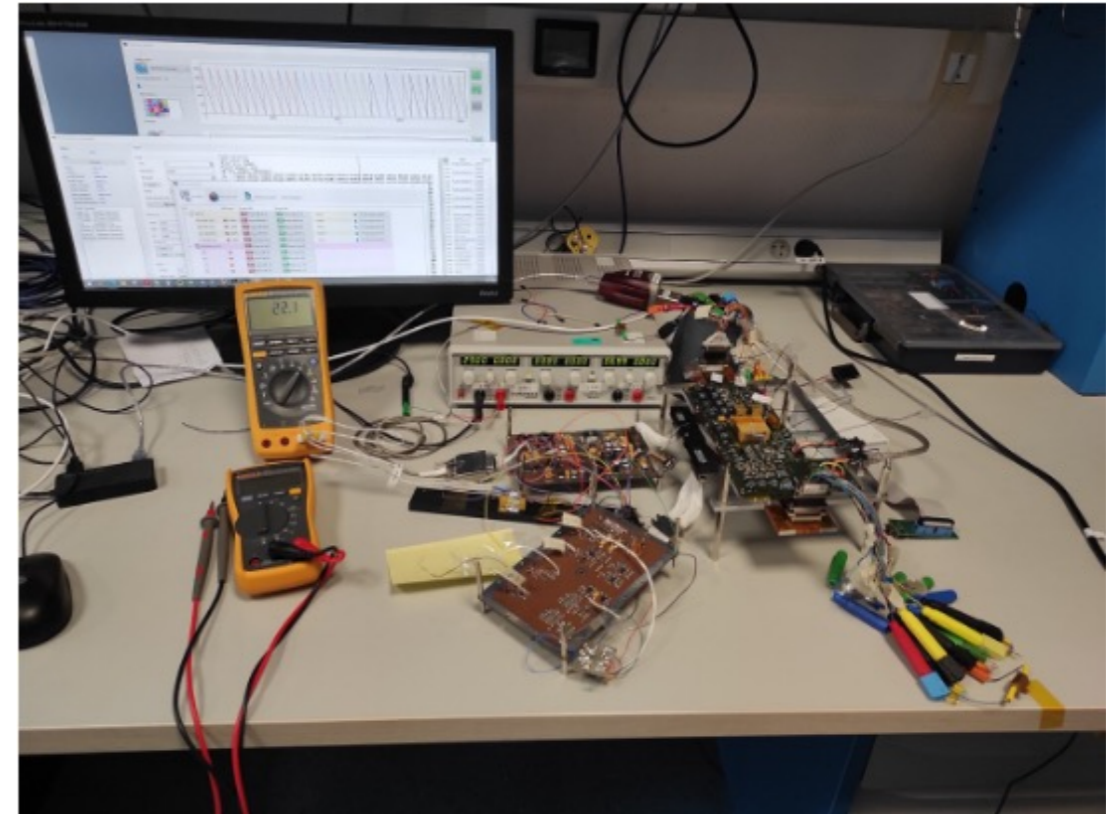
## VHDL code statistics

- 22 000 code lines ( DORN + 3DPlus IPs )
- SPI, AXI, UART and custom serial protocols

# DORN debug tools

## Software tools

- SIGASI IDE
- NX map 3
- Mentor Questasim



## Hardware tools

- Angie NX probe
- FUSIO-RT eval board
- Opal Kelly board with xilinx FPGA

## Goal:

Search for the evidence of cosmic inflation in the early Big Bang universe by the measurement of the cosmic microwave background (CMB) polarization signal

## Localization of the satellite:

L2 Lagrange point

## Detectors:

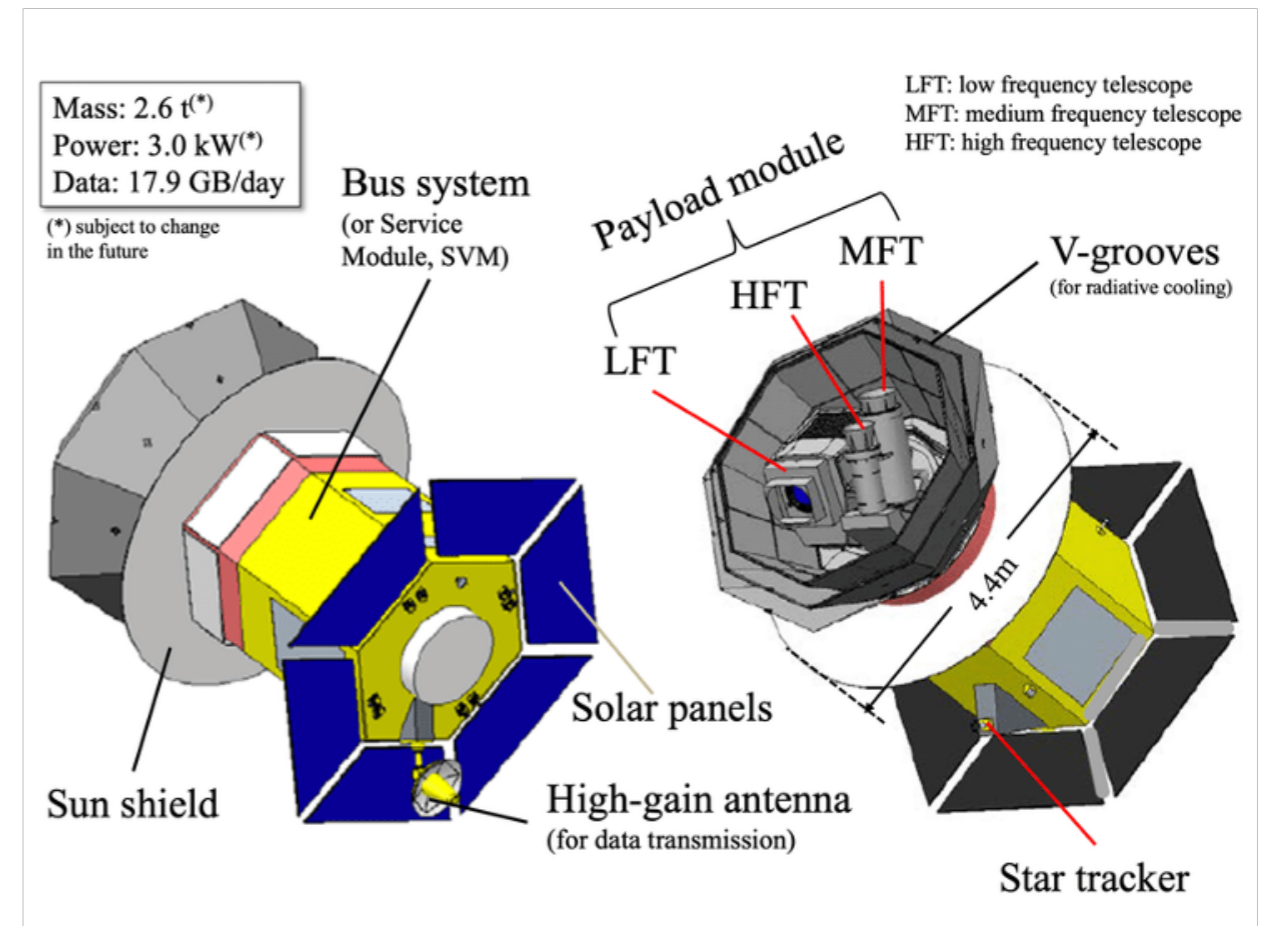
5000 bolometers cooled at 100mK

## 3 instruments (34GHz to 448GHz):

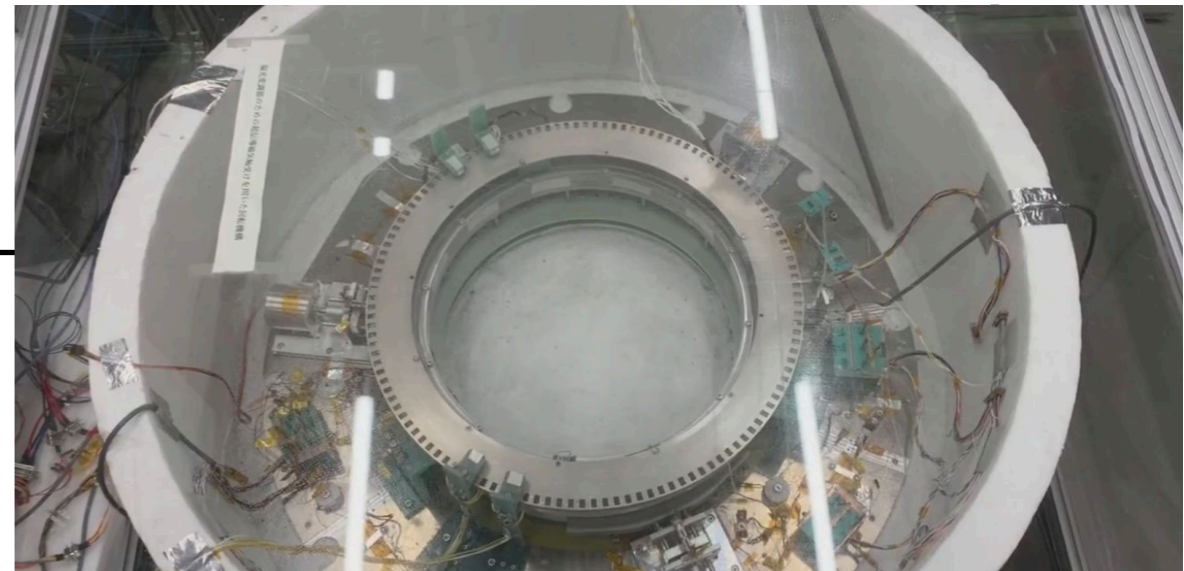
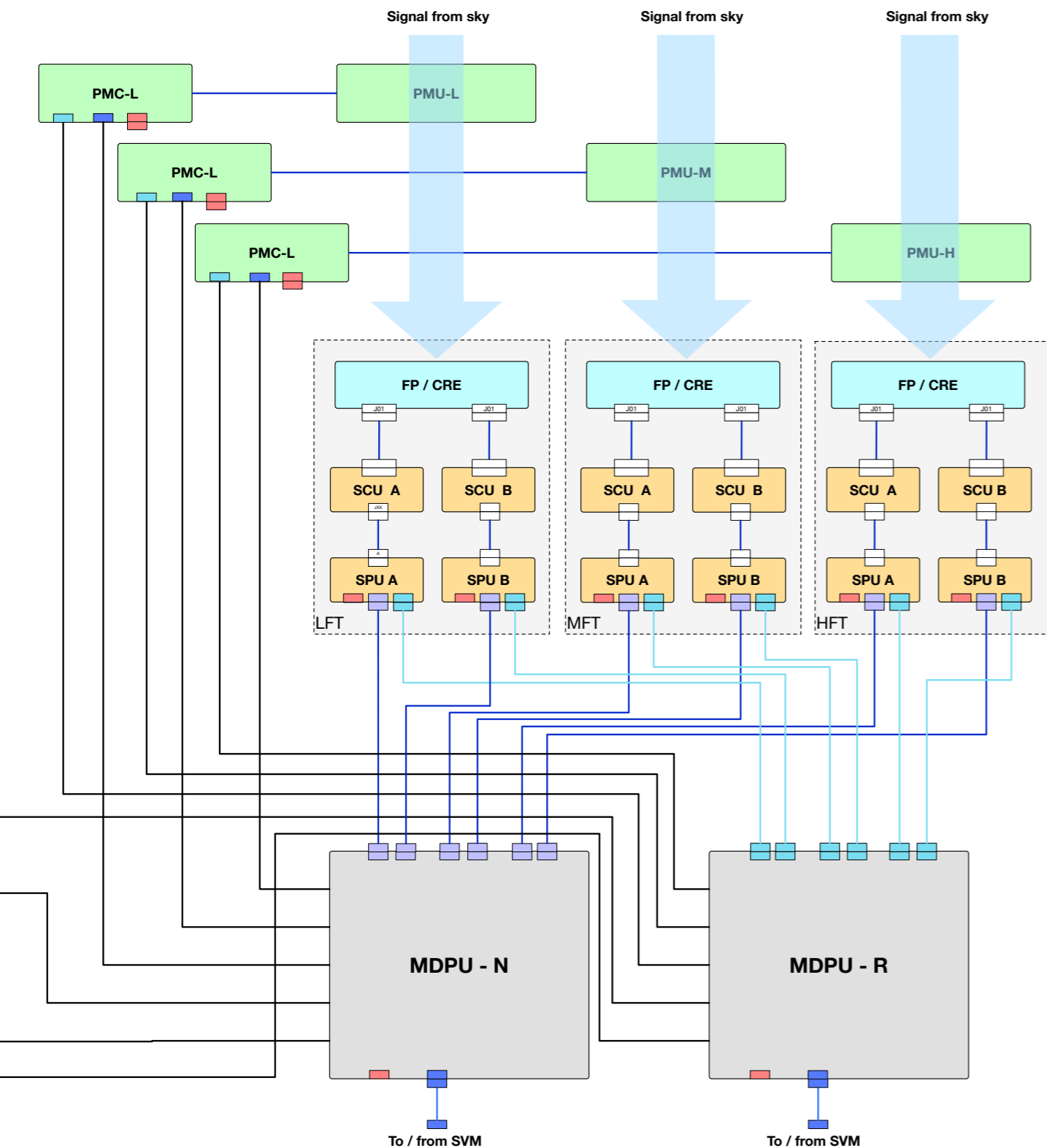
- Low Frequency Telescope
- Medium Frequency Telescope
- High Frequency Telescope

## Previous satellite:

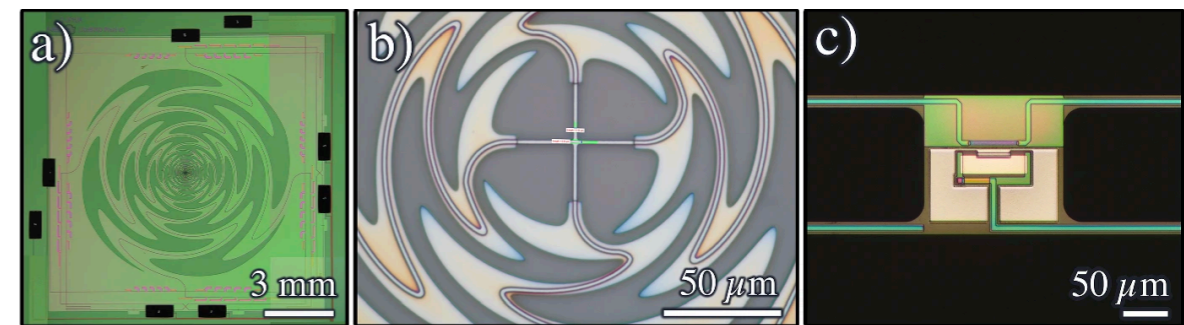
- COBE (NASA, 1989)
- WMAP (NASA, 2001)
- Planck (ESA, 2009)



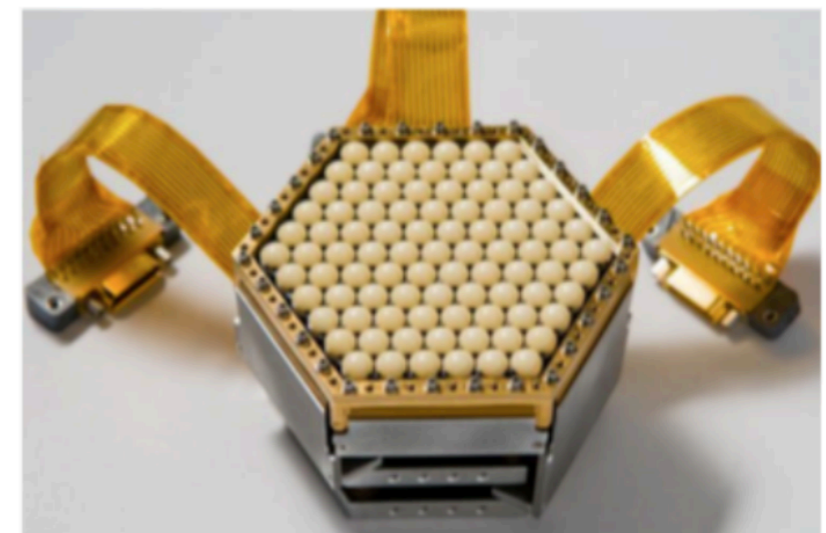
# Litebird items



The LFT half-wave plate,



the bolometers...



and a Litebird focal plane detectors assembly

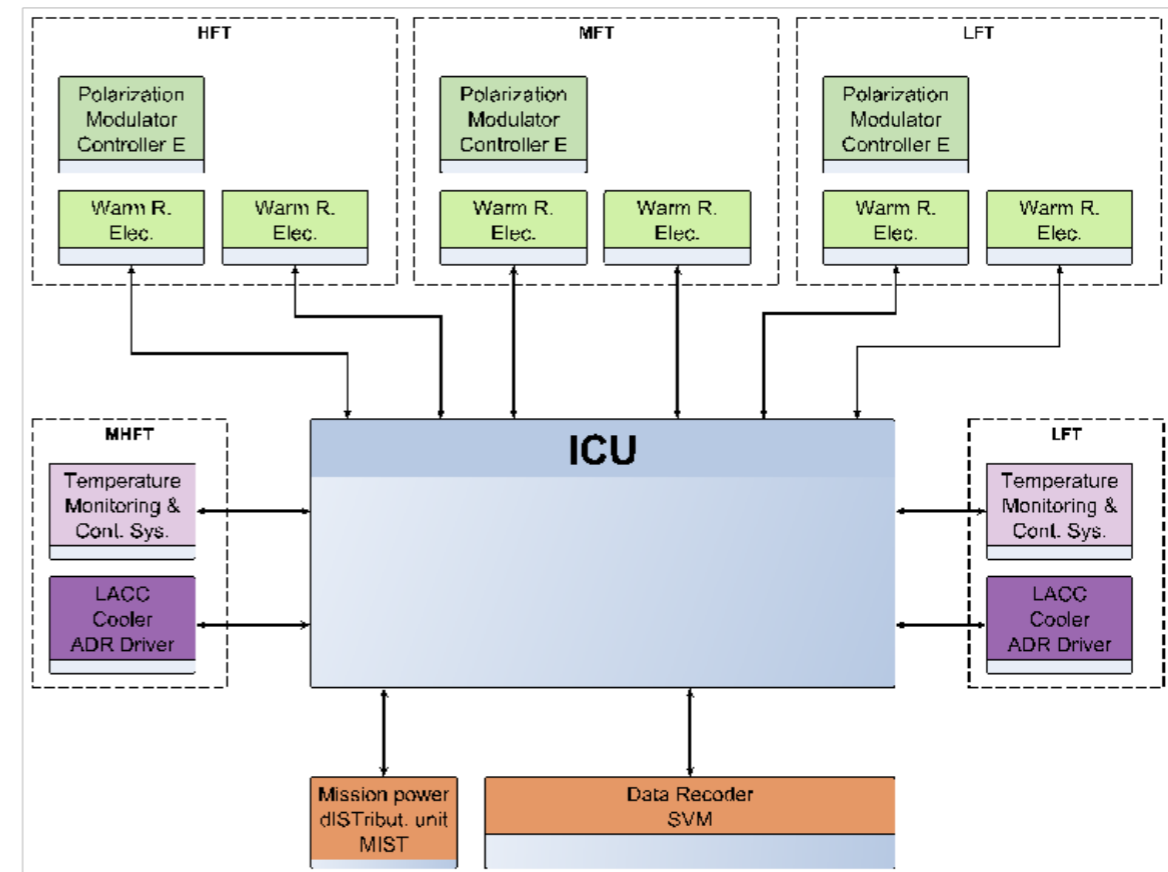


## Science signal key numbers

- 5000 TES detectors
- 152,6Hz sampling rate
- Raw signal : 6 Mbyte / s
- Science signal output rate : 400 Kbyte / s

## Functional Requirements:

- Communication with the Service Module (platform) via spacewire
- Communication with the 6 x Warm Readout Electronics
- Control of the cooler driver electronics via spacewire
- Control of the Polarization Modulator Controller
- FPGA firmware and software maintenance
- Implementation of any FDIR needed
- Science on-board processing






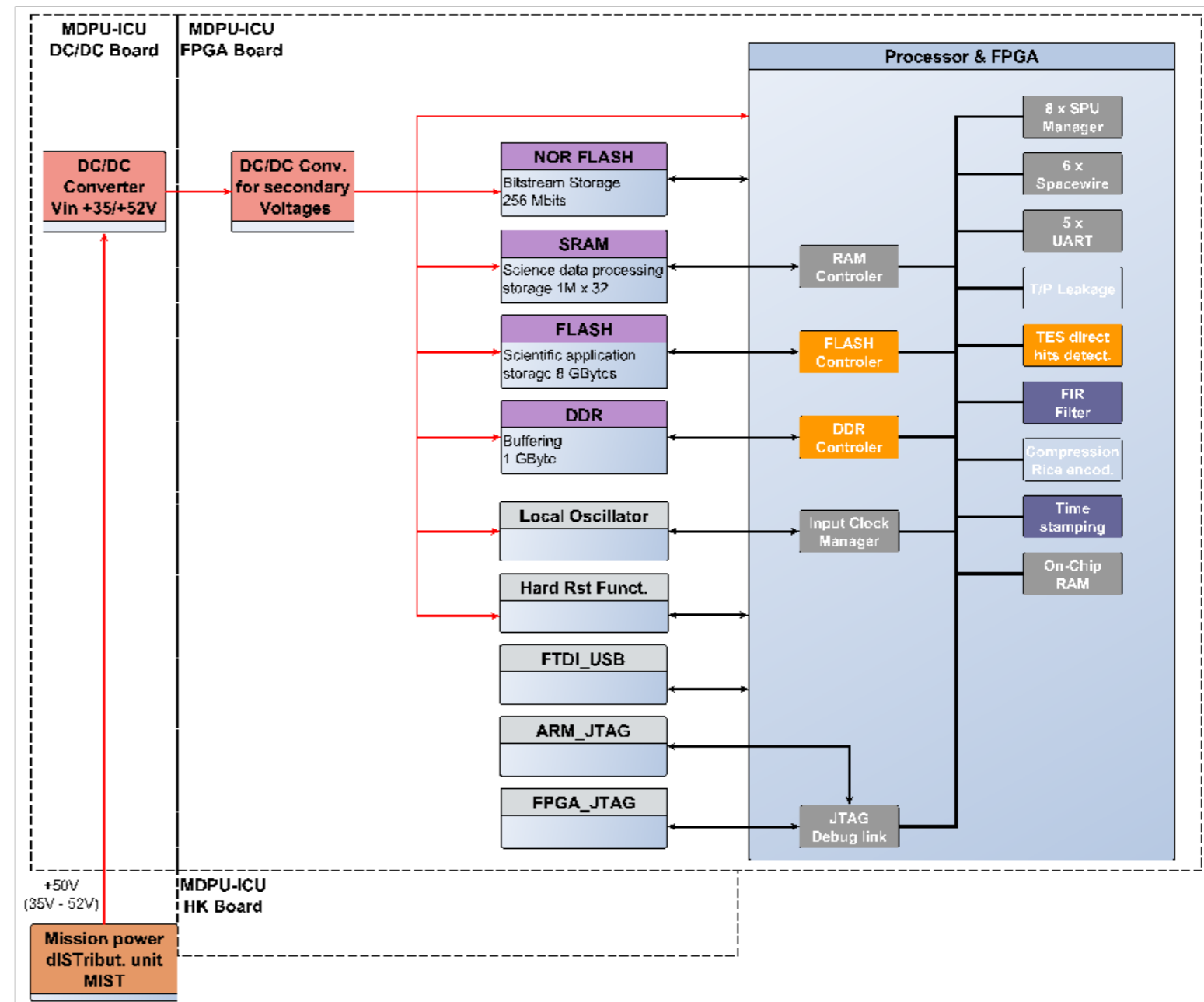
## Specs :

- NG-ULTRA
- 4 cores, ARM processor at 600MHz
- 1 M x 32 Static RAM
- 3 GBytes DDR3
- 8 GBytes Flash storage
- 6 Spacewire links
- 5 Serial links
- 8 Warm Electronic links

 Managed by the processor

 Managed by the FPGA

 Data processing managed by the FPGA



# Litebird - On-board processing



## FIR Filter feature:

- Convolution between the data & coefficients vect.
- 65 taps

## Occupancy (NG-LARGE target):

- Less than 25 DFlipFlop added
- 65 DSP blocks

Reporting instances					
4-LUT	DFF	XLUT	1 - bit Carry	Register file block	Digital signal processor
2/129024 (1%)	8/129024 (1%)	0/8064 (0%)	0/32256 (0%)	0/672 (0%)	65/384 (17%)

## Data treatment for 5200 channels

- Input : 152.6Hz \* 5200 channels

Method	Structure	Data length	Coeff length	Project frequency	Time to treat 1s of data
1	Transpose	24	18	<b>60MHz</b>	<b>&lt; 15ms</b>
2	Systolic	18	24	<b>100MHz</b>	<b>&lt; 10ms</b>



First investigations



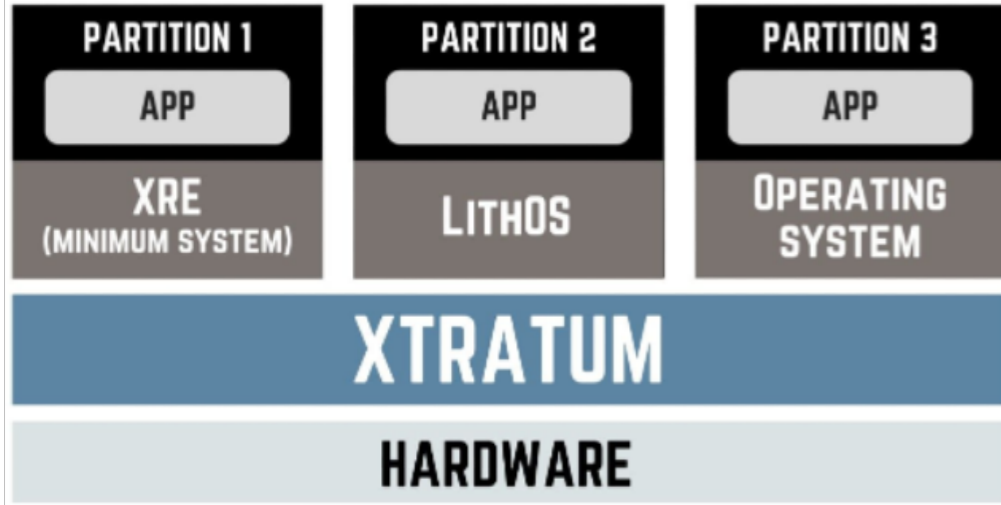
**Litebird FIR Filter can easily be implemented in NG-LARGE or NG ULTRA**

Function	Occupancy rate on NG-LARGE target		
	LUT	D Flip flop	Memory block
UART	<1%	<1%	<1%
Spacewire	<1%	<1%	~1%
SPU Manager	...	...	...
T/P Leakage Removal	...	...	...
TES direct hits detection	...	...	...
FIR filter	<1%	<1%	~1%
Compression (rice encod.)	...	...	...
Timestamping	...	...	...

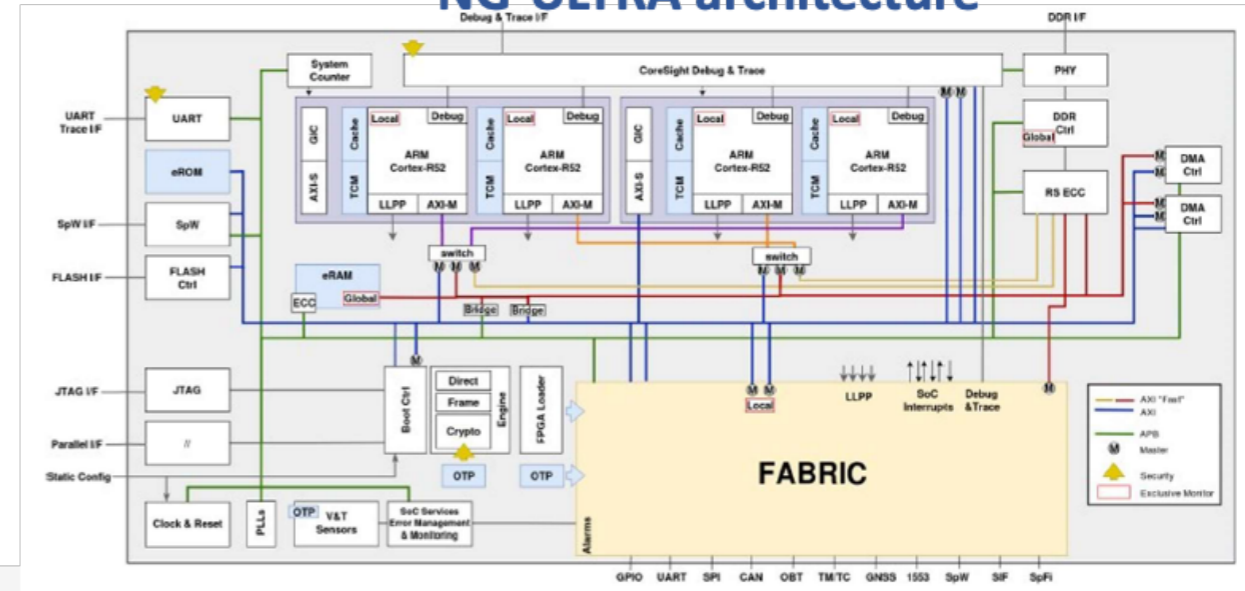
# Litebird - 2023 dvp setup



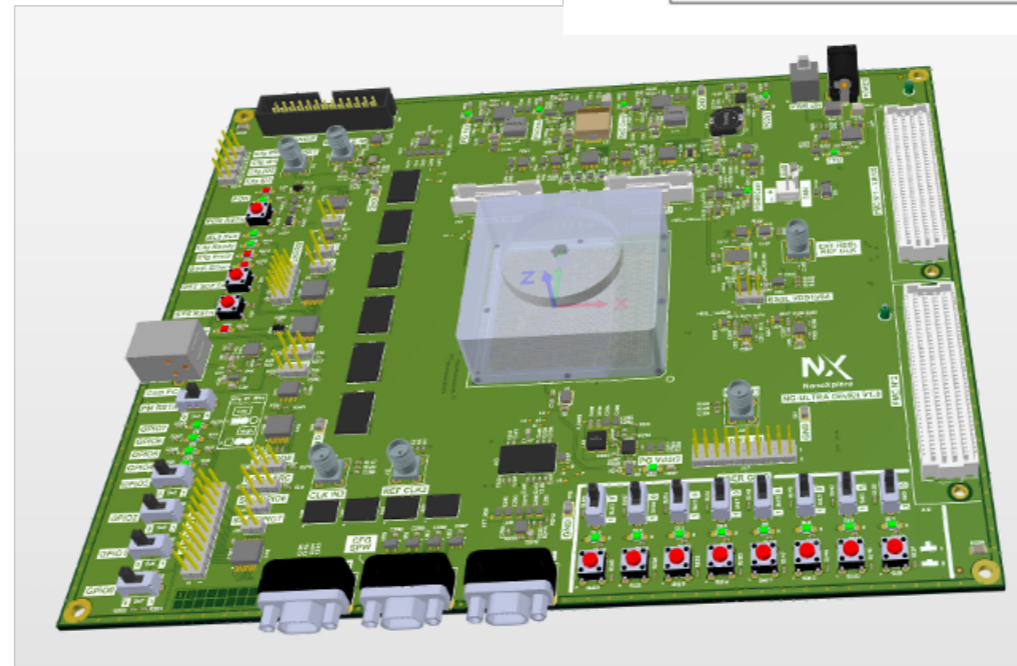
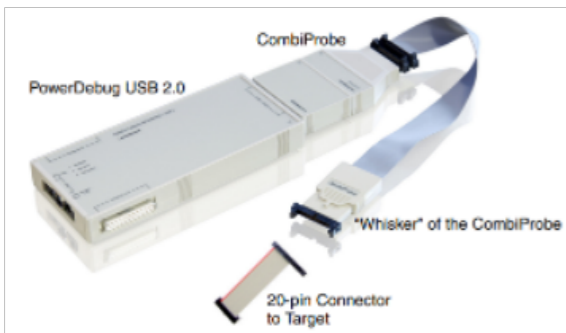
## XtratuM hypervisor



## NG-ULTRA architecture

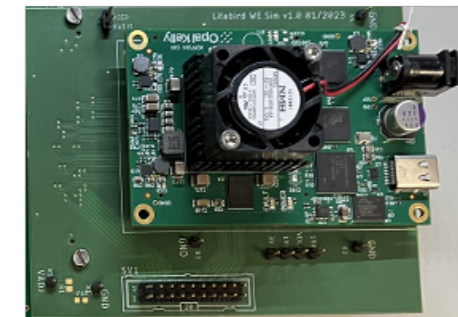


## Lauterbach probe



NG-ULTRA Dev Kit.

## WRE Sim



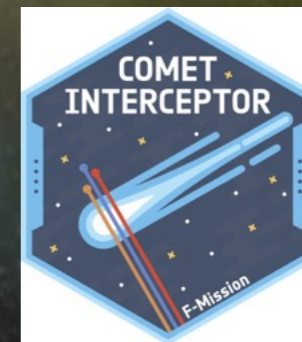


# Comet interceptor / LEES

Multiple views of cometary nucleus: views from three spacecraft reveal 3D structure of nucleus and coma from a single flyby



ESA first Fast-class mission – collaboration with JAXA  
Target: 1 pristine comet (to be identified)  
Launch: 2028 (companion of ARIEL)



The Low-Energy Electron Spectrometer (LEES) instrument is a part of dust field and plasma platform.

It will determine the electron density, temperature, and the velocity distribution functions of the local plasma environment of the solar wind and coma.

It will detect the suprathermal photoelectrons created in the coma. It will also measure the properties of negatively charged ions and dust.

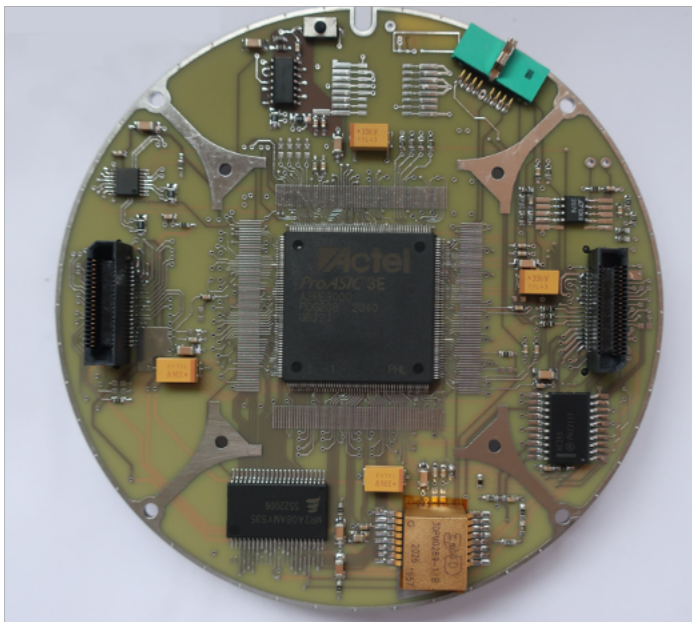
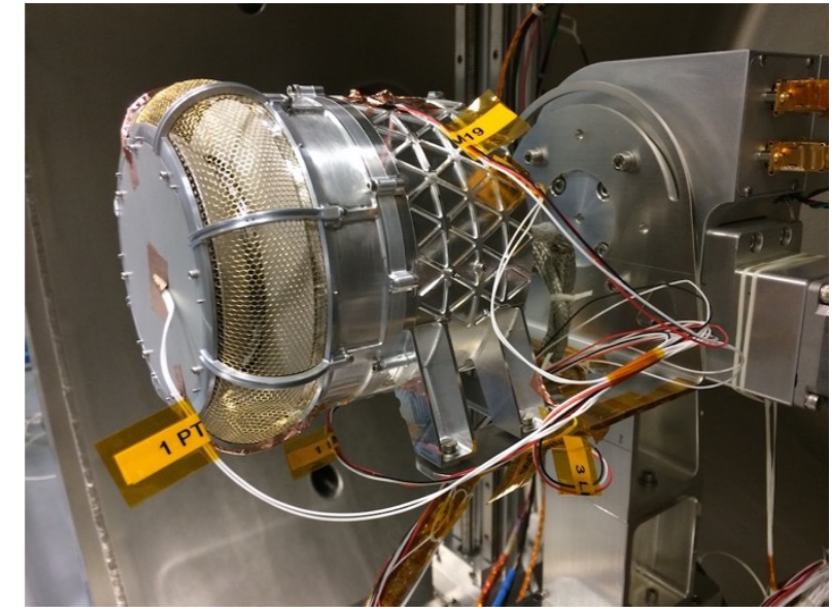
The energy range covered by LEES will be from a few eV up to 1 keV. Particles are measured in 360° azimuth angles with elevation angles ranging from -40° to 70°.

# Comet interceptor / LEES

## FPGA Functional requirements:

- Operate SpaceWire link at 10Mhz
- Handle Data Protocol
- Operate SPI lines for ADCs and DACs
- Compute and Drive Sweeping High Voltages
- Detect Events from the Front End Electronics

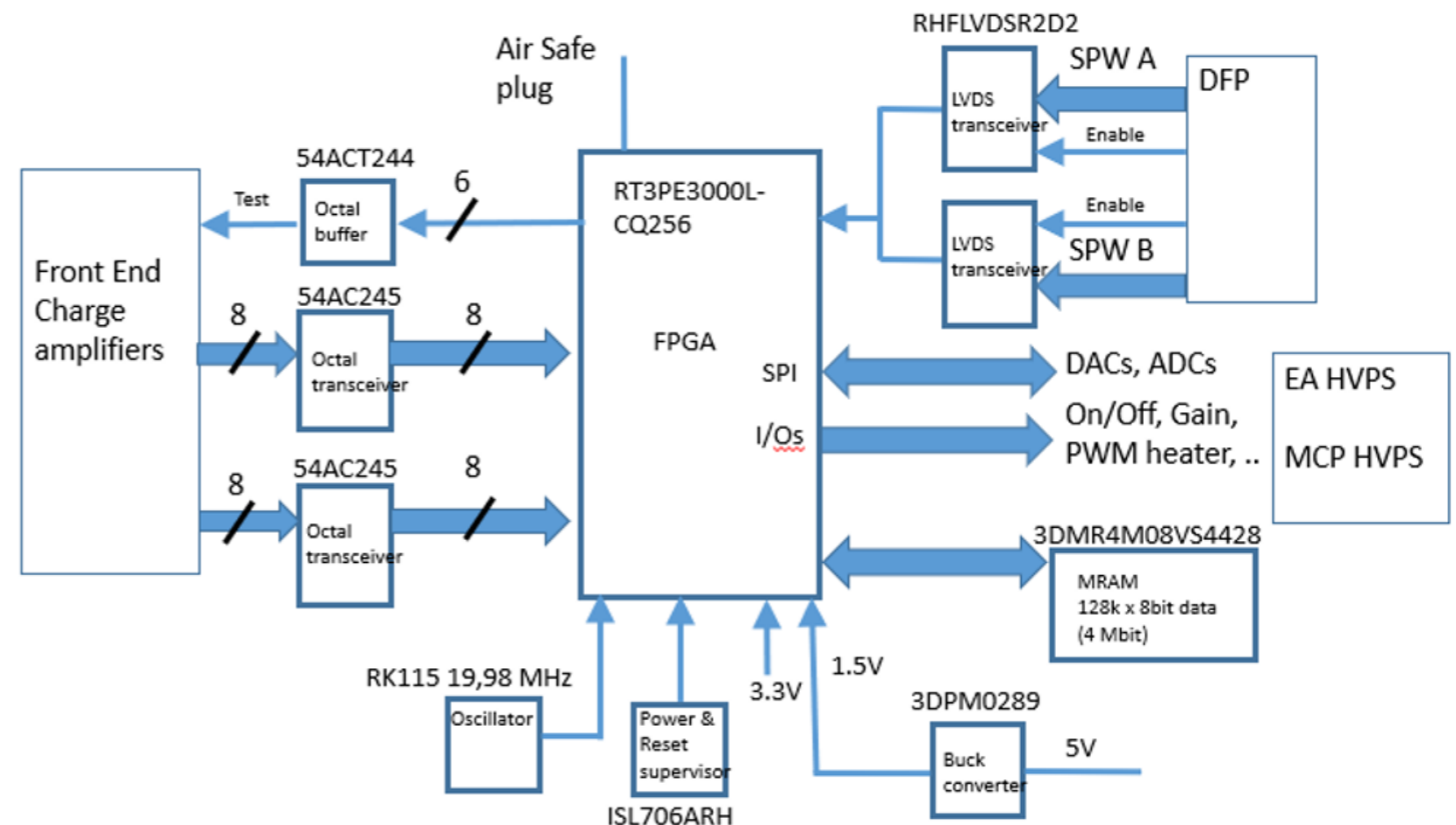
Prototype Instrument in vacuum chamber



EM FPGA BOARD

With Actel Proasic3E A3PE3000 pq208

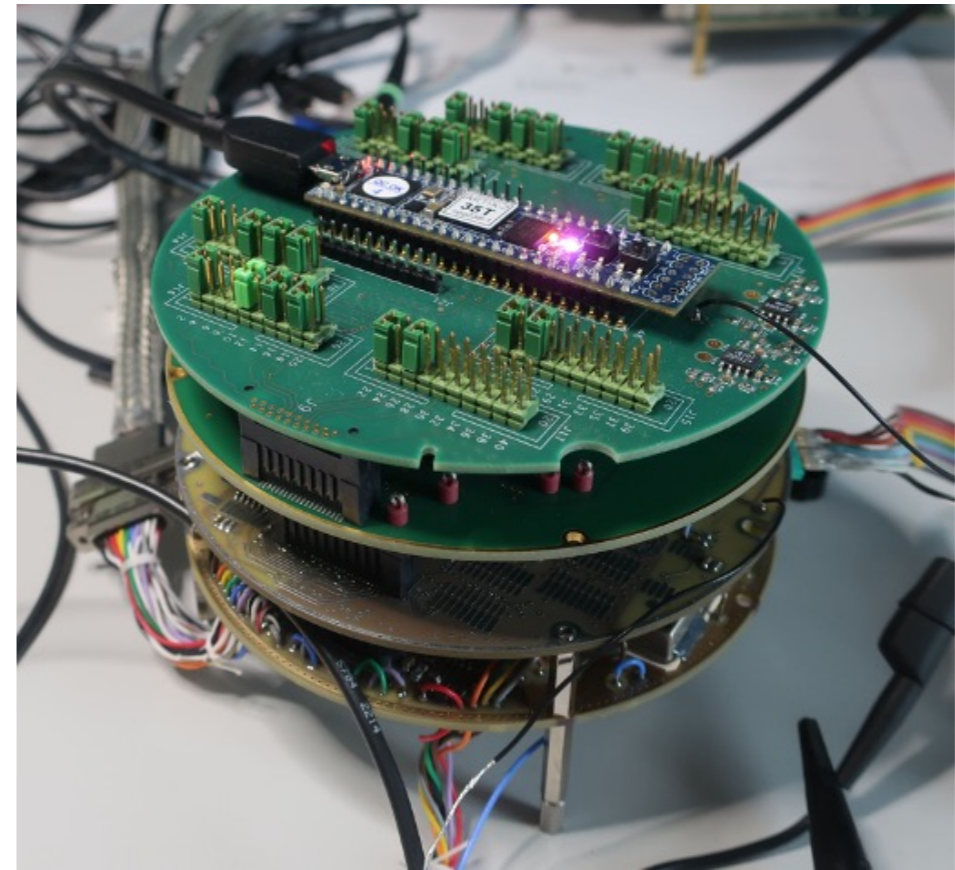
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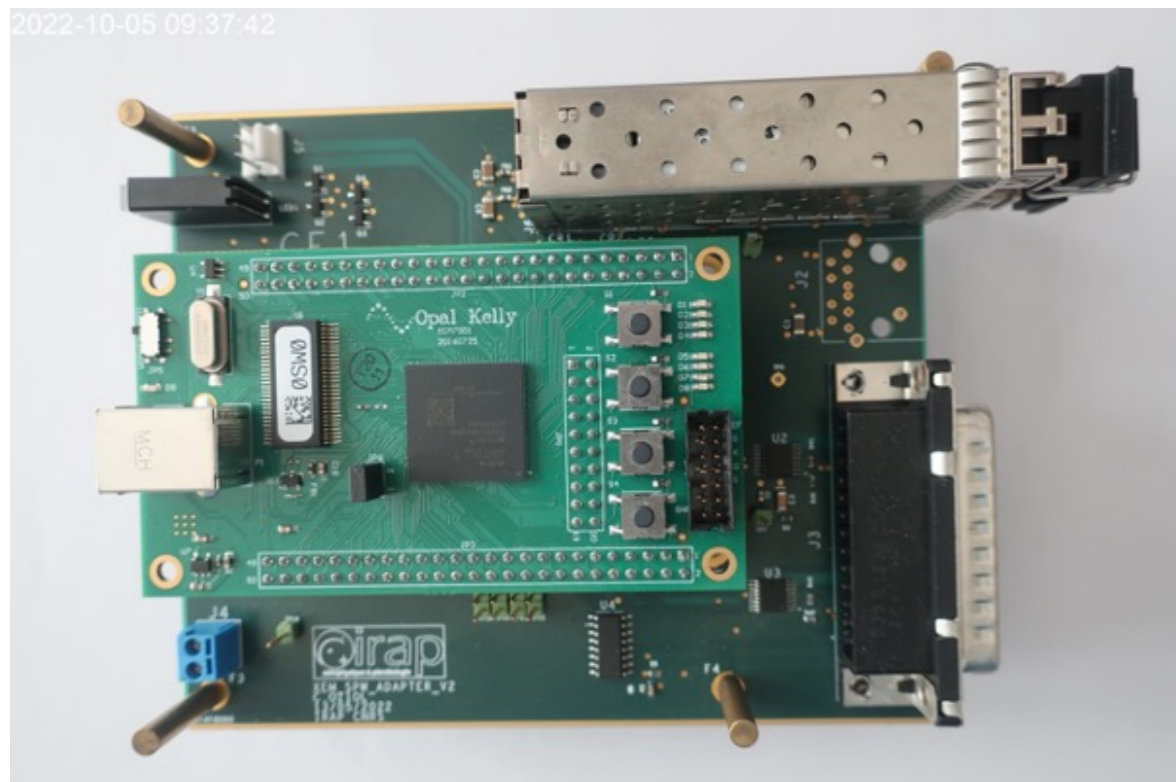
# Comet interceptor / LEES dvp tools

## Software tools

- Microsemi Libero
- Mentor Questasim
- VSCode
- Vivado



FPGA board stacked with HV board and FE event generator



Opal Kelly spacewire adapter with optical fiber interface

## Hardware tools

- Opal kelly board with Xilinx
- Digilent CMOD A7
- Star dundee spacewire analyser

# Conclusion

	FPGA	Frequency	Resources occupation
<b>SVOM / Eclairs</b>	NG-Medium	10 MHz	44 %
<b>DORN</b>	NG-Medium ( FUSIO )	100 MHz	81 % ( !! )
<b>Litebird</b>	NG-Ultra	600 MHz ( R52 ) 200 MHz ( FPGA, TBC )	TBD
<b>Comet interceptor</b>	RT3PE	10 MHz	TBD ( > 20 % )

Current FPGAs described in these slides have been performant enough to provide solutions for scientific instruments development.

We are now excited to be able to work on developments using NG-Ultra SOC and XStratum Hypervisor ( Litebird project ).