Airbus Crisa

Verification Strategy of Multi-FPGA Systems

I. Hidalgo, A. Carballo, J. Cerro, J.A. Ortega

CRISA

Isabel Hidalgo

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Airbus Crisa: Airbus Defence and Space Location Tres Cantos

- **For more than 36 years, with more than 2000 flight units delivered, Airbus Crisa has contributed to most of the European Space Agency (ESA) programs**
- Airbus Crisa in Tres Cantos employs about 600 qualified employees.
  - Roadmaps & Experts Team: 12 engineers (AIRBUS Experts , CRISA Experts and Product Portfolio Managers)
  - Microelectronics Team: 30 engineers (> 150 years of accumulated experience in Space microelectronics).

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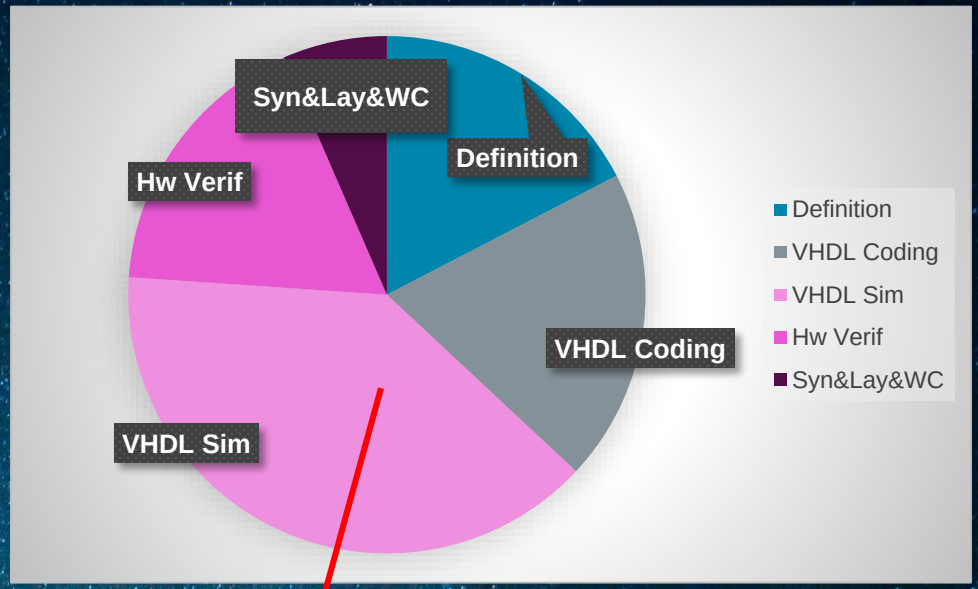
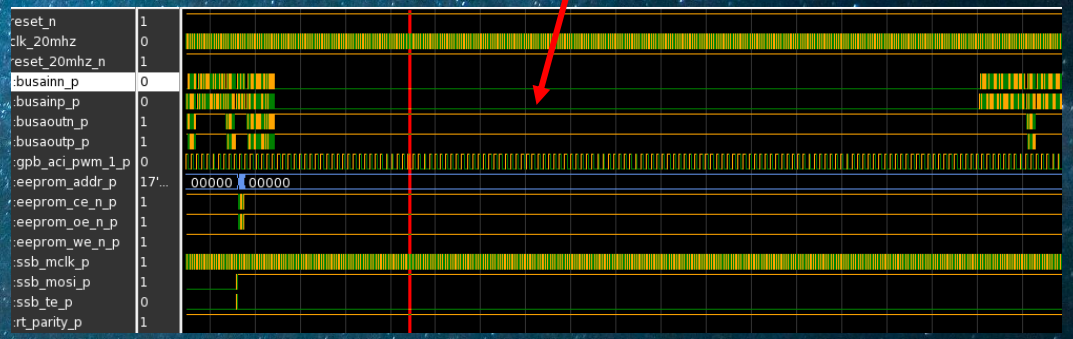
Challenges in current FPGAs verification

- **Verification tasks take > 40% of the FPGA development process**
- **Challenges of the VHDL simulations :**
  - Generate models for external functions with enough representability
  - High effort to cover as many as possible of the system configurations
  - Very long sequences to move FPGA to the operational modes
  - High effort to get functional coverage in systems with high configurability

  - Few **ms** might take minutes or **hours** to simulate (RTAX2000)
  - Full **regression** campaigns take **days** to simulate (RTAX2000)

It is need to speed up simulations and go to HW prototyping as soon as possible or used FPGA prototyping PLATFORMS





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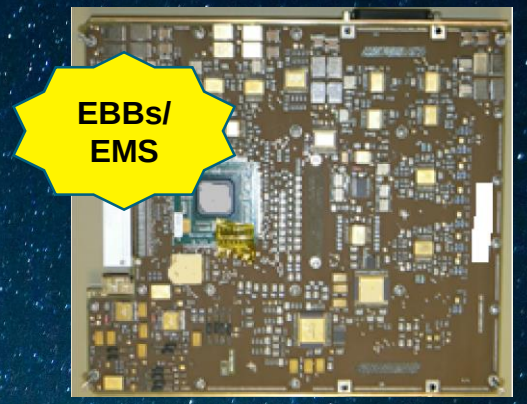
Solutions analyzed to improve FPGAs verification

Solutions analyzed:

- **Reprogrammable FPGAs on Bread Boards or Engineering Models**

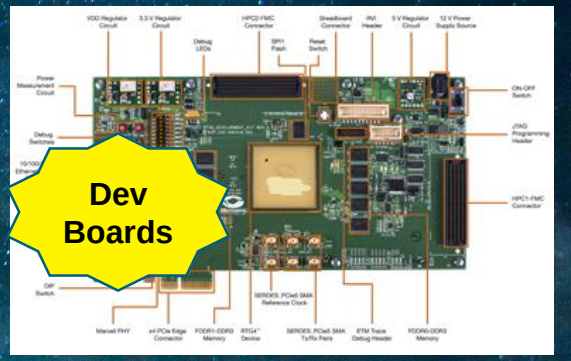
Major advantage is representability (99.99%) but

- Low controllability and observability
- Difficult to force error conditions
- Very difficult to execute random, long or “stress” tests.
- Availability in very LATE stages of the FPGAs development



- **Different families of FPGA Development boards**

  - Medium/High FPGA capability : not enough for Systems with mode that three FPGAs
  - Poor observability and controllability
  - User has to built all the communication with the computer

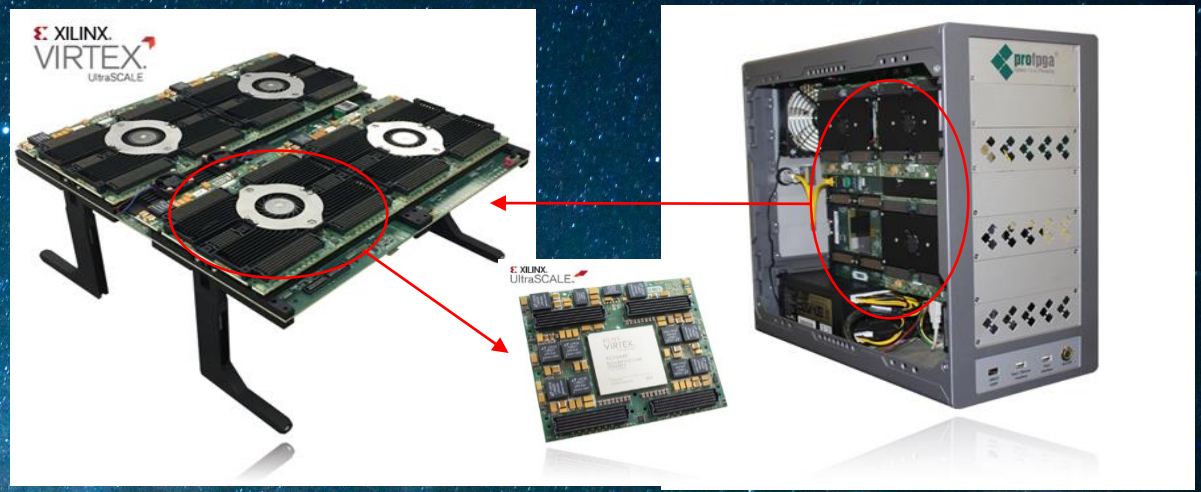


- **FPGA Prototyping Solutions: Siemens EDA Veloce® Emulation line product**

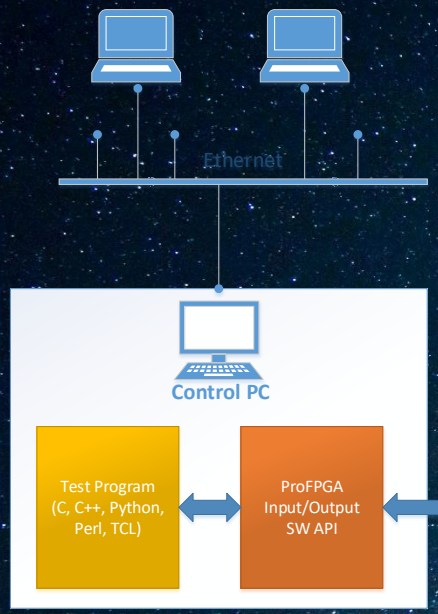
FPGA Prototyping platform: proFPGA

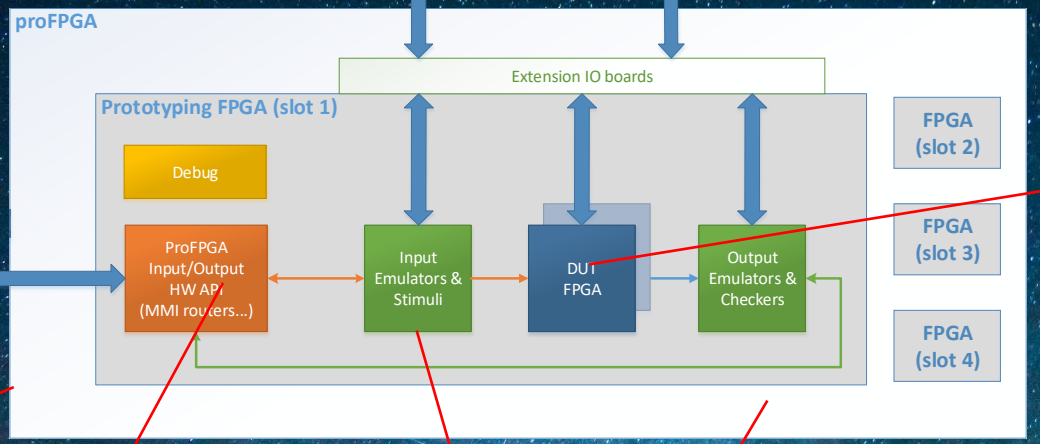
Siemens EDA Veloce™ hardware-assisted verification system for integrated circuits

- **ProFPGA 1 Slot FPGA:**
  - XCVU440 FPGA
    - 30M ASIC gates capacity
    - Internal memory 88,600 kbits
  - 1327 free user I/O
    - Observe signals by 100's
  - Up to 1.0 Gbps single ended (standard I/O)/ up to 12.5 Gbps (MGT) differential
  - 5M CLB Flip-Flops (~500 x RTAX2000)
- **HW API and SW API**
  - Resolved, providing USB/PCIe/Ethernet drivers (Plug and Play)
- **Test programs**
  - Phyton or C
- **Observability and controllability**
  - Connection to Digital Analyzer (monitor up to 96 internal signals)
  - Connection to external HW

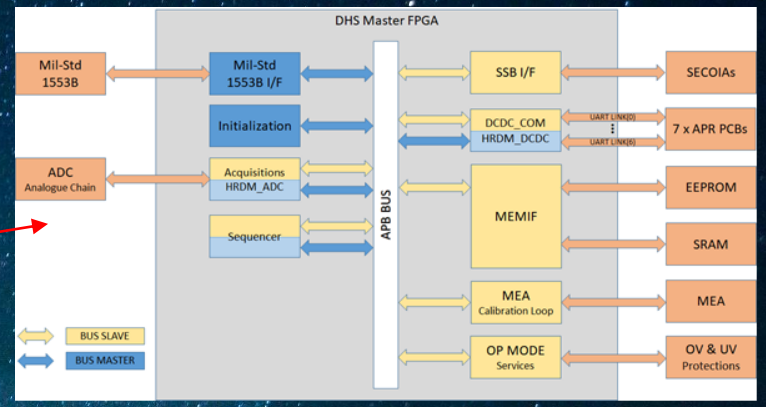


FPGA Prototyping platforms: ProFPGA

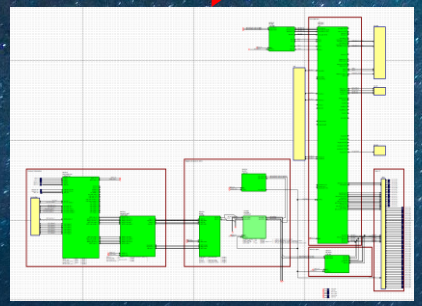


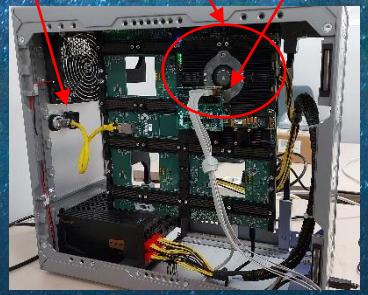


... allows designer be focus on VHDL to prototype and Phyton/C to create test programs



- **MILBUS-1553**
  - Manage Commands reception and telemetry packets
- **EEPROM/SRAM**
  - EEPROM: Drivers configuration
  - SRAM: Store configuration copy and HDRM samples
- **Sequencer:**
  - Manages ON/OFF sequences
- **HRDM: (debugging),**
  - High Rate Data Module for the ADC, DCDC and LCLs telemetries .
  - Asynchronous start and stop(abort)
  - Rate configuration between 100 us and 25.5 ms
  - Trigger delay wrt last command reception
- **Acquisition**
- **DCDC Communication**
  - All structure around APB internal bus





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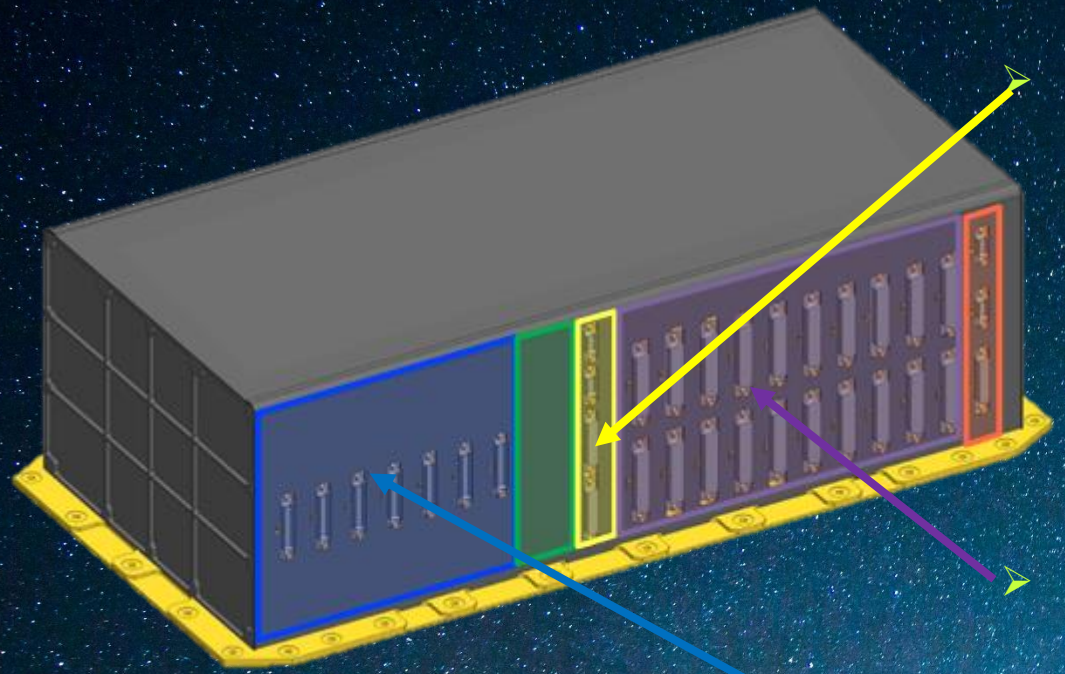
Power System Units with Multiple FPGAs and ASICs



	Board	FPGAs
Yellow	DHS	1 RTAX2000S
Blue	DCDC Converters	21 RTAX250S
Purple	10 LCL	10 ASICs (CRISA SeCOiAs)

- **Data Handling System (DHS FPGA):**
  - Communication Interfaces with platform through MILBUS-1553
  - Control and monitoring > 200 Latching Current Limiters as distributions modules by means of 10 ASICs developed in house (CRISA SECOiAs)
  - Control and monitoring >40 DCDC Converters through a Serial link (UART)
  - Housekeeping analog Telemetries
  - OV and UV Protections
  - High Rate Data Monitoring **(HRDM)** to capture up to 8 TMs channels configured Data rate until complete 2Mbits of data (125 Ksamples)
  - RTAX2000S per DHS Board @ 40 MHz
- **LCL Boards:**
  - Distribution power function
  - 12 LCLs per module
  - 24 drivers per LCL module.
  - 10 ASICs (CRISA SECOiA) per Board @ 10 MHz.
- **DCDC Boards:**
  - Power bus conditioning function.
  - 6 DCDCs converters in each board
  - 3 RTAX250S FPGAs per Board @ 32 MHz

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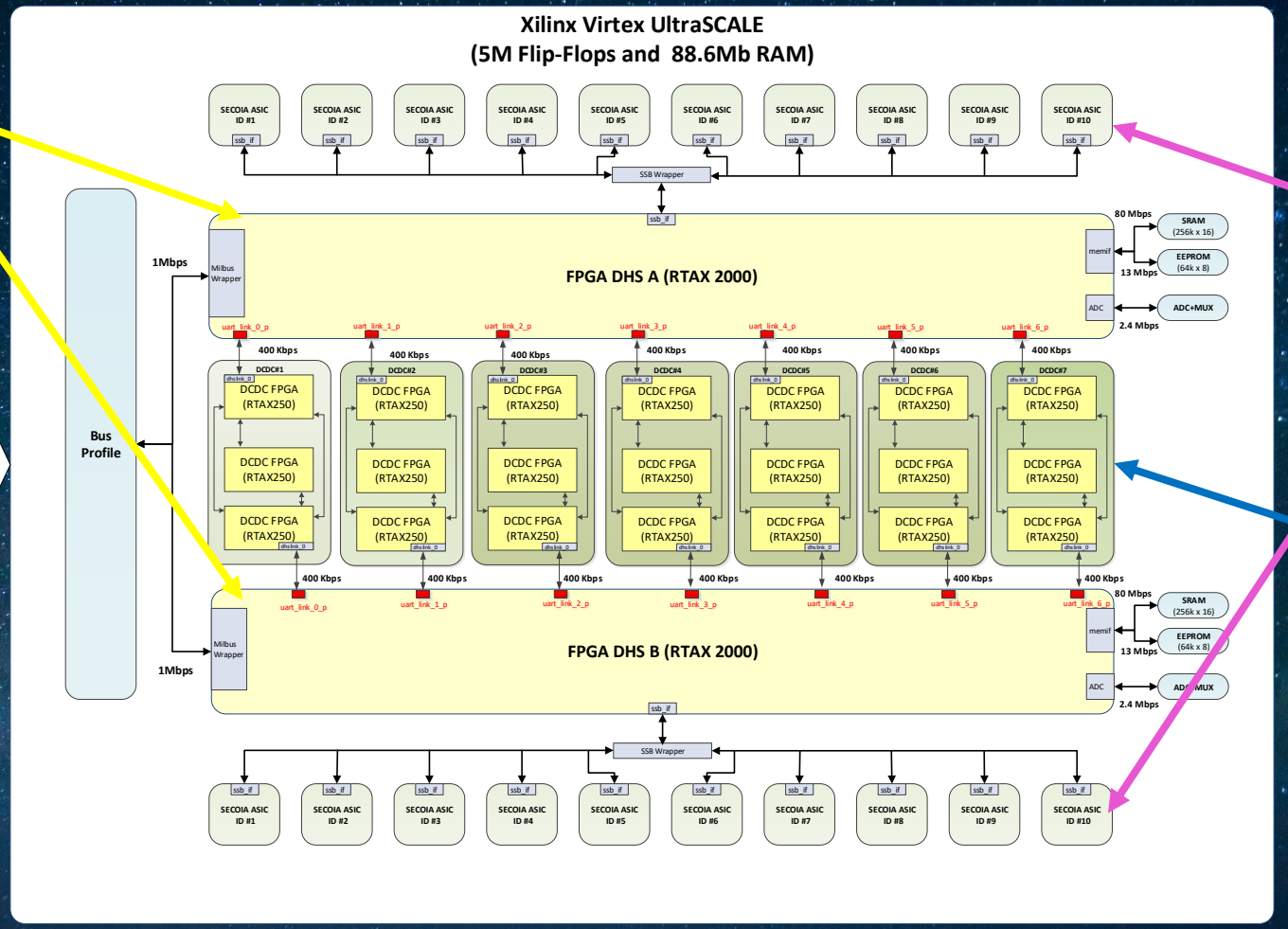
ProFPGA Emulation enviroment for Data Handling System

UP to 43 FPGAS/ASICs connected!!

RTAX2000

2xDHS

USB / PCIe
100Mbps / 3.2Gbps



20xASICs

20 LCL

21xRTAX250

7xDCDC

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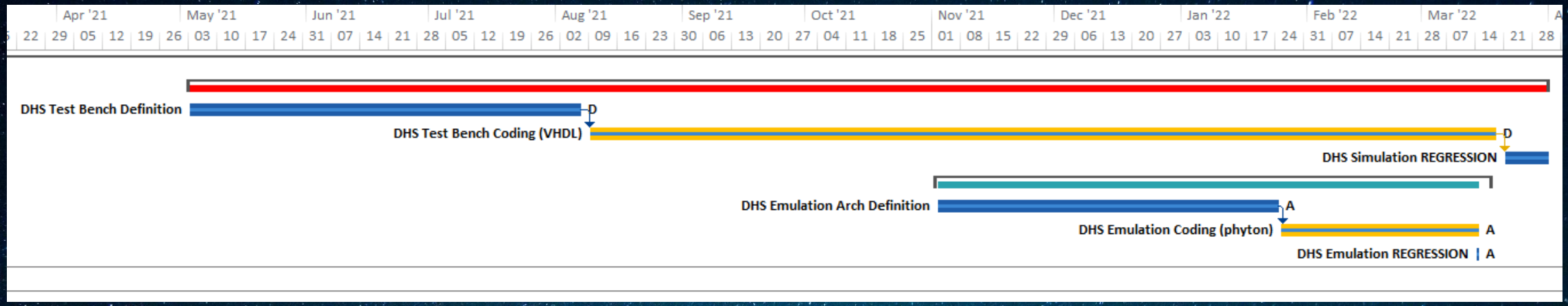
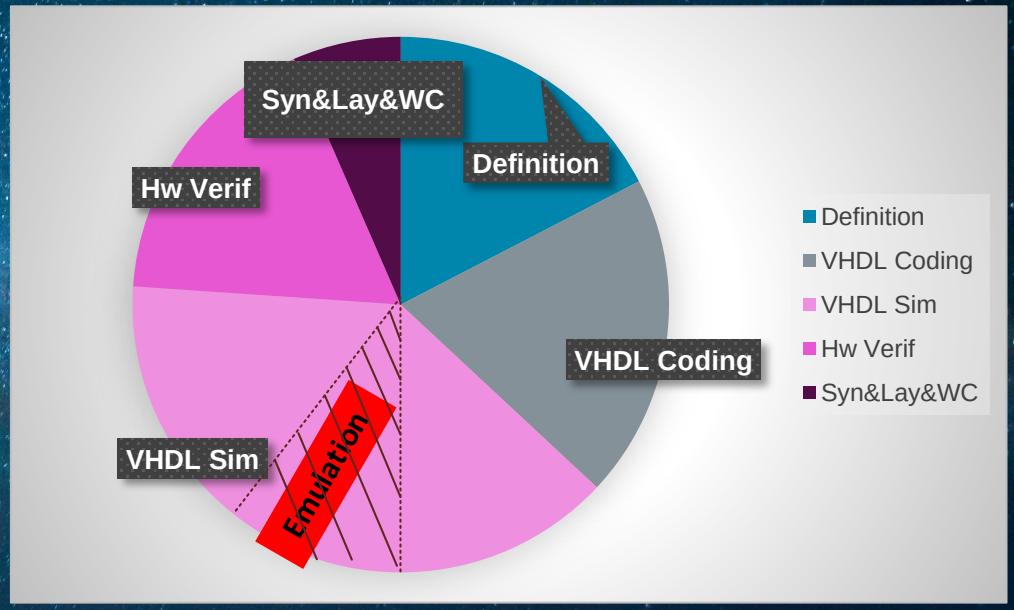
Data Handling System verification development



- **Analysis between Verification and Emulation efforts**
  - Both tasks (Simulation and Emulation) develop by Juniors Engineers
  - Equivalent numbers of "models" to be developed
  - Similar time needed for setup both environments
  - Emulation requires 50% less time for tests coding and execution
  - Significant reduction in regression times (Simulations takes days vs hours for Emulation)

Simulation is still required but

…combined with the EMULATION!!



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Emulation Results for Data Handling System

- **Evaluation results:**

Points analyzed	SIMULATION (VHDL)	EMULATION (proFPGA)	HW Verification (EM)
Telecommands sent	3540	7413	250
Telemetries packet processed (@420x16bits)	195	3700@100ms	450@1sec
Nb. of tests implemented	96	14	40
Longest duration test	467 sec	12 hrs.	--
Asynchronous commands (HDRM)	110	>1000	--
Regression time	90 hrs.	1h 30min	2 wks.

- **Early problem detection**
  - DCDC interconnection: Wrong addressing when multiple DCDC lines send data.
  - Lost of Debug Telemetry : HRDM doesn't start properly after abort in DCDC acquisition.
  - Lost of House-Keeping Telemetry: HRDM fails when starting from HK in ADC acquisition.

Power Unit System in Emulation enviroment

- **Conclusions**
  - The use HW emulation system for complex FPGAs or system with multiple FPGAs:
    - anticipating to integration errors,
    - increasing functional coverage,
    - speeding up verification,
    - and ensuring functionality, robustness and quality of the FPGA and the system
- **Next steps**
  - Prototyping in projects with complex FPGAs and FPGAs including microprocessors (IP or silicon)
  - proFPGA- Improve bus communication protocols
    - AXI through FPGA
    - Ethernet as API
    - Use Extensions boards for SDRAM, MRMA, NOR Flash memories

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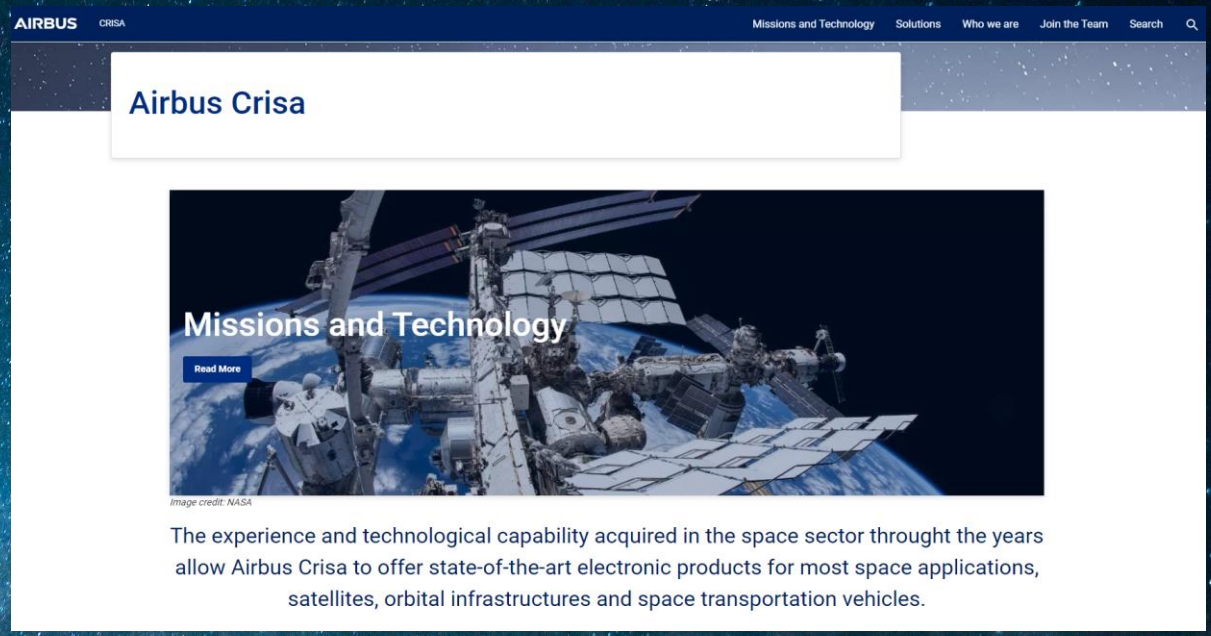
Thank you!



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