Universidade Federal do Rio Grande do Sul, Brazil
Graduate Program in Microelectronics
www.ufrgs.br/pgmicro

Enhancements on Fault Injection for Xilinx 7 Series and UltraScale+ SRAM-Based FPGAs

Fabio Benevenuti, Fernanda Lima Kastensmidt

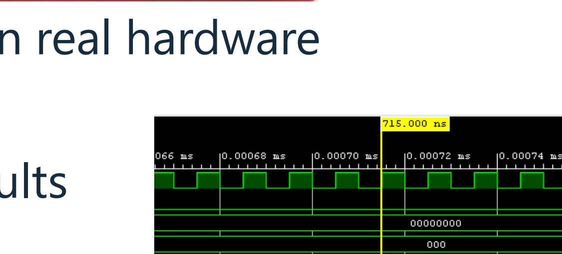
5th SEFUW
SpacE FPGA Users Workshop
March 2023, ESTEC, Noordwijk, The Netherlands

Content

- Reliability and fault injection
- Investigation on Xilinx 7 Series & UltraScale+
- Improvements on UFRGS fault injector

Motivation

- Physical fault injection
  - Real hardware
  - Radioactive sources, particle accelerators, laser
  - Costly facilities, controlled environment
- Emulation-based fault injection
  - Real hardware, but exploiting test & configuration circuitry to manipulate device and emulate radiation effects
    - ❑ JTAG, SelectMAP, PCAP, ICAP, ...
  - Lower cost, no complex facilities
  - May be focused on modules of interest
  - Application running near or at nominal speed in real hardware



- Simulation-based fault injection
  - Hardware or circuit models used to simulate faults
  - Detailed observations
  - Available on early stages of engineering, even before real hardware existence
  - Possibly the lower cost (mostly software), but also the slower

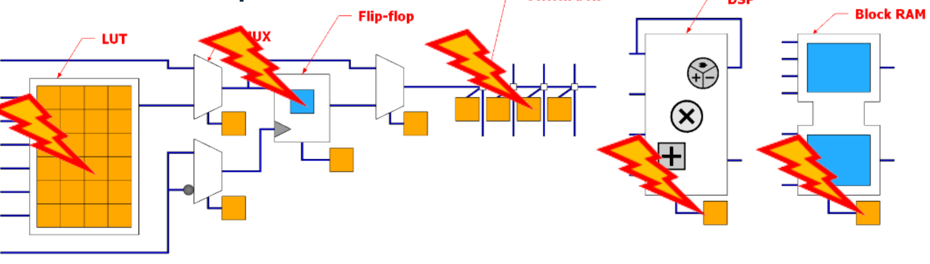
Motivation

- Physical fault injection
  - Real hardware
  - Radioactive sources, particle accelerators, laser
  - Costly facilities, controlled environment
- Emulation-based fault injection
  - Real hardware, but exploiting test & configuration circuitry to manipulate device and emulate radiation effects
    - JTAG, SelectMAP, PCAP, **ICAP**, ...
  - Lower cost, no complex facilities
  - May be focused on modules of interest
  - Application running near or at nominal speed in real hardware
- Simulation-based fault injection
  - Hardware or circuit models used to simulate faults
  - Detailed observations
  - Available on early stages of engineering, even before real hardware existence
  - Possibly the lower cost (mostly software), but also the slower

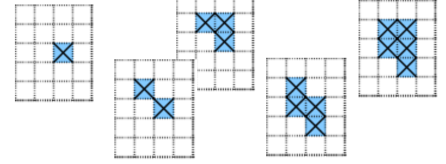
Reliability & Fault Injection

Fault space

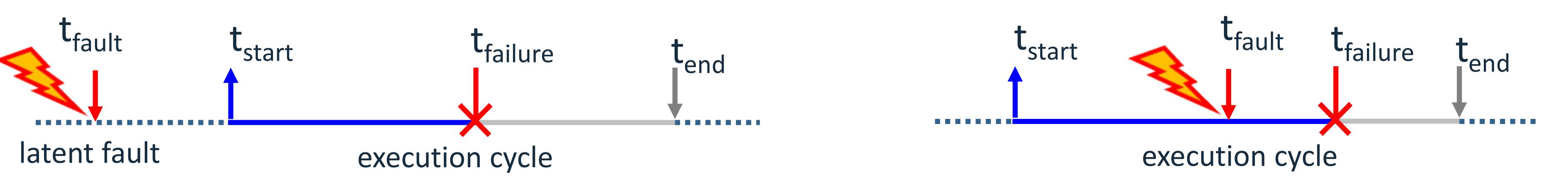
- Fault location: where
  - User/Application data: BRAM, flip-flips, LUTRAM/shift-registers,...
  - Configuration memory: LUT equation, DSP opmode, INT/PIP switchbox routing,...



- Fault type: emulated effect
  - Single bit-flip (SBU-SEU), multiple bit-flips (MBU-SEU)

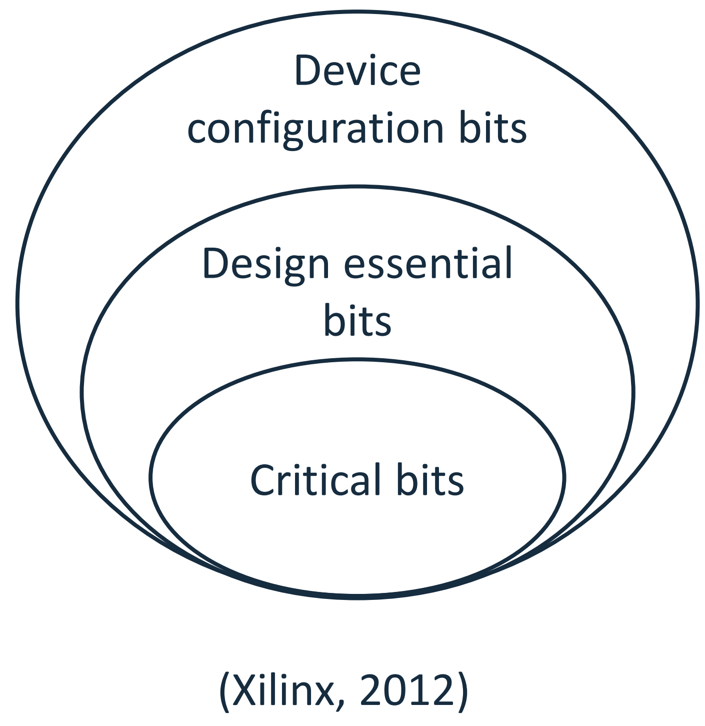


- Fault time: when
  - Important for dynamic data (BRAM, flip-flop), subject to temporal masking
  - Also important for CRAM when memory scrubbing is active
  - Less important for persistent data (CRAM) without scrubbing



Qualification metrics

- Essential and critical bits
  - Captures only a static behavior of the design
  - There special conditions where non-essential bit may become a critical bit



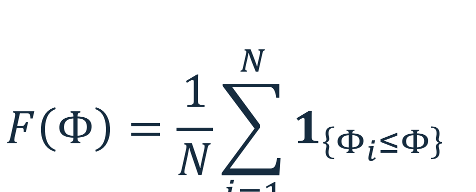
(Xilinx, 2012)

Qualification metrics

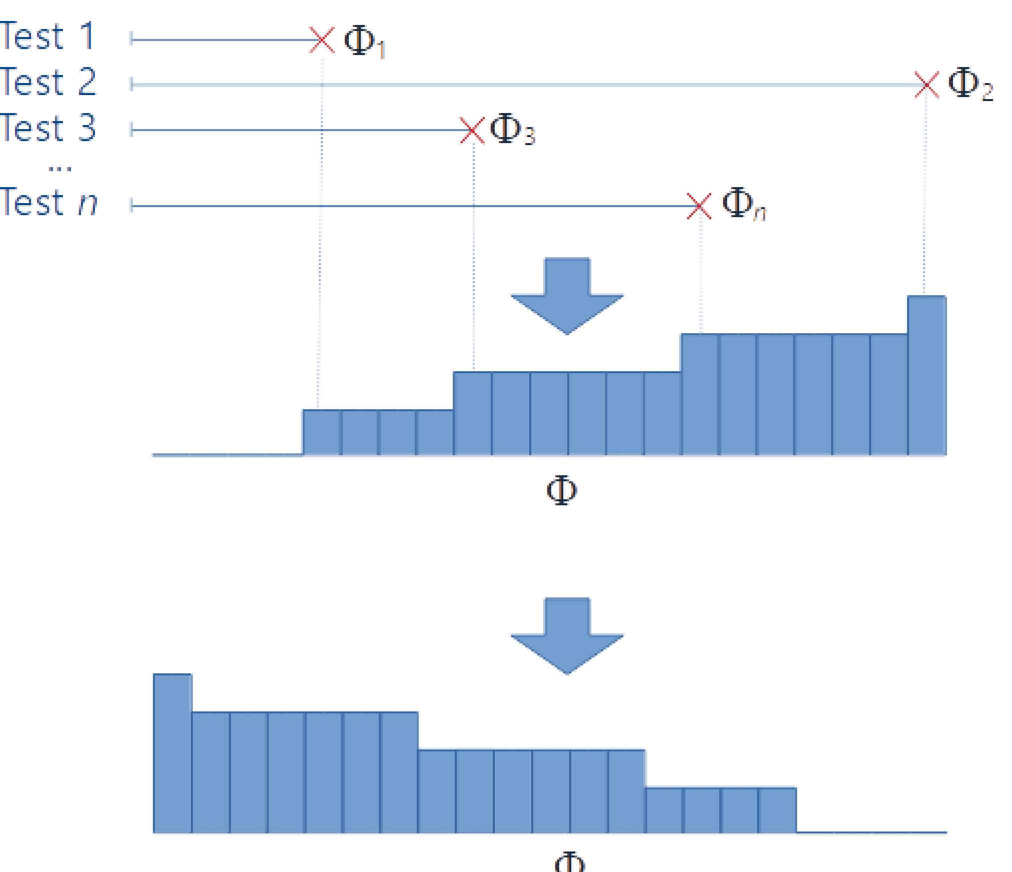
- AVF, architectural vulnerability factor
  - May require extensive scan of the whole processing cycle to describe AVF in terms of sensitive surface over residency time
- Mean metrics, single-point statistics
  - Cross-section, Mean time between failure (MTBF): not good for comparison in the presence of mitigations/redundancy (TMR)
  - Mean execution between failure (MEBF), Mean workload between failure (MWBF): not good for comparison when design bellow 100% duty cycle
- Reliability curves, mission time
  - Captures the dynamic and cumulative effect over time
  - Allows for focusing on the high-reliability zone (experiment truncation/censoring)
  - Allows for extraction of mean metrics
  - Allows cross-validation between radiation and emulated fault injection

Reliability curves

- Accumulate faults (or fluence) until failure (or until limit of interest)
  - Collect a number N of events, recording time t, fluence Φ or number of accumulated faults for each event



$$F(\Phi) = \frac{1}{N}\sum_{i=1}^{N} \mathbf{1}_{\{\Phi_i \leq \Phi\}}$$



$$R(\Phi) = 1 - F(\Phi)$$

Fault injectors for Xilinx FPGAs

- Not an exhaustive list

Cumulative, R curve

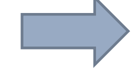
Fault Injector	Data manipulation	Target device	Access interface
Antoni et al. (2000)	Modifies bitstream file before loading in FPGA. Bitstream may be 1 single frame.	Xilinx Virtex	JTAG/ MultiLINX
Johnson et al. (2003)		Xilinx Virtex	JTAG/ MultiLINX
Aldeghiri et al. (2007) FLIPPER	Uses one device/FPGA to manipulate bitstream inside the target FPGA.	Xilinx Virtex-II	SelectMAP/ JTAG
Napoles et al. (2007) FT-UNSHADES		Xilinx Virtex-II	SelectMAP
Mogollon et al. (2011) FT-UNSHADES2		Xilinx Virtex-5	SelectMAP
Aldeghiri et al. (2014) FLIPPER2		Xilinx Virtex-4	SelectMAP/ JTAG
Hardward et al. (2015) BYU XRTC-V5FI		Xilinx Virtex-5	SelectMAP
Thurlow et al. (2019) BYU TURTLE		Xilinx 7 Series	JTAG

Fault injectors for Xilinx FPGAs

- Not an exhaustive list

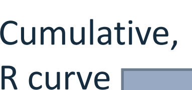
Sampling for critical bits

MBU



Complete list of critical bits

Cumulative, R curve



Fault Injector	Data manipulation	Target device	Access interface
Sterpone et al. (2007)	Instrumented design, modifies bitstream from within FPGA.	Xilinx Virtex-II	ICAP
Nazar et al. (2012) UFRGS		Xilinx Virtex-5	ICAP
Tarrillo et al. (2015) UFRGS	Replays SEUs database collected from radiation experiment.	Xilinx Virtex-5	ICAP
Leipnitz et al. (2016) UFRGS	High speed fault injetion controller through PCI-Express interface.	Xilinx Virtex-5	ICAP
Nunes et al. (2015) FIRED	Instrumented design, modifies bitstream from within FPGA.	Xilinx Virtex-5	ICAP
Villalta et al. (2014)	Modifies bitstream from Arm Cortex-A software using processador access port.	Xilinx Zynq-7000	PCAP
Tonfat et al. (2016) UFRGS	Exhaustive scan for critical bits.	Xilinx Artix-7	ICAP
Gomes-Cornejo et al. (2017)	Modifies BRAM content from Arm Cortex-A software using processador access port.	Xilinx Zynq-7000	PCAP
Bozzoli et al. (2018) PyXEL	Produces bitstream file variants emulating SEU effect.	Xilinx 7 Series	SelectMAP/ JTAG
This work UFRGS	Cumulative fault injection, SBU+MBU, coexistence with scrubbing.	Xilinx 7 Series & UltraScale+	ICAP

Understanding
Xilinx 7 Series & UltraScale+

Investigation on Xilinx FPGAs

		Techniques	ICAP	Laser	Radiation
		Facilities	UFRGS PGMICRO	ies l'institut d'électronique	IEAv / IFUSP Instituto de Física da USP
Circuits and applications	High level	Reliability of the integrated system			
		Integration tests at SoC level (FPGA + Arm Cortex)			
		Integration tests of Xilinx reusable AMBA AXI/AXI-S soft IPs			
	Low level	Reliability tests of specific design blocks/modules			
		Qualification of mitigation techniques			
		Test on basic reconfigurable elements CLB/DSP/BRAM			
		Characterization of Xilinx modular device floorplan (ASMBL level)			microbeam

Investigation on Xilinx FPGAs

		Techniques	ICAP	Laser	Radiation
		Facilities	UFRGS PGMICRO	ies l'institut d'électronique	IEAv, IFUSP Instituto de Física da USP
Circuits and applications	High level	Reliability of the integrated system			
		Integration tests at SoC level (FPGA + Arm Cortex)			
		Integration tests of Xilinx reusable AMBA AXI/AXI-S soft IPs			
	Low level	Reliability tests of specific design blocks/modules			
		Qualification of mitigation techniques			
		Test on basic reconfigurable elements CLB/DSP/BRAM			
		Characterization of Xilinx modular device floorplan (ASMBL level)			

static tests

Investigation on Xilinx FPGAs

			ICAP	Laser	Radiation
		Techniques			
		Facilities	UFRGS PGMICRO	ies l'institut d'électronique	IEAv IFUSP Instituto de Física da USP
Circuits and applications	High level	Reliability of the integrated system			
		Integration tests at SoC level (FPGA + Arm Cortex)			
		Integration tests of Xilinx reusable AMBA AXI/AXI-S soft IPs			
	Low level	Reliability tests of specific design blocks/modules			
		Qualification of mitigation techniques			
		Test on basic reconfigurable elements CLB/DSP/BRAM			
		Characterization of Xilinx modular device floorplan (ASMBL level)			

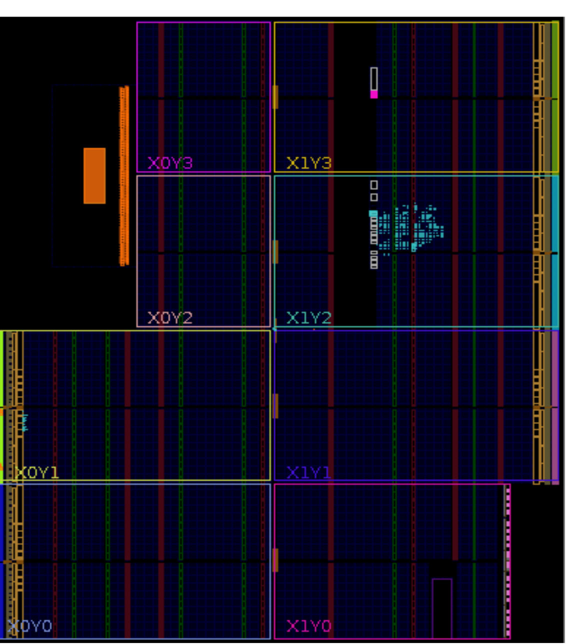
dyn. tests

Floorplan reachable by fault injector

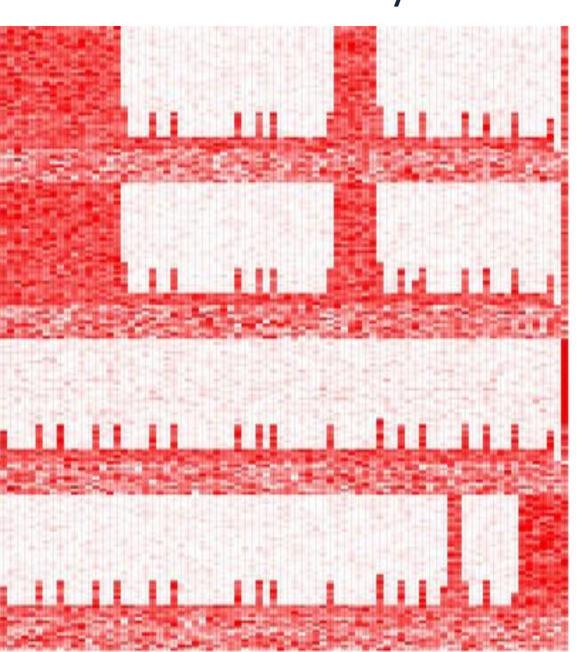
- Example Zynq-7000 XC7Z030

Physical Device
IR Imaging

Vivado Logical
Floorplan



Fault Injector
Reachability



Floorplan reachable by fault injector

- Example Zynq-7000 XC7Z030

Physical Device IR Imaging

Arm Cortex-A9 Processing System (PS)

7 Series FPGA (PL)

Vivado Logical Floorplan

X0Y3 X1Y3 X0Y2 X1Y2 X0Y1 X1Y1 X0Y0 X1Y0

Fault Injector Reachability

ARM Cortex

ADC, ICAP, BSCAN, …

PCI Express

Gigabit I/O

7 Series laser cartography

- Two ROIs, less then 0.02 mm^2

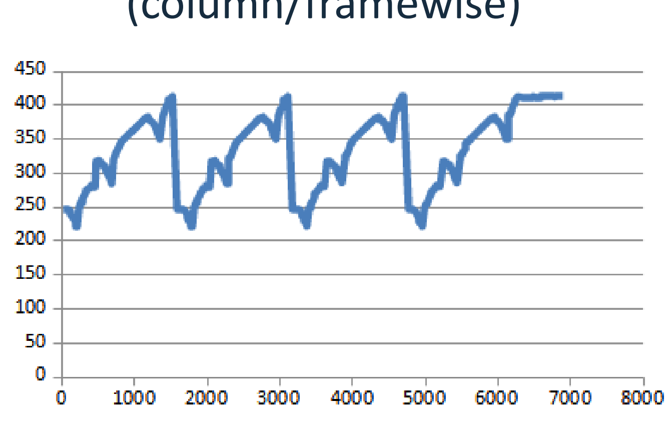
- Laser energies 300pJ and 220 pJ
- Laser shot each ~4 s, readback each ~16 s
- Step ~1 µm horizontal, 5 µm vertical

7 Series laser cartography

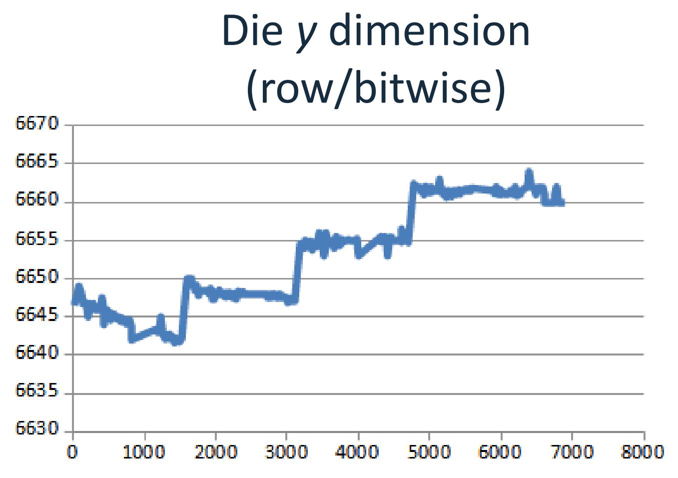
- Each color a different readback file
  - Run 1
  - Run 2

- Time/position of artifacts

Die *x* dimension
(column/framewise)



Die *y* dimension
(row/bitwise)



7 Series laser cartography

- Each color a different readback file
  - Run 1
  - Run 2
- Time/position of artifacts

Frame grows upward

Die *x* dimension (column/framewise)

450
400
350
300
250
200
150
100
50
0

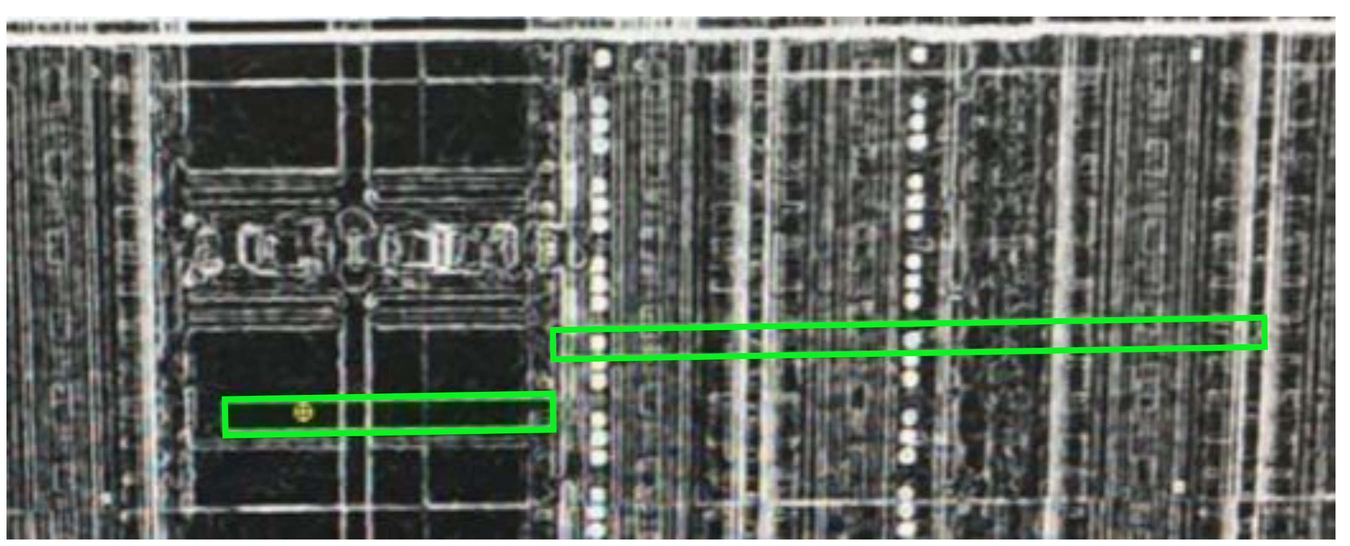
0 1000 2000 3000 4000 5000 6000 7000 8000

Die *y* dimension (row/bitwise)

6660
6655
6650
6645
6640
6635
6630

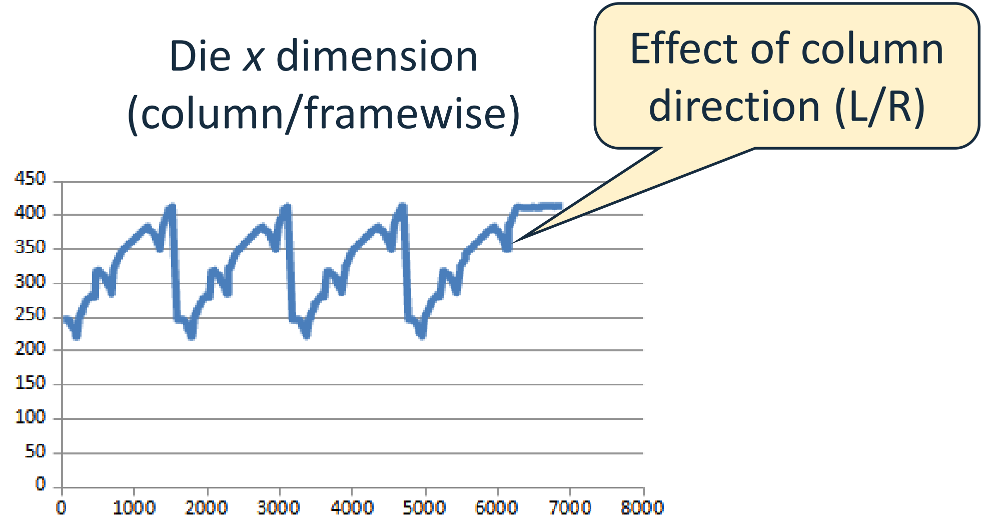
0 1000 2000 3000 4000 5000 6000 7000 8000

7 Series laser cartography

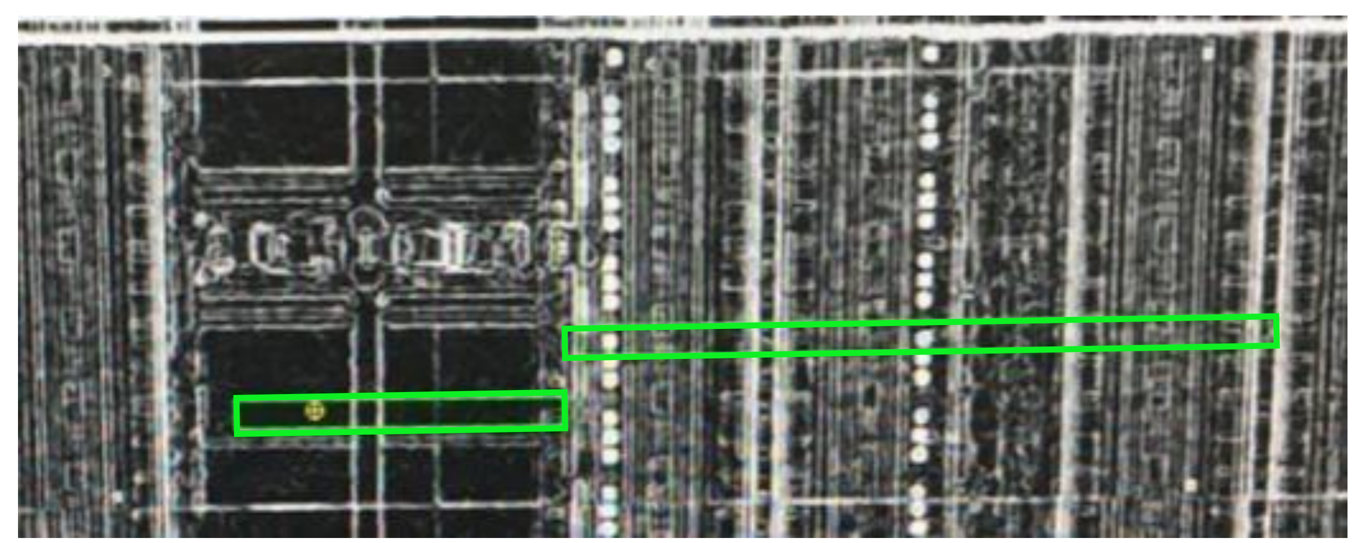


- Time/position of artifacts

Die *x* dimension (column/framewise)



7 Series laser cartography



- Time/position of artifacts

Die *x* dimension (column/framewise)

Adjusted alignment

Die *x* dimension (column/framewise)

450
400
350
300
250
200
150
100
50
0

0 1000 2000 3000 4000 5000 6000 7000 8000

450
400
350
300
250
200
150
100
50
0

0 1000 2000 3000 4000 5000 6000 7000 8000

7 Series static tests

100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%

1 bit-flip
2 bit-flips
3 bit-flips
4 bit-flips
>4 bit-flips
Single-bit SEU
Multiple-bit SEU

- α Particles LAFN USP 241Am
- Heavy Ions LAFN USP 13.1 to 87.5 MeV 7Li to 63Cu
- Neutron 14.1 MeV LRI IEAv Front-side (0°)
- Neutron 14.1 MeV LRI IEAv Back-side (180°)
- Neutron (Epi-)Thermal TENIS ILL 2021 July

7 Series static tests

SBU and MBU distribution α & Heavy Ions

100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%

0,7 1,0 2,9 3,1 3,6 3,7 3,9 4,0 4,1 4,2 4,3 4,4 4,8 4,9 5,1 5,2 5,5 6,0 6,3 6,6 6,8 6,9 7,1 8,1 8,5

LET

CRAM 1-1-1 CRAM 2-2-2 BRAM 1-1-1 BRAM 2-1-2 CRAM 2-1-2

7 Series static tests

Type of memory	Type of SEU	Examples	α Particles	Heavy ions	Neutrons		
					14 MeV 0°	14 MeV 180°	(Epi)Thermal
BRAM	SBU 1-1-1		100.0%	82.0%	93.4%	97.1%	95.4%
	MBU 2-1-2		—	16.2%	4.7%	2.9%	—
	MBU 1-2-2		—	—	—	—	4.5%
	Others		—	1.8%	1.9%	—	0.1%
CRAM	SBU 1-1-1		97.6%	38.1%	76.7%	79.9%	78.1%
	MBU 2-2-2		2.4%	41.9%	16.9%	15.5%	0.0%
	MBU 2-1-2		0.0%	4.4%	3.5%	2.1%	0.0%
	MBU 1-2-2		—	—	0.3%	1.5%	17.8%
	MBU 2-2-3		—	3.0%	1.3%	0.5%	0.0%
	MBU 2-2-4		—	0.2%	—	0.5%	—
	MBU 2-3-4		—	8.3%	0.6%	—	0.0%
	MBU 2-3-5		—	0.6%	0.3%	—	0.0%
	Others		—	3.4%	0.3%	—	4.1%

7 Series static tests

Type of memory	Type of SEU	Examples	α Particles	Heavy ions	Neutrons		
					14 MeV 0°	14 MeV 180°	(Epi)Thermal
BRAM	SBU 1-1-1		100.0%	82.0%	93.4%	97.1%	95.4%
	MBU 2-1-2		—	16.2%	4.7%	2.9%	—
	MBU 1-2-2		—	—	—	—	4.5%
	Others		—	1.8%	1.9%	—	0.1%
CRAM	SBU 1-1-1		97.6%	38.1%	76.7%	79.9%	78.1%
	MBU 2-2-2		2.4%	41.9%	16.9%	15.5%	0.0%
	MBU 2-1-2		0.0%	4.4%	3.5%	2.1%	0.0%
	MBU 1-2-2		—	—	0.3%	1.5%	17.8%
	MBU 2-2-3		—	3.0%	1.3%	0.5%	0.0%
	MBU 2-2-4		—	0.2%	—	0.5%	—
	MBU 2-3-4		—	8.3%	0.6%	—	0.0%
	MBU 2-3-5		—	0.6%			0%
	Others		—	3.4%	0.3%	—	4.1%

Challenge to scrubber

UltraScale+ (16 nm FinFET)

- Main changes in floorplan
  - Same number of LUTs and flip-flops in a CLB, but now all in one slice instead of two
  - Floorplan simplification
  - Switch box columns are now independent from CLB/DSP/BRAM logic
  - There is no more the concept of TOP and BOTTOM rows
  - New layout of BRAM bits (sliced in 256 frames instead of 128)

- Since UltraScale (20 nm planar)
  - More interleaving on CRAM: aggressive reduction of intraframe MBU
    - Positive impact of scrubbing

UltraScale+ (16 nm FinFET)

7 Series

CLB | Interface | Switch box | Switch box | Interface | CLB

CENTER_INTER_L

CENTER_INTER_R

CLB column with 36 frames

CLB column with 36 frames

UltraScale+ (16 nm FinFET)

UltraScale+

CLB

Switch box

CLB

CLB column with 16 frames

Switch box column with 76 frames

CLB column with 16 frames

Enhancements on UFRGS Fault Injector

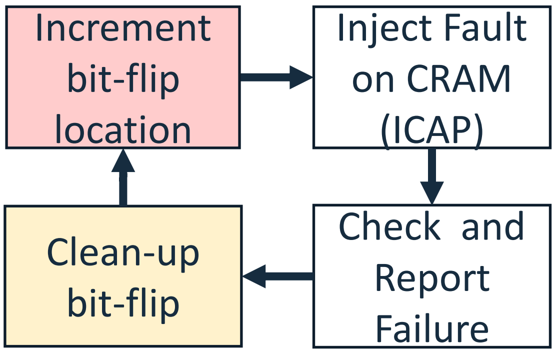
Random-Accumulated Fault Injection

- Emulate cumulative effect of SEUs
  - Build a reliability curve (CDF) similar to obtained from radiation
- Accelerate fault injection campaign

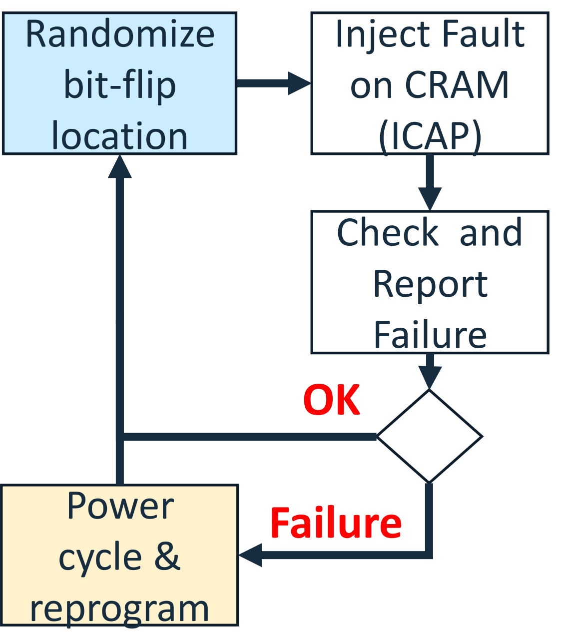
Random-Accumulated Fault Injection

- Emulate cumulative effect of SEUs
  - Build a reliability curve (CDF) similar to obtained from radiation
- Accelerate fault injection campaign

Tonfat et al. (2016)
7 Series



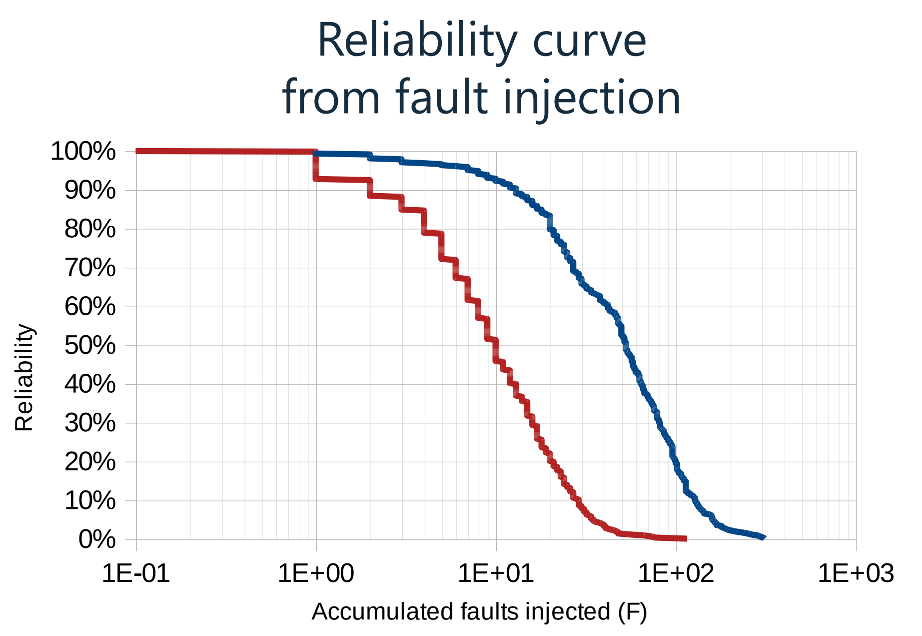
Cumulative process
7 Series & UltraScale+



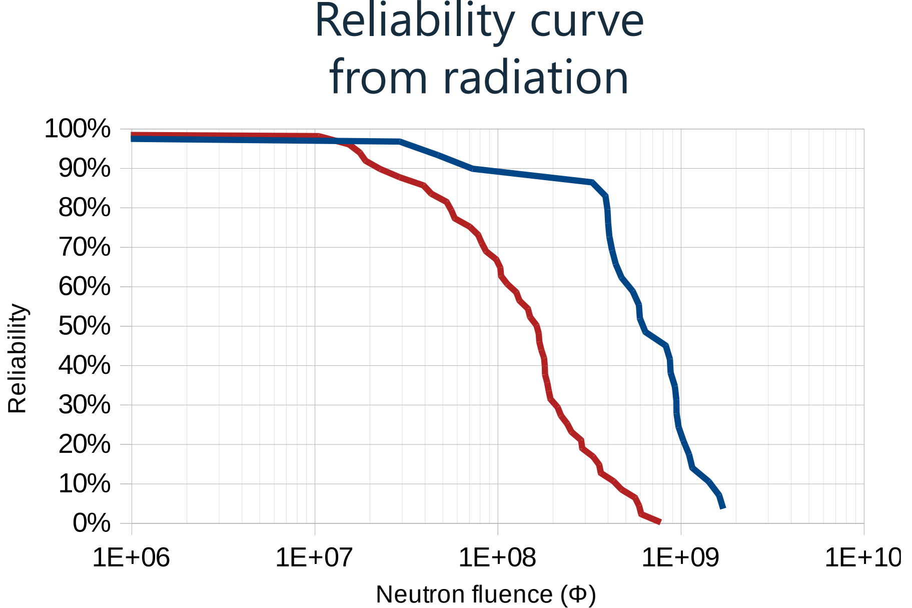
Random-Accumulated Fault Injection

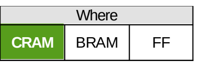
- Test results for two implementations of *study-case CNN* for aerial image classification (RADECS 2021)

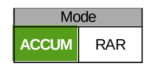
Reliability curve from fault injection

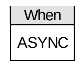


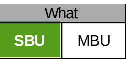
Reliability curve from radiation



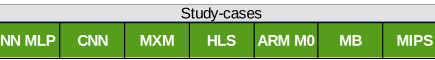








What: SBU | MBU



Mitigations: SCRUB | HAMM | SIHFT | CGTMR | FGTMR

Random-Accumulated Fault Injection

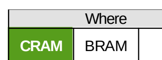
- An estimate on the number of critical bits can still be obtained with random-accumulated methodology
  - R(t=1) ~ Nazar et al. (2012) random sampling

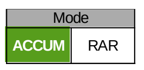
Reliability

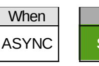
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%

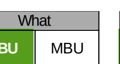
1E-01 1E+00 1E+01 1E+02 1E+03

Accumulated faults injected (F)









Random-Accumulated Fault Injection

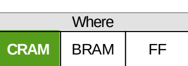
- Test results for different blocks of a *study-case MLP* (SBCCI 2018)

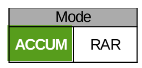
180,000
160,000
140,000
120,000
100,000
80,000
60,000
40,000
20,000
0

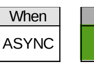
■ Observed critical bits from exhaustive FI (5.9 days)
■ Estimated critical bits from random FI (3.7 hours)

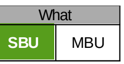
C2 P2 C3 P3 Whole MLP

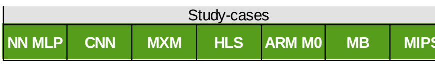
The lower the better











Asynchronous Fault Injection

- Inject faults in designs when Xilinx native scrubber (FRAME_ECC) is active
- Fault may be injected during DUT processing cycle
  - And scrubbed at any point in time of the processing cycle

Randomize bit-flip location → Inject Fault on CRAM (ICAP) → Check and Report Failure → OK / Failure → Power cycle & reprogram

Split in two independent processes

Emulates radiation

Randomize bit-flip location → Inject Fault on CRAM (ICAP)

Same test monitoring used under radiation

Check and Report Failure → OK / Failure → Power cycle & reprogram

Asynchronous Fault Injection

- Test results for two implementations of *study-case CNN* for traffic sign classification (RADECS 2019, JICS 2021)

Mission time for R(f) ≥ 90% from fault injection

Accumulated faults injected

100
90
80
70
60
50
40
30
20
10
0

Float Q16 Q10 Q10 H Float S Q16 S Q10 S Q10 H+S

Design variant

The higher the better

Mission time for R(Φ) ≥ 90% from heavy ions

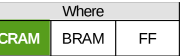
Particle fluente (Φ)

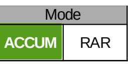
2500
2000
1500
1000
500
0

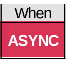
Float Q16 Q10 Q10 H Float S Q16 S Q10 S Q10 H+S

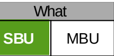
Design variant

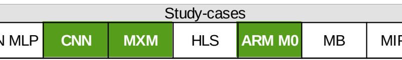
Implementations using Xilinx scrubber







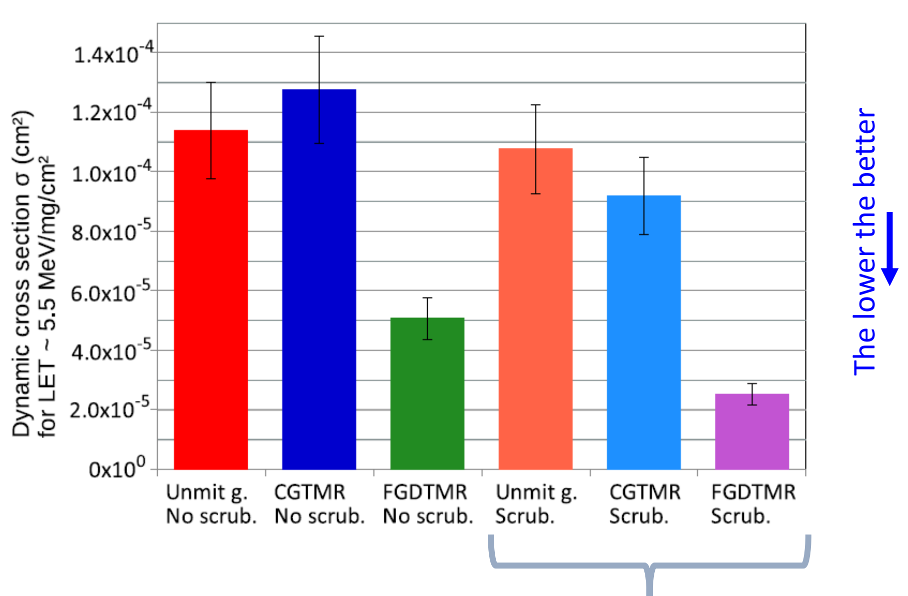




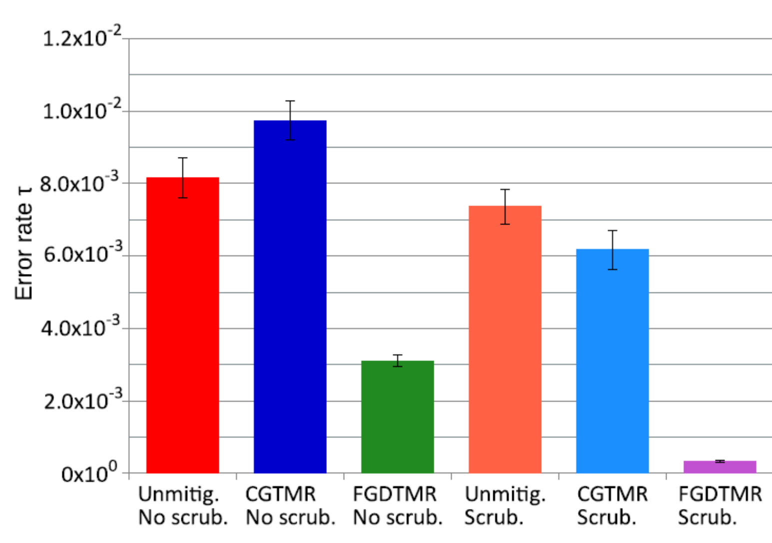
Asynchronous Fault Injection

- Test results for experimental design implementing a *softcore microprocessor* with different levels of fault mitigation (TNS 2019)

Dynamic cross section from heavy ions



Error rate from fault injection



$$\sigma_{failure} = \frac{N_{failure}}{\Phi}$$

Implementations using Xilinx scrubber

$$\tau_{failure} = \frac{N_{failure}}{N_{faults\,injected}}$$

Emulation of multiple-bit upsets

- All bit-flips must be seen as a single SEU
  - Instrument clock-gate for design under test
- Scrubber should not correct partially injected SEU
  - Suspend scrubber during MBU injection (FPGA control registers)
- A table of most frequent MBU geometries was embedded into the fault injection module
  - Single command, faster communication
- It is up to the fault injection campaign scripting to decide the ratio of SBU and MBU, and its geometry, to emulate the targeted radiation environment

Emulation of multiple-bit upsets

- Test results for experimental design of *matrix multiplication generated by high-level synthesis (HLS)*

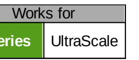
Mission time for R(f) ≥ 95%

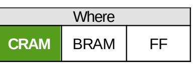
Accumulated faults

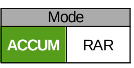
		SBU Only	SBU+MBU (IEAv)	SBU+MBU (16O 38.4 MeV)	SBU+MBU (28Si 73.5 MeV)
No scrubber	Unhard	3.0	2.7	2.8	1.6
	CGTMR	8.1	5.9	4.5	4.3
	FGDTMR	15.2	12.3	10.8	8.3
Scrubber active	Unhard	3.2	2.9	2.0	2.1
	CGTMR	18.5	10.4	5.4	5.4
	FGDTMR	22.5	15.4	10.0	8.1

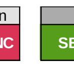
$$R_{Weibull,\alpha,\beta}(t)=e^{-\left(\frac{t}{\alpha}\right)^{\beta}}$$

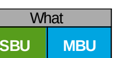
$$MT_{\{R(t)\geq r\}}=\alpha(-\ln r)^{\frac{1}{\beta}}$$

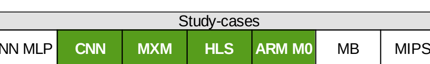












Mitigations: SCRUB | HAMM | SIHFT | CGTMR | FGTMR

Emulation of multiple-bit upsets

- Test results for experimental design of *matrix multiplication generated by high-level synthesis (HLS)*

More MBU
More scrubber disruption
More FGDTMR disruption
Lower mission time

Accumulated faults

	Unhard (No scrubber)	CGTMR (No scrubber)	FGDTMR (No scrubber)	Unhard (Scrubber active)	CGTMR (Scrubber active)	FGDTMR (Scrubber active)
SBU Only	3.0	8.1	[illegible]	3.2	[illegible]	22.5
SBU+MBU (IEAv)	2.7	5.9	12.3	2.9	10.4	15.4
SBU+MBU (16O 38.4 MeV)	2.8	4.5	10.8	2.0	5.4	10.0
SBU+MBU (28Si 73.5 MeV)	1.6	4.3	8.3	2.1	5.4	8.1

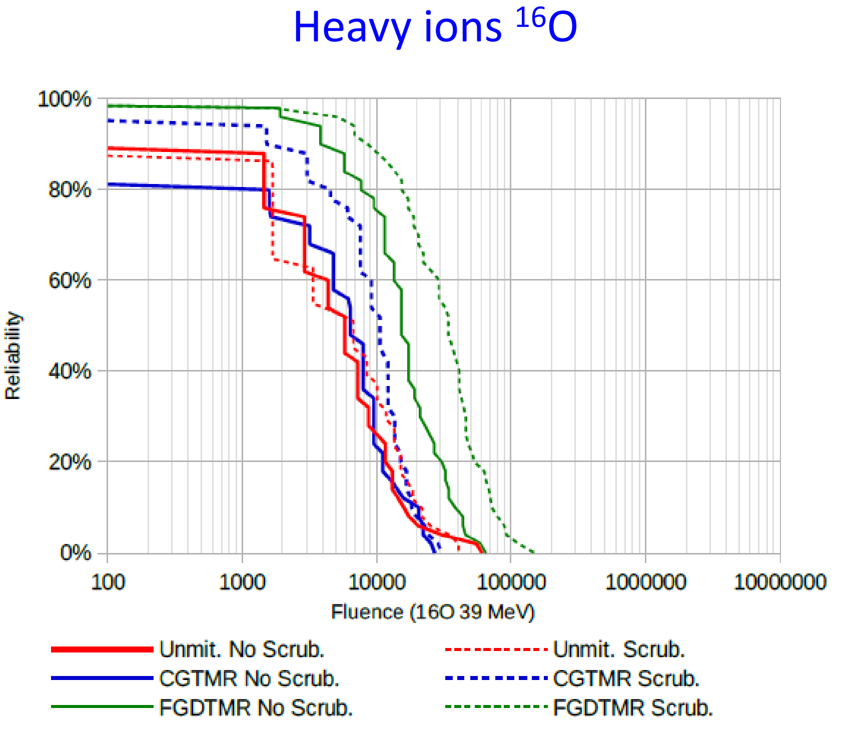
$$R_{Weibull,\alpha,\beta}(t)=e^{-\left(\frac{t}{\alpha}\right)^{\beta}}$$

$$MT_{\{R(t)\geq r\}}=\alpha(-\ln r)^{\frac{1}{\beta}}$$

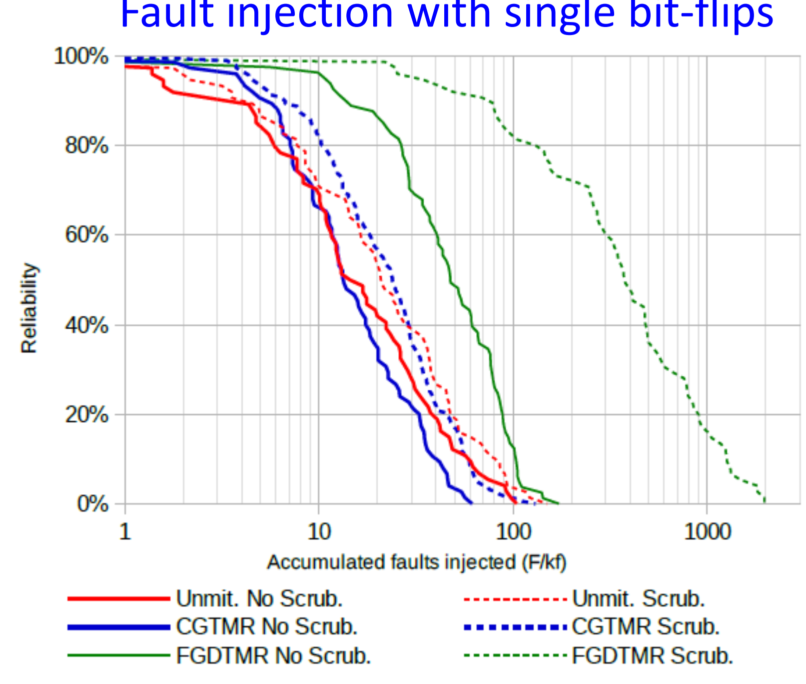
Emulation of multiple-bit upsets

- Test results for experimental design implementing a *softcore microprocessor* with different levels of fault mitigation (TNS 2019)

Heavy ions ^{16}O

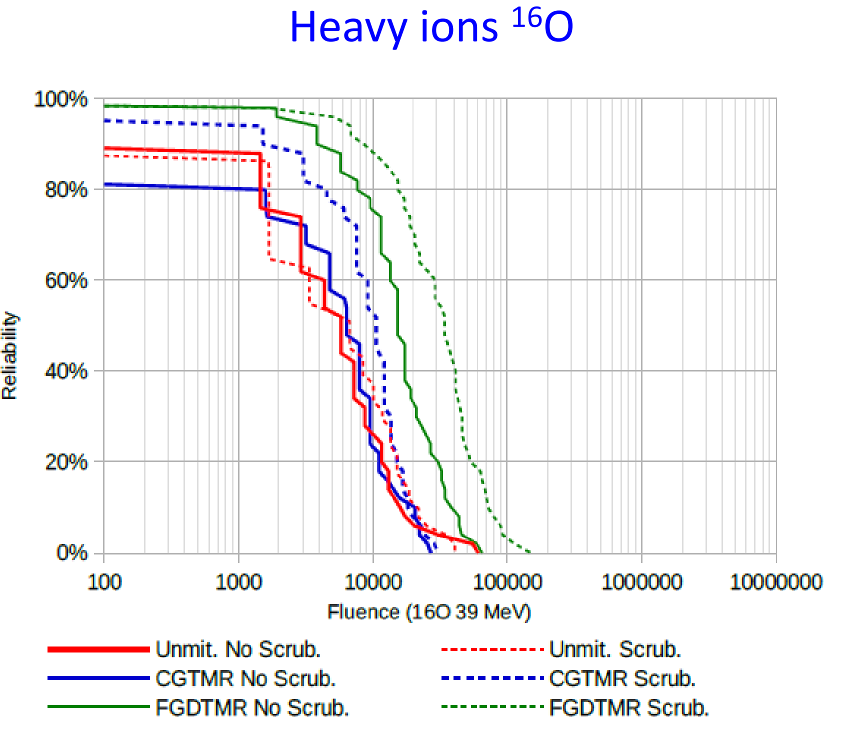


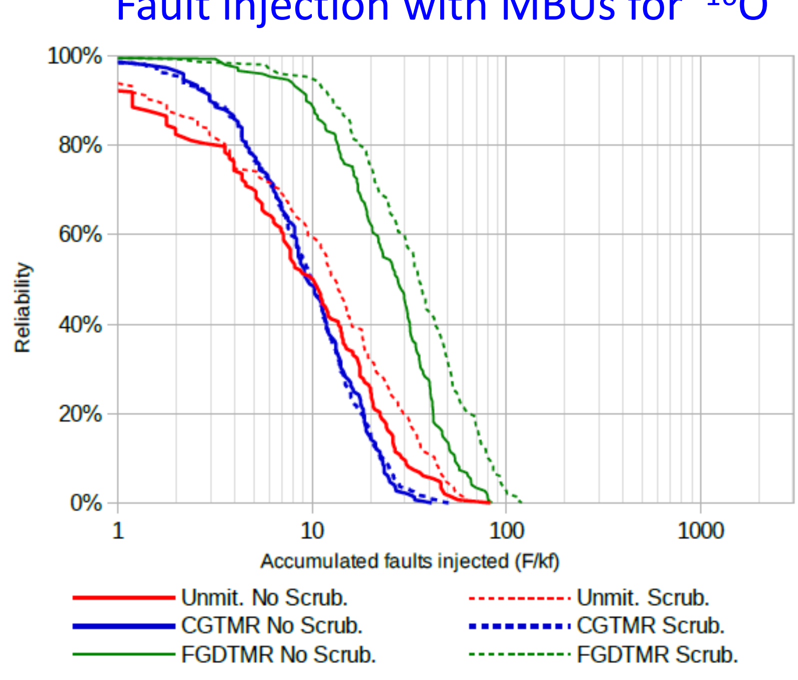
Fault injection with single bit-flips

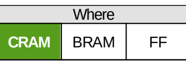


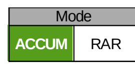
Emulation of multiple-bit upsets

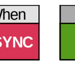
- Test results for experimental design implementing a *softcore microprocessor* with different levels of fault mitigation (TNS 2019)

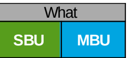




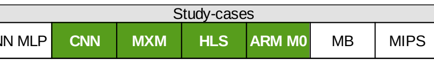








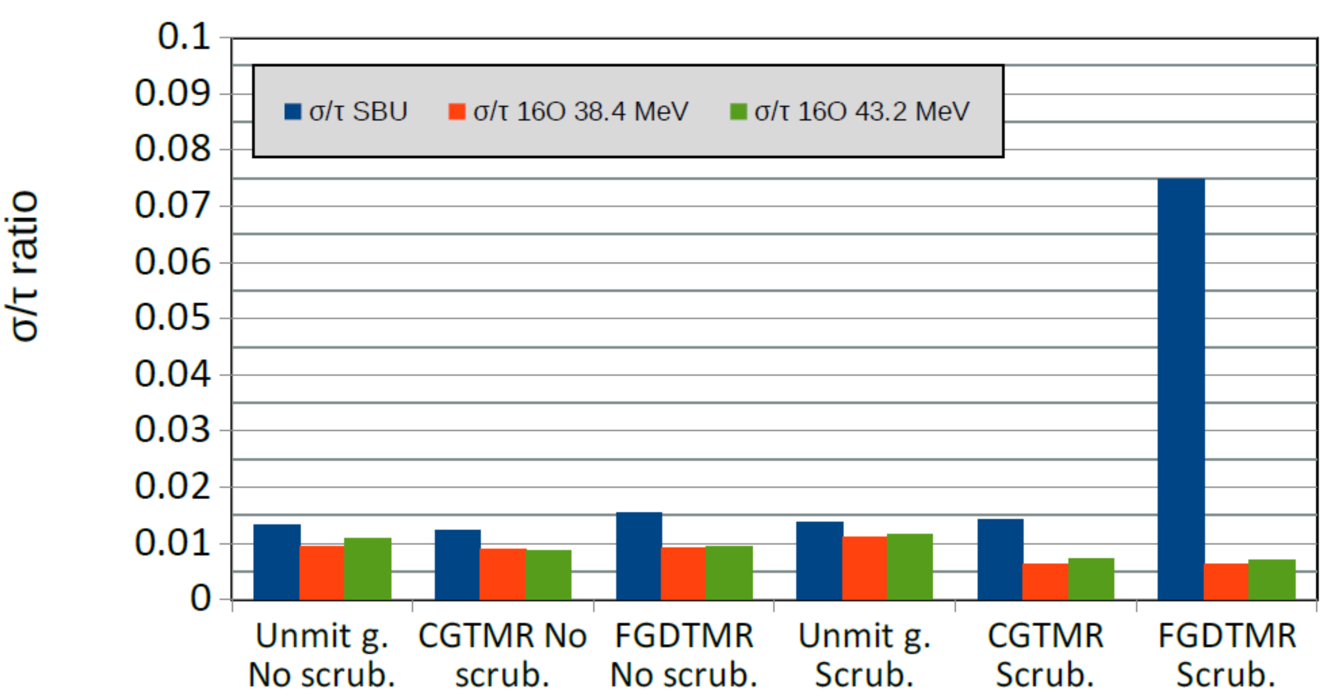
What: SBU | MBU



Mitigations: SCRUB | HAMM | SIHFT | CGTMR | FGTMR

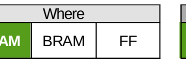
Emulation of multiple-bit upsets

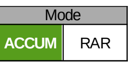
- Test results for experimental design implementing a *softcore microprocessor* with different levels of fault mitigation (TNS 2019)

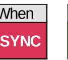


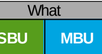
$$\sigma_{failure} = \frac{N_{failure}}{\Phi}$$

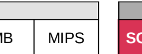
$$\tau_{failure} = \frac{N_{failure}}{N_{faults\ injected}}$$





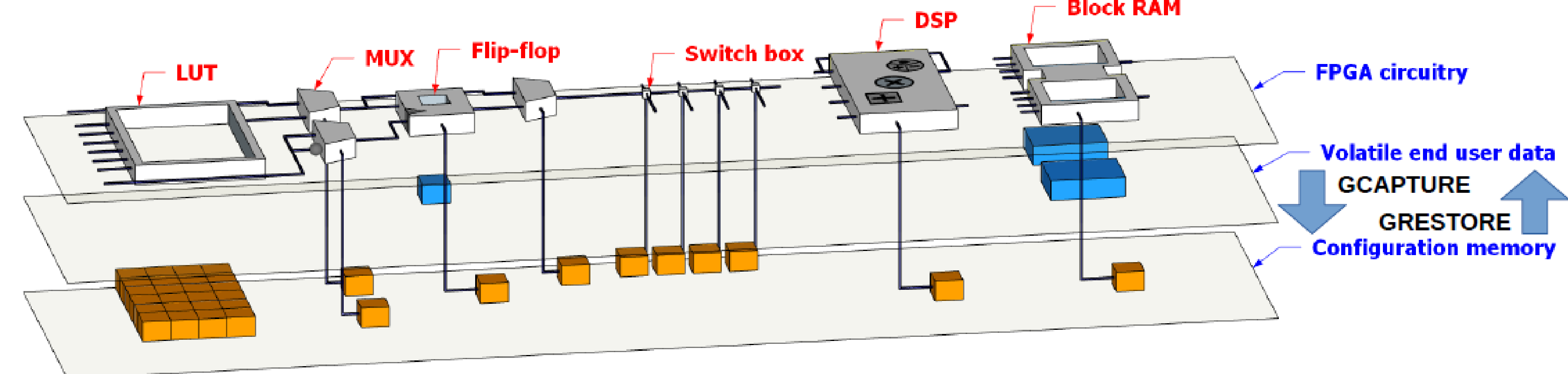






Fault injection on flip-flops

- Reuse the mechanisms for capture, readback, partial reconfiguration mask and reset after reconfiguration (RAR)
  - 7 Series only, RAR is different for UltraScale+
  - Can be used concomitantly with the CRAM fault injection



Fault injection on flip-flops

- Test results for experimental design of *softcore* MicroBlaze and miniMIPS microprocessors onboard NanoSatC-BR2 cubesat payload (RAW 2019)
  - Software hardened by SIHFT techniques
  - Faults injected selectively on <u>CLB flip-flops only</u>

Distribution of errors and functional failures

100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%

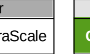
MicroBlaze
miniMIPS

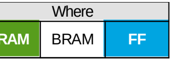
Reboot
Compute timeout
Boot timeout
SDC
DUE

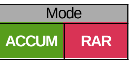
DUE triggered by SIHFT

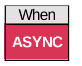
MicroBlaze register file <u>not</u> stored on flip-flips

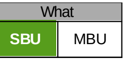
miniMIPS register file is stored on flip-flips (including $PC and $RA)

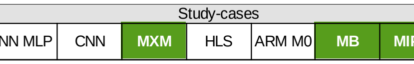


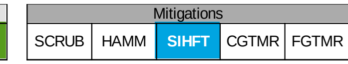






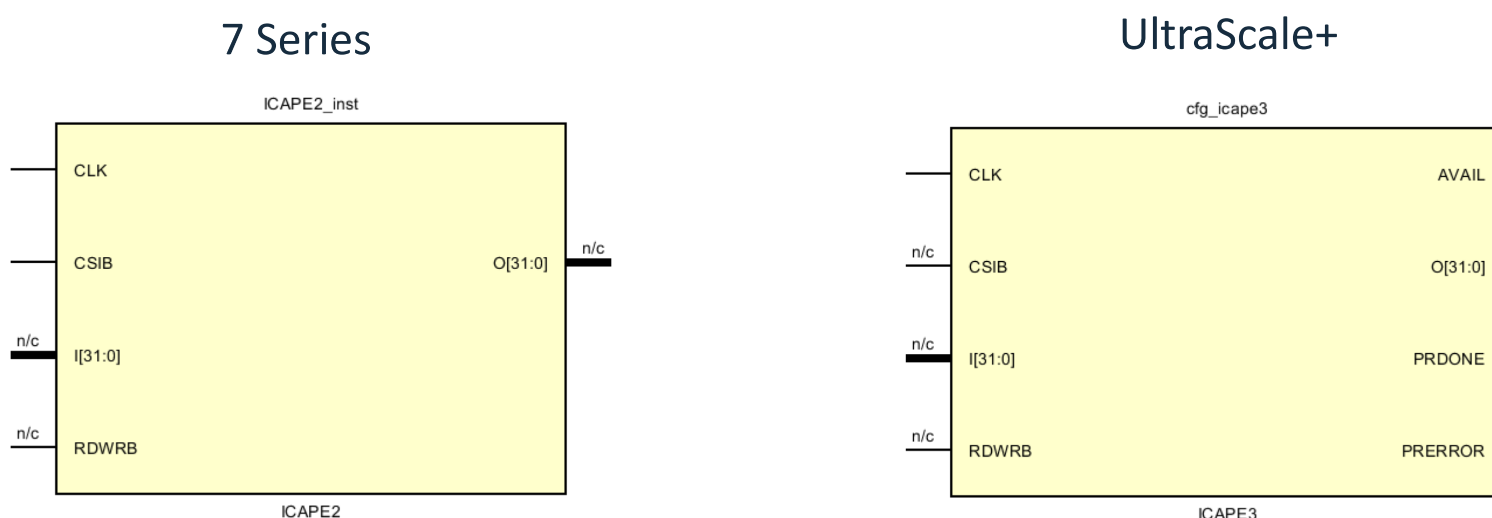






Port of fault injector to UltraScale+

- Main changes
  - Different number of bits inside a frame
  - Switch box columns addressed independently
  - New semantics for some FPGA registers
  - Minor changes on ICAP hardware block interface
    - Better coordination among multiple ICAP instances



Port of fault injector to UltraScale+

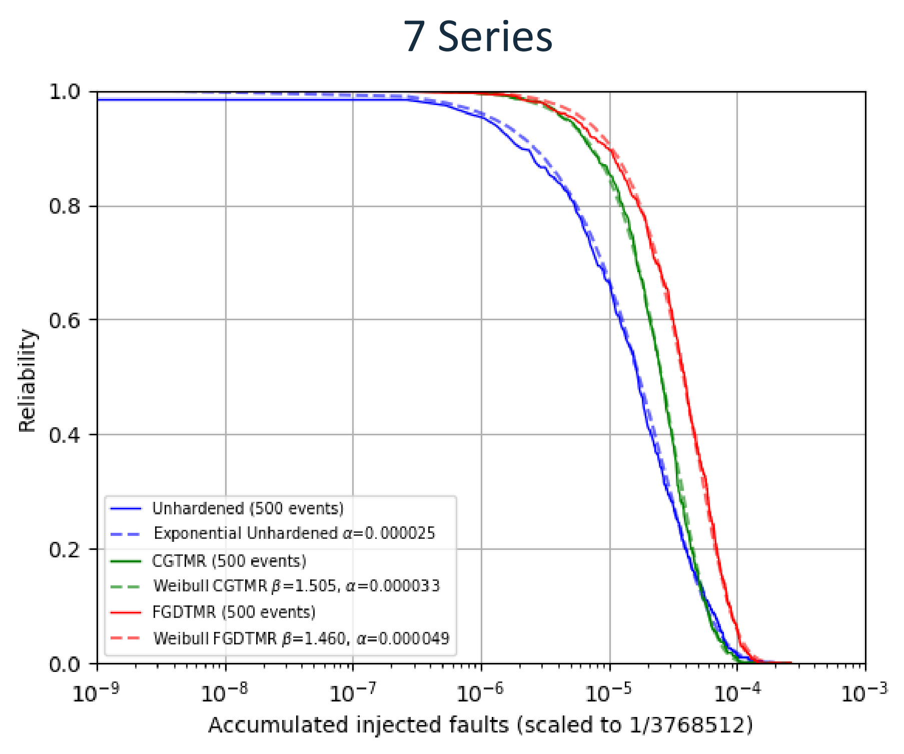
- Test results for experimental design of *matrix multiplication generated by high-level synthesis (HLS)*

Matrix Multiplication Benchmark Application	
7 Series Zynq-7000 SoC (Z030)	Ultrascale+ Zynq MPSoC (ZU3EG)
Clock: 100 MHz WNS (FGDTMR): 0.7 ns	Clock: 100 MHz WNS (FGDTMR): 3.1 ns
Unhardened: LUT 487 FF 564 CARRY4 59 BRAM 3 DSP 7	**Unhardened**: LUT 430 FF 564 CARRY8 28 BRAM 3 DSP 7
CGTMR: LUT 1691 FF 1692 CARRY4 177 BRAM 9 DSP 21	**CGTMR**: LUT 1536 FF 1692 CARRY8 75 BRAM 9 DSP 21
FGDTMR: LUT 8383 FF 3276 CARRY4 132 BRAM 9 DSP 18	**FGDTMR**: LUT 8381 FF 3276 CARRY8 66 BRAM 9 DSP 18
FI pblock 1166 frames x 101 words = 3768512 bits	FI pblock 1330 frames x 93 words = 3958080 bits

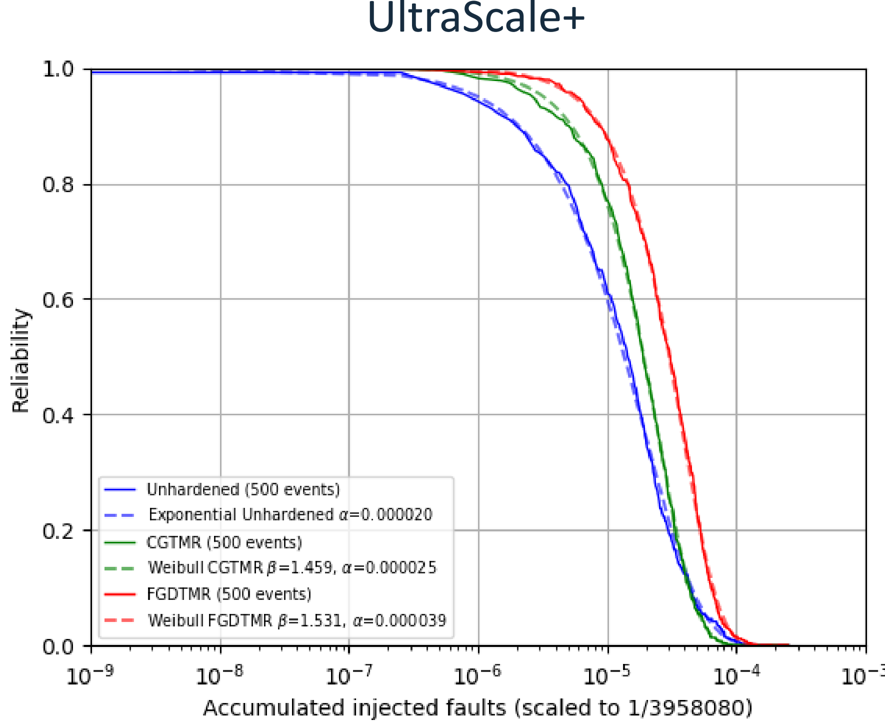
Port of fault injector to UltraScale+

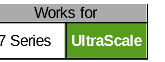
- Test results for experimental design of *matrix multiplication generated by high-level synthesis (HLS)*

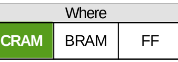
7 Series

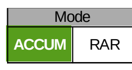


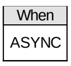
UltraScale+

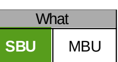


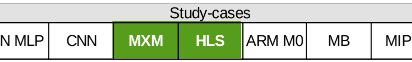












Mitigations: SCRUB | HAMM | SIHFT | CGTMR | FGTMR

Final discussion

- Legacy features of UFRGS fault injector ported successfully to UltraScale+
- Tighter integration of fault injector with clock gating and FPGA control registers allowed coexistence of scrubbing and MBU emulation

- Fault injector support to MBU improved fidelity to radiation
  - MBU breaks scrubbing
  - MBU breaks fine-grained distributed TMR
  - Without MBU, the fault injector is exceedingly optimistic

- Fault injector operates with a general interface
  - It is up to the campaign planning and scripting to emulate the MBU profile of the targeted environment

Future work

- Open to new experiments:
  - UltraScale+ new reset-after-reconfiguration (RAR, PR) policies
  - UltraScale+ softcore only scrubber (SEM IP)

- Port fault injector to Xilinx Versal ACAP
  - Keep up with new product family and technology (FinFET 7 nm)

Thank you for your attention!

Contact details

Name:	Fernanda Lima Kastensmidt
	Head of Fault Tolerance & Reliability Team
Affiliation:	Universidade Federal do Rio Grande do Sul (UFRGS)
Email:	fglima@inf.ufrgs.br
Link:	www.inf.ufrgs.br/~fglima