Strategies for reliable on-board reconfiguration of FPGAs (R3FPGA)

16.03.2023

SpacE FPGA Users Workshop, 5th Edition

[1]BISCHOFF, Ole; JIA, Lei ; GRÜRMANN, Kai; USTAOGLU, Buse ; RUST, Jochen
[2]BUCHHORN, Dennis; FIETHE, Björn; KLEINBECK, Benedikt ; MICHALIK, Harald
[3]MÜLLER, Urban
[4]SANTOS FALCON, Lucana

[1]DSI Aerospace Technologie GmbH
[2]Institute of Computer and Network Engineering (IDA), TU Braunschweig
[3]HENSOLDT Sensors GmbH
[4]Moltek Consultants Ltd. For European Space Agency

INSTITUT FÜR DATENTECHNIK UND KOMMUNIKATIONS-NETZE

Motivation
Use Cases and Demonstrators
System Design
Reconfiguration Engine
Test Platform
Radiation Tests
Conclusion

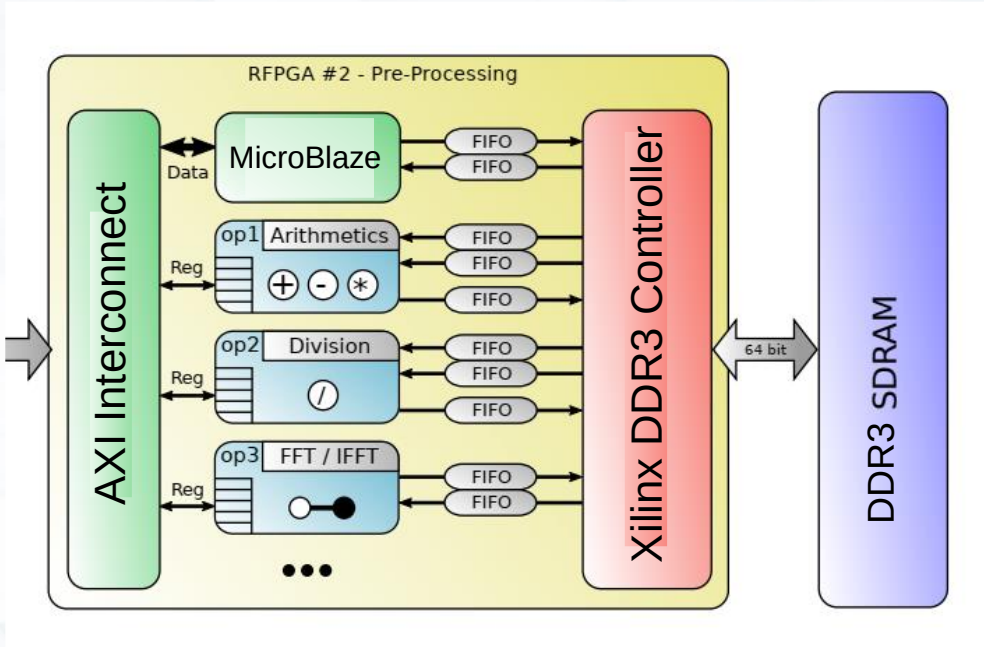
Motivation

- **Increasing demands** on the computing power of future missions can only be **fulfilled** by **efficiently usage** of available **resources**
- **Efficiency** can be achieved **through** greater **flexibility** (e.g. **reconfiguration** of FPGAs)
- The **challenge** is to enable **reconfiguration** of FPGAs from **different manufacturers** and **technologies** (Flash, SRAM) in space
- **Methods** are to be **developed**, such as a **generic interface** to a reconfiguration engine **based on** standardized TM/TC commands (**PUS**) implemented in the **bootloader**
- Finally, the results of this study will support the use of **reconfiguration** of **FPGAs** under **space conditions**

Science Use Case – Optical / Hyperspectral

Processing of optical and hyperspectral instrument data

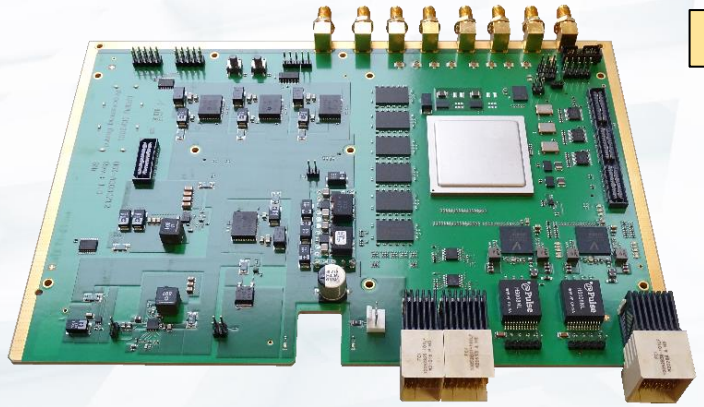
- **Optical** or **hyperspectral** instruments leads to **high** computational **demands**
- Even classical ground **processing** steps like data evaluation already need to be **performed on-board** in near **real time**, and needs to be **adaptable** to changing mission specific requirements
- Such a **processing pipeline** has to be **flexible**, consisting of a high quantity of different processing modules, which can be **loaded on demand**
- This use of partial in-flight **reconfiguration** will not only **improve** the **resource utilization** of the processing pipeline, it generally **enables** to use all the required **modules** in a **time-shared** approach
- This use case will be implemented on an **Ultrascale** FPGA from Xilinx (**SRAM-based**)

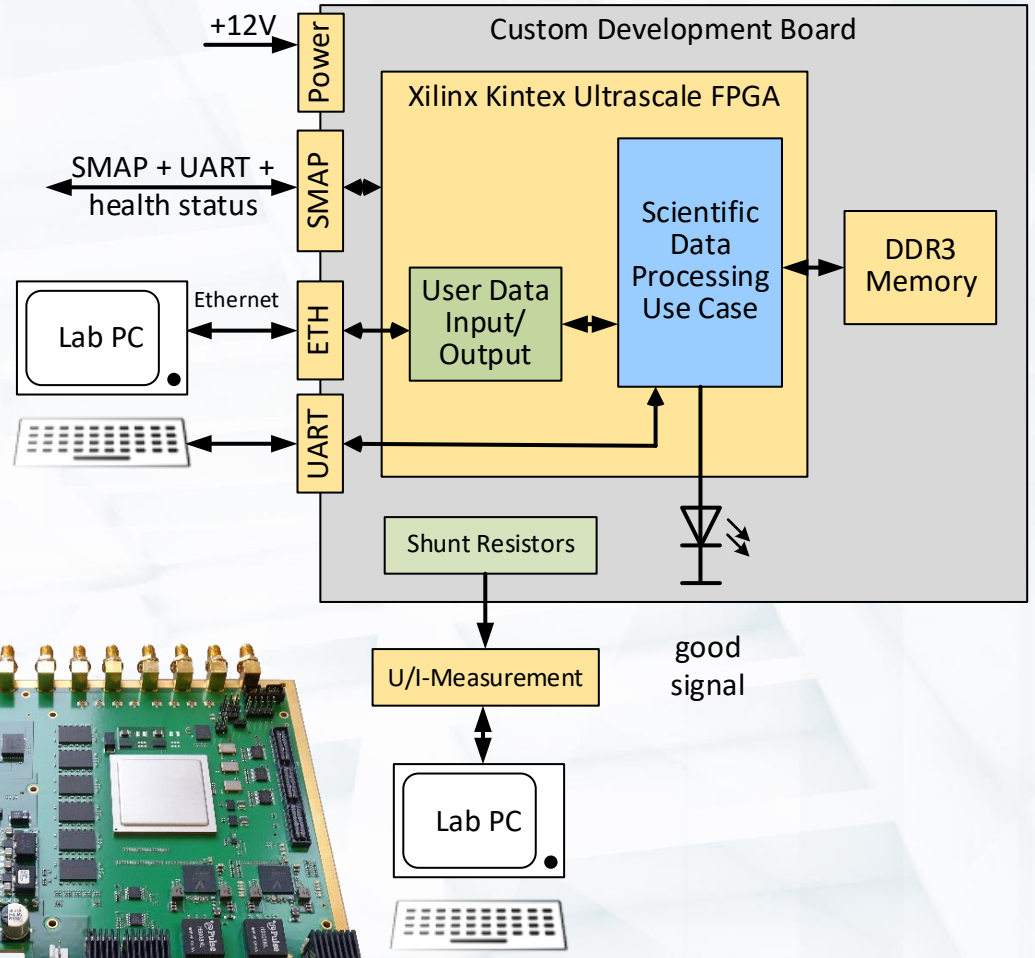


Science Use Case Demonstrator – Optical / Hyperspectral

Demonstrator for optical and hyperspectral instrument data processing

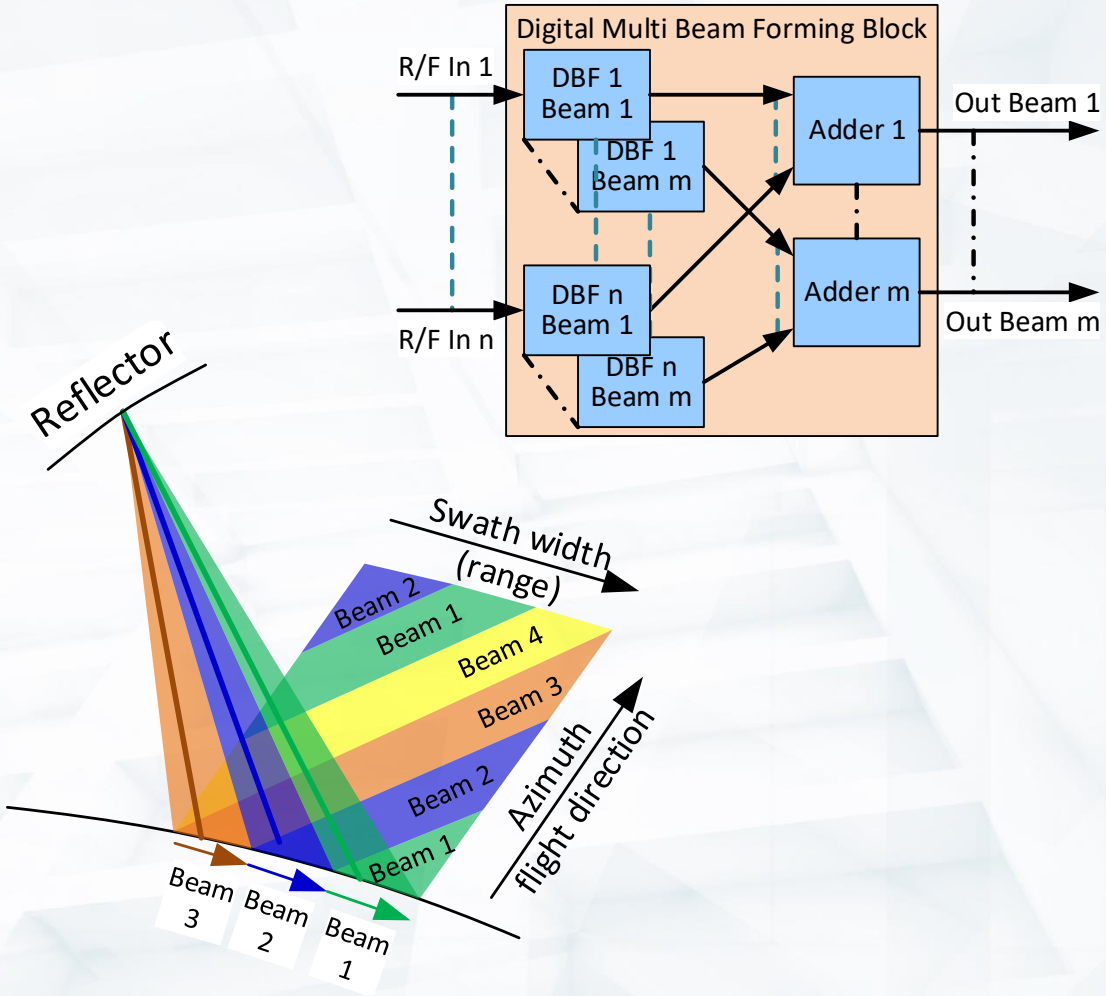
- Custom cPCI-SS development board equipped with **XCKU060** (XQRKU060) FPGA
- **Demonstrator** can be connected directly to a reconfiguration engine control board by **dedicated connector**
- 8-bit parallel **SelectMap configuration IF** provides a good comprise between overhead and speed
- **Health monitoring** by internal Xilinx **SEM IP-Core** includes scrubbing of the configuration FPGA
- **SEM IP-Core** is also used to perform **fault injection** into the Xilinx FPGA and thus exercise FDIR aspects during verification
- **Scrubbing** and **error detection** by **external rad-hard** device is **needed** for **reliable** on-board **reconfiguration**





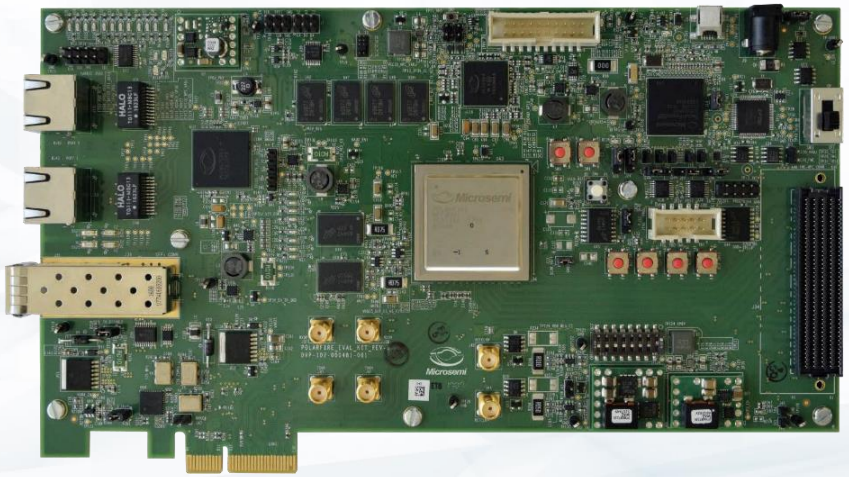
Synthetic Aperture Radars (SAR) with wide swath width and Scan-On-Receive (SCORE)

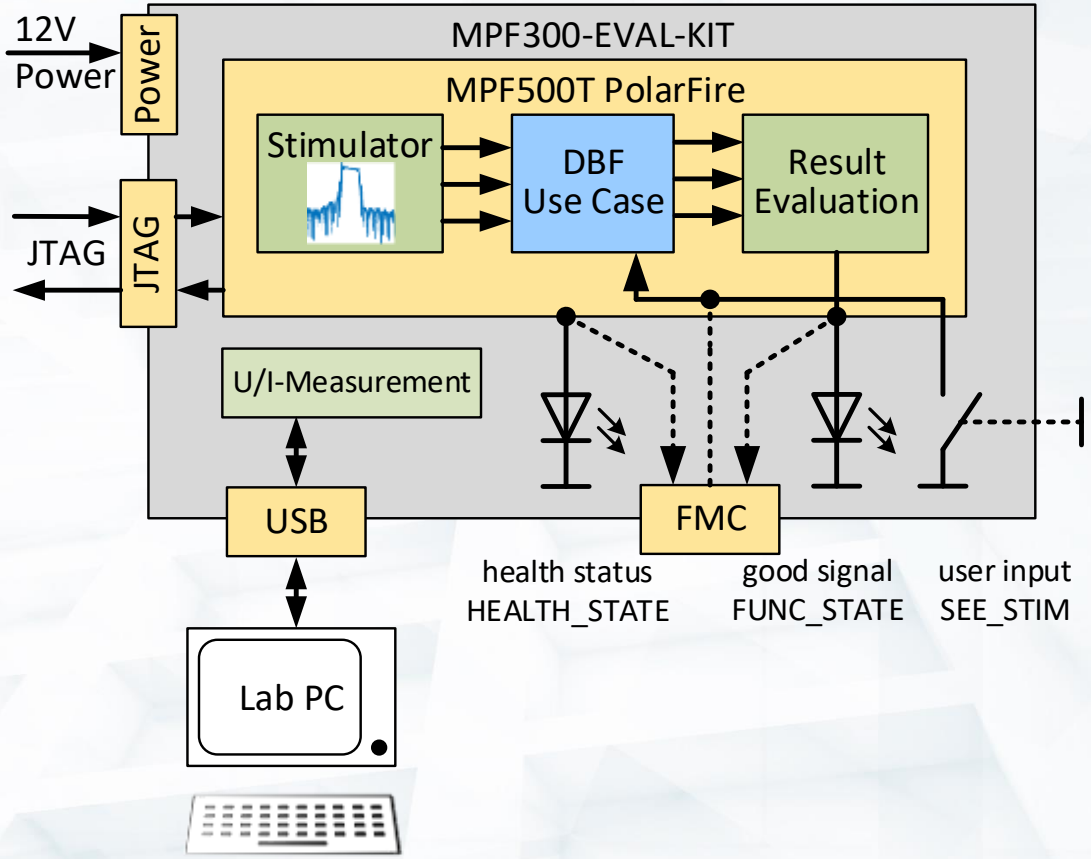
- The **SAR** application uses **multiple beams** at the same time to reach the needed **low noise** levels and **side lobe suppression**
- The **SCORE** principle supports 3 to 4 **simultaneous** active **beams**. On the receive side are 3 to 4 beams received on the same time with different range angles caused by the successively sent transmit pulses (Tx) and therefore different receive angle caused by the different time of flight (ToF) / echo positions
- The **reconfiguration** of the digital multi beam forming block allows the usage of several **filtering methods** or **refreshing** of the FPGA fabric Flash memory
- This use case will be implemented on a Microchip **PolarFire** FPGA (**Flash-based**)



Demonstrator for Radar use case

- Microchip **MPF300-EVAL-KIT** represents the use case demonstrator
- **Partial reconfiguration** is **not supported**, since it is a **flash-based** FPGA
- **JTAG** is selected as the **reconfiguration** interface
- **Monitoring signals** via the **FMC**
- **User input** (switch) to stimulate a **SEE** and induce a **SEFI**

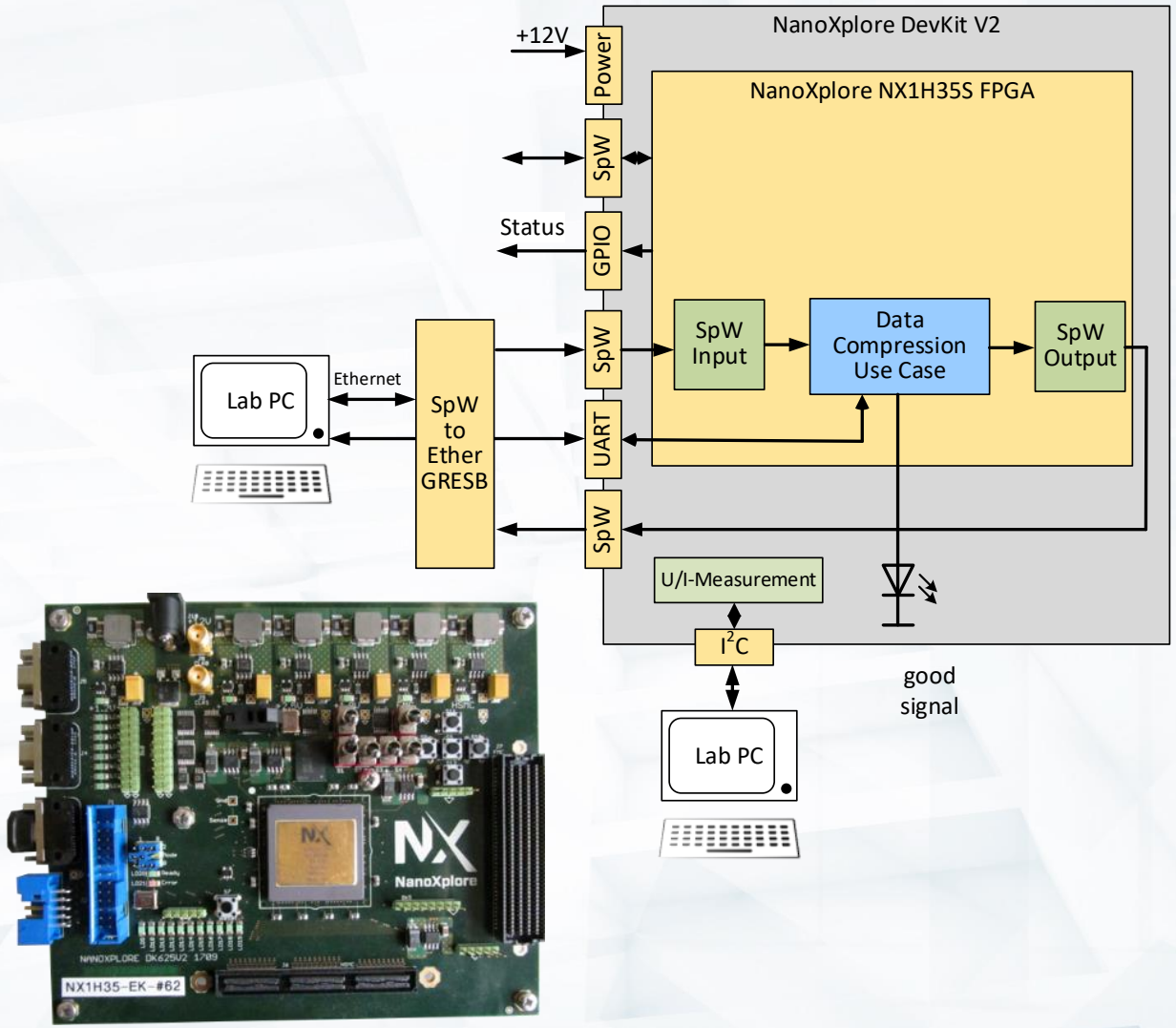




Science Use Case Demonstrator – Data Compression

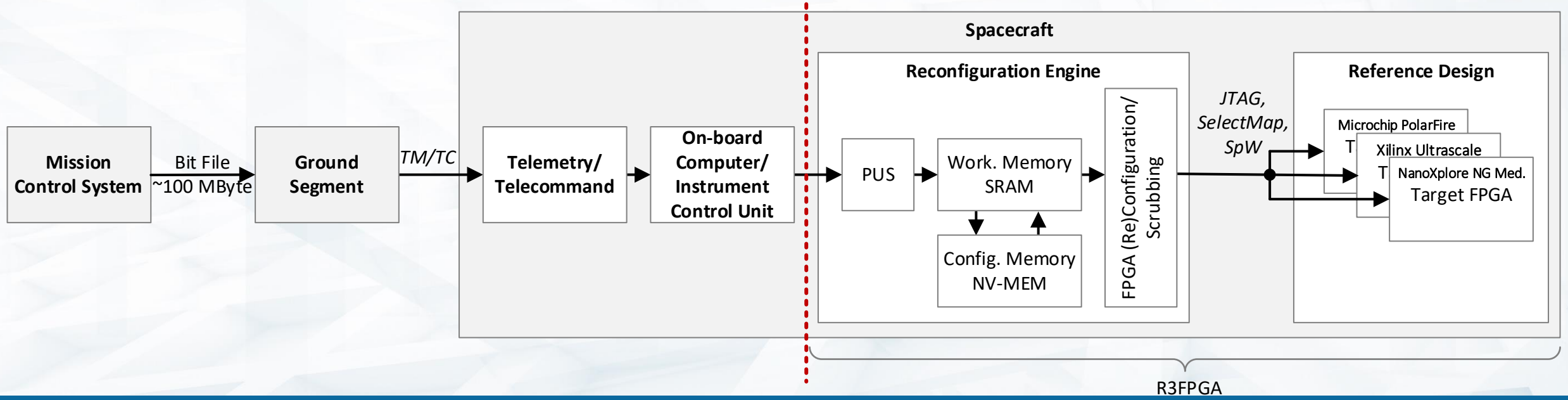
Data compression use case and demonstrator

- Dedicated lossless data **compression** and **decompression** programs based on Rice coding according to the CCSDS-121 standard
- Depending on the **reconfiguration compression or decompression** is available
- Implementation on a **NanoXplore** NG Medium FPGA (**SRAM-based**)
- COTS DevKit V2, containing the NG_Medium (**NX1H35S**) FPGA
- **SpaceWire** interface for **reconfiguration**
- Data input and output for the use case is performed by the available SpaceWire interfaces
- A serial UART interface is available for debugging
- **No external scrubbing** needed due to integrated **Configuration Memory Integrity Check**, but SEFI detection and correction is required



System Design - Architecture

- The **system** consists of a **target FPGA** (use case) and a reliable/flexible **reconfiguration engine**
- **Reconfiguration engine** is responsible for **reconfiguration** and managing the proper state of the target FPGA that includes **detecting and responding** to single-event functional interrupts (**SEFIs**) as well as **scrubbing** of configuration memory for SRAM-based FPGAs
- Target FPGAs: Xilinx Ultrascale (SRAM), NanoXplore NG-Medium (SRAM), Microchip Polarfire (Flash)

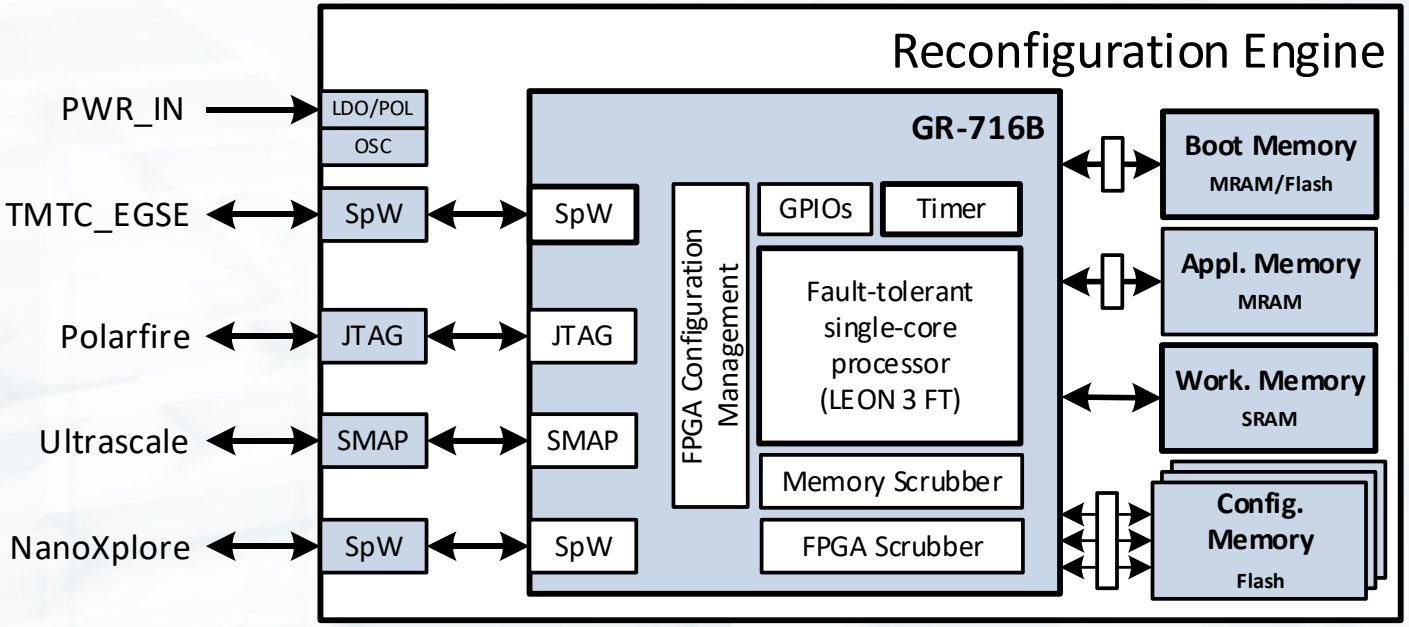


High-level Requirements Summary

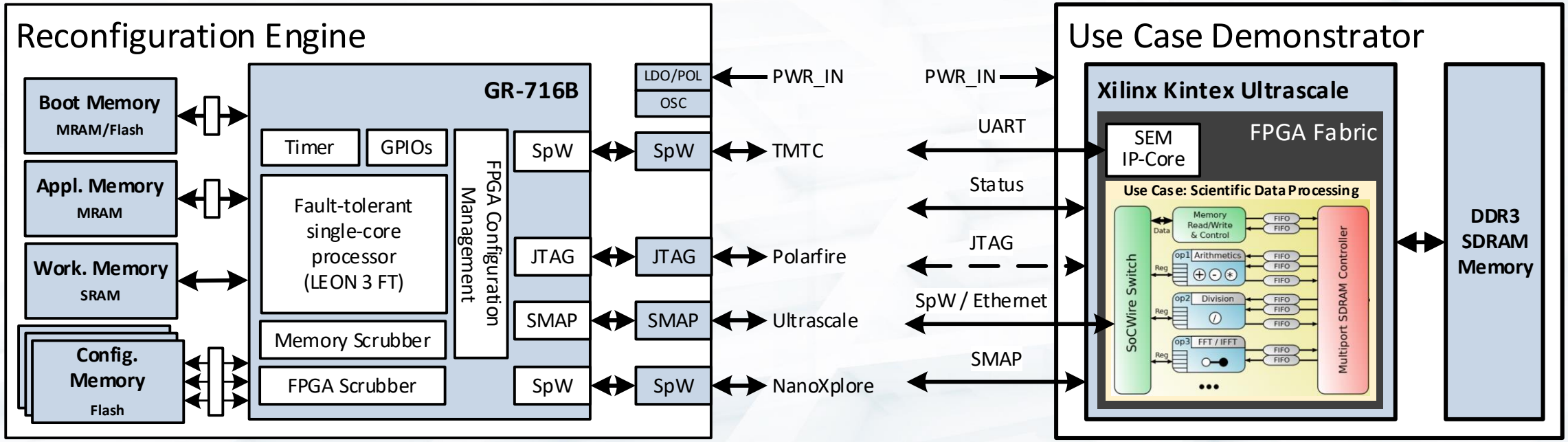
- Partial / full reconfiguration
- Support multiple target FPGAs
- Reliability and robustness against radiation induced SEEs during the critical reconfiguration process
- Reconfiguration engine based on rad-hard FPGA/CPU
- Dedicated configuration memory to store the bitfile
  (at least 128 MByte to support newer FPGAs)
- Interface for reconfiguration and scrubbing incl HW drivers
- Support PUS-based TM/TC commands (bootloader)
- Health monitoring of target FPGA during programming and operation incl U/I measurements

Architecture Design

- Based on GR-716B LEON3FT microcontroller from Frontgrade Gaisler
  - Memory/FPGA scrubber
  - TM/TC IF: Spw
  - Reconfiguration IFs: SpW, JTAG, SMAP
- Configuration memory (Flash)
  ECC protected (EDAC, TMR/DMR + CRC)
- Boot memory (MRAM/Flash)
- Application memory (MRAM)
- Working memory (SRAM)

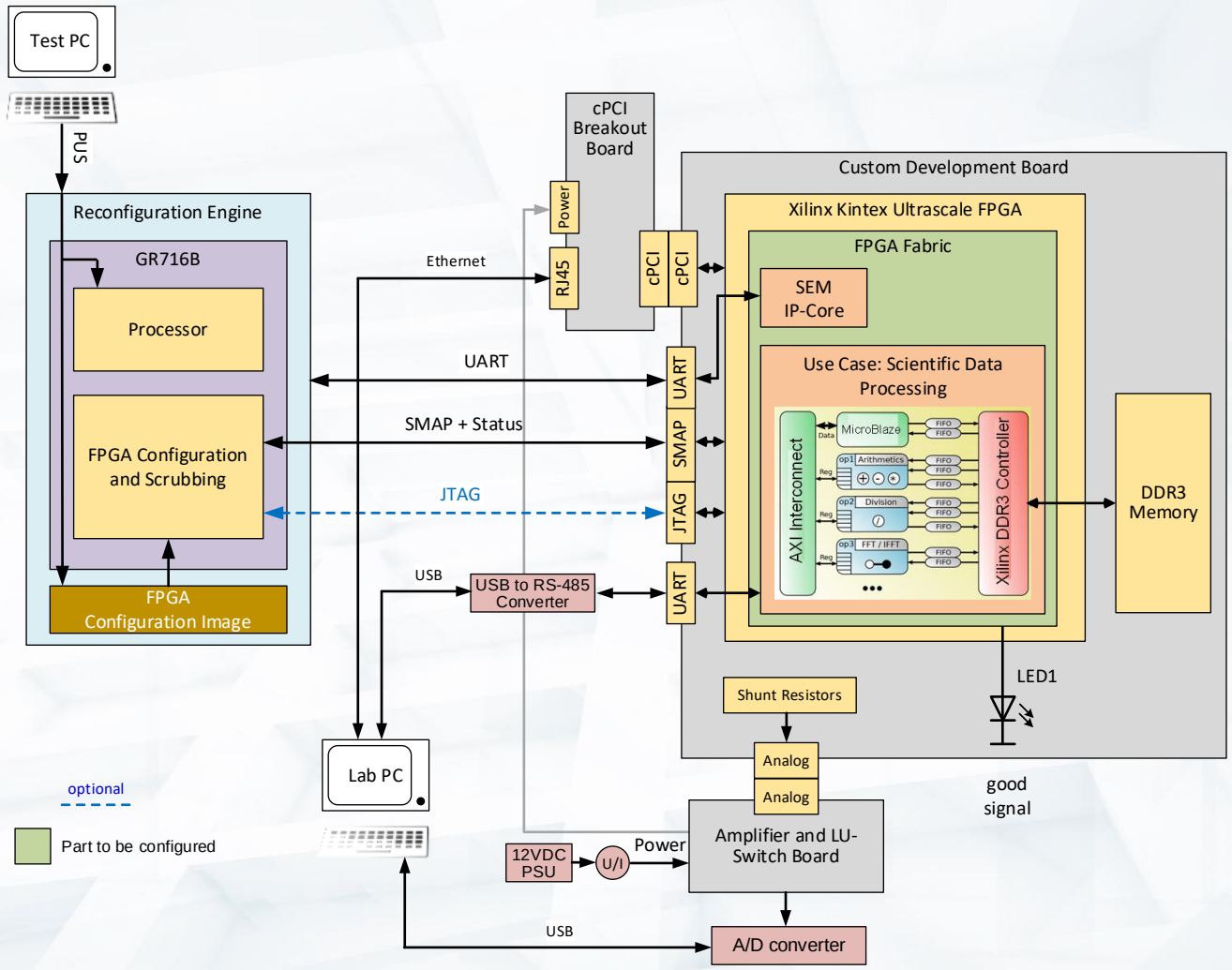


- The **reconfiguration engine** and the three **use case demonstrators** are **integrated** and **tested**
- A selected **demonstrator** (Xilinx Ultrascale) together with the **reconfiguration engine** will **form** the **test platform**
- The **test platform** is used for the **radiation tests**



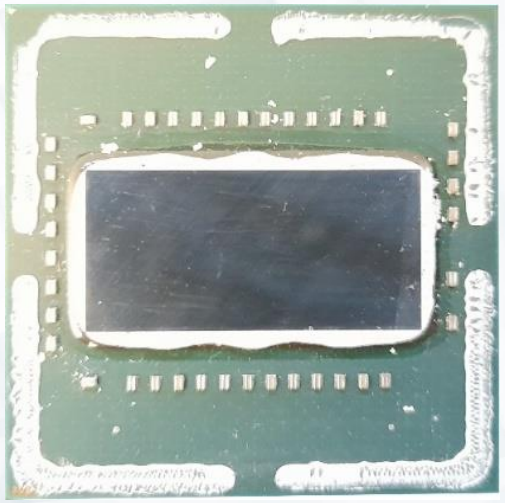
Approach

- **Heavy ion** and **proton test** of the Xilinx Kintex XCKU060 FPGA with focus on reconfiguration
- As the **chip area** used for **reconfiguration** is very **small** compared to the whole FPGA the cross section of possible **errors** during reconfiguration is believed to be quiet **small**
- The **test equipment** will be able to **determine all** different Single Event Effects (**SEE**) already described in the literature to **determine** whether **additional** SEE develop **during** the **reconfiguration** process



DUT Preparation

- Xilinx Kintex XCKU060 **FPGA** is packaged as a **flip-chip BGA**
- To allow the accelerator **ions** to reach the **active zone** of the chip the **heatsink** has to be **removed** and the **die** has to be **thinned**
- This might **influence** the **SEL susceptibility** as parts of the substrate forming **parasitic thyristor** structures responsible for SEL are **removed** by the thinning process
- The heatsink was removed successfully and the initial **thickness** of the **die** was measured to be **~760 µm**
- **Thinned** DUT is very **fragile** and sensitive to **temperature changes** and might **impede soldering**
- As an **alternative** to soldering a **socket** is foreseen. But the **cover** needs some **modification** in order to allow to **penetrate** the **ions** and **avoid damaging** the die, while applying sufficient **pressure** to the >1000 contacts
- At facilities like Jyvaskyla, Finland (**JYFL**) a **wide LET range** could be tested



Summary

- Future missions have increasing demands on computational power that can be meet by enhancing **efficiency** through **flexibility/reconfiguration**
- Solution for **reconfiguration** needs to be **reliable** (radiation) and **generic** (manufacturers/technologies)
- Three use case **demonstrator** are developed that represent **different manufacturers** and **technologies**
  KU060/SRAM-based/SMAP *PolarFire/Flash-based/JTAG* *NanoXplore/SRAM-based/SpW*
- **Reconfiguration** engine based on the rad-hard **GR-716B** offers several **reconfiguration IFs** and **scrubbing**
- **Reconfiguration** engine and the use case **demonstrators** will be **integrated** and **tested**
- Finally the r**obustness/reliability** will be shown during **radiation tests**

Lookout

- Additionally, also parts with **embedded processors** and AI elements, like the XQR **Versal**, should be considered for a compatible reconfiguration engine

Acknowledgment

The work is carried out under ESA contract No. 4000134941/21/NL/CRS.