# FPGA development in Airbus products

DEFENCE AND SPACE

Jean-Luc Poupat

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# FPGAs

Key components
for most of our digital designs

Usage ?

- Space products
- Test units
- Prototyping

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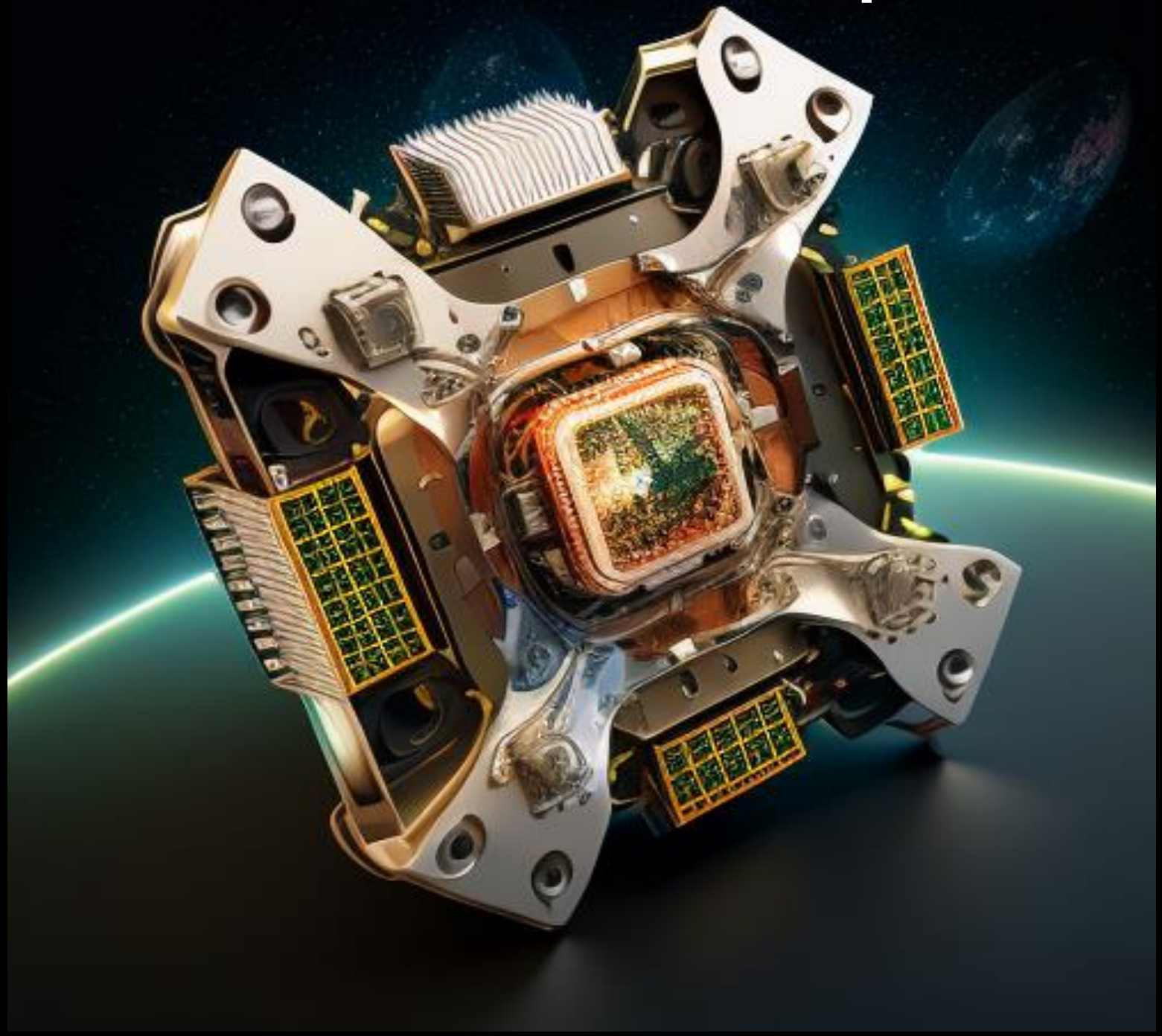
# Future of FPGA for Space ?



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# The Feedback Challenge

*30 years of FPGA in Airbus in 5 minutes*

## Skills, Process & Development Flow

*Adapting to FPGA evolution… and Pioneering it !*

## What else ?

*Other key topics about how to use FPGA in Space*

## Conclusion

*Not really a conclusion because story will continue…*

Airbus DS has developed FPGA for Space since more than 30 years.
Following slides will remind of FPGA types which have been considered / used up to the ones which are now evaluated for future projects, with some focus on key achievements

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# Antifuse FPGA used by Airbus D&S

- **MICROSEMI / ACTEL**
  - **A1020** → it all started here for FPGA introduction within Airbus DS !
  - **A1280**
  - **RT14100**
  - **RTSX32SU**
  - **RTSX72SU**
  - **RTAX2000**

# Reprogrammable FPGA used by Airbus D&S

- **MICROCHIP / MICROSEMI / ACTEL**
  - **ProASIC3**
  - **RTG4**
  - **RT PolarFire**




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# ProAsic3

- Good RETEX from (many) flight designs
- Very high filling rate (> 95%) possible thanks to improved design flow

# RTG4

The biggest Rad-Tolerant FPGA (150 KLUTs) before NG-Ultra (>500 KLUTs)

- Mastering tools is very complex, Airbus knows how to properly use them after huge number of exchanges with Actel/Microsemi

- Example of achievements: RTG4 with 78% filling rate, more than 50 clocks (some of them over 200 MHz) → has required to set up a dedicated design flow


Some performances reached by design team are at the extreme limit of what Microsemi experts thought it was possible to achieve on this FPGA target !

# Reprogrammable FPGA used by Airbus D&S

- **XILINX**
  - **Spartan 6**
  - **Kintex KU60**
  - **Zynq UltraScale +**
  - **Versal**

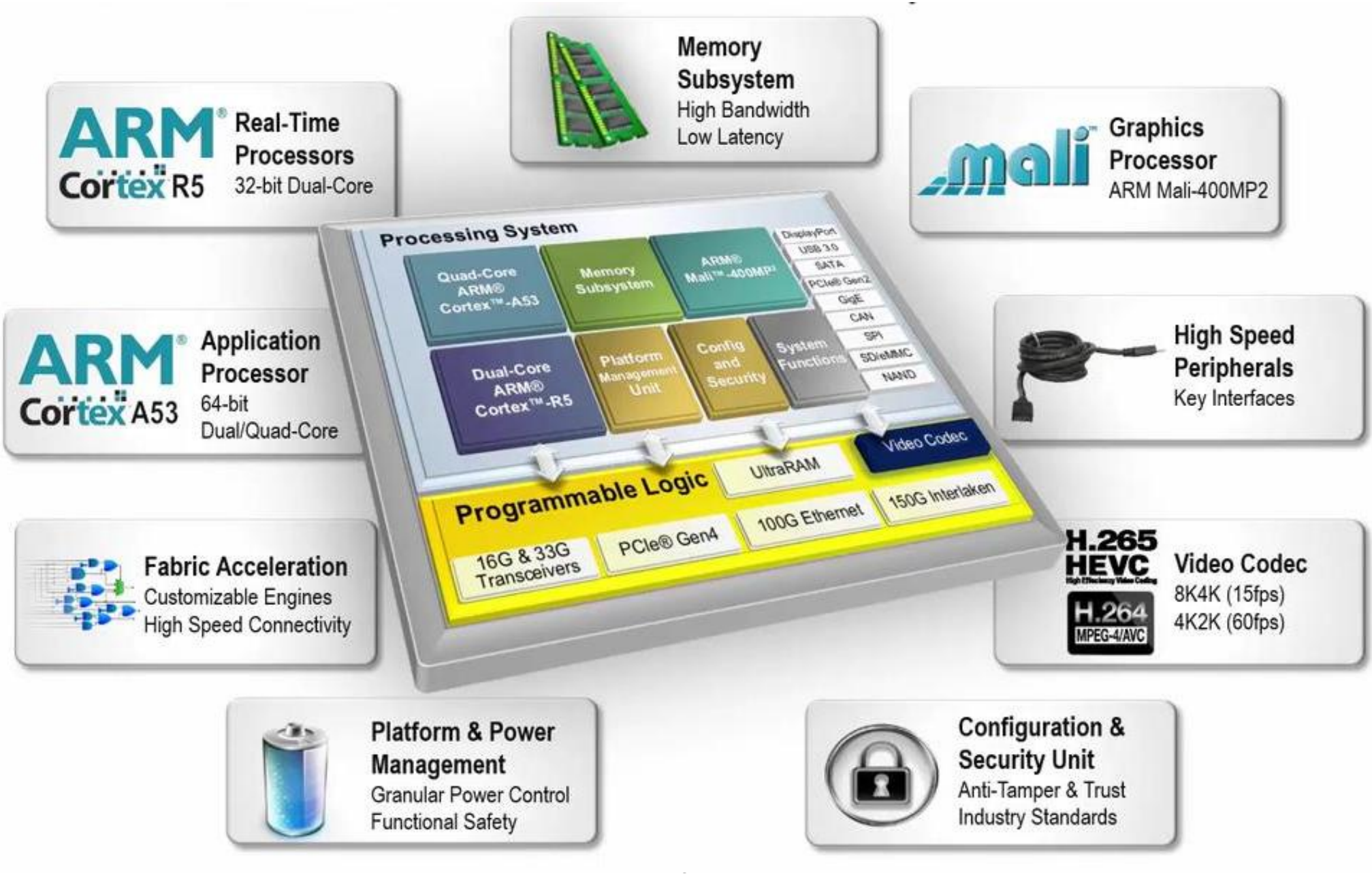
# Spartan6

COTS component not designed specifically for Space, but characterized by Airbus to be assessed in TRL and to be used from New Space to CQ1

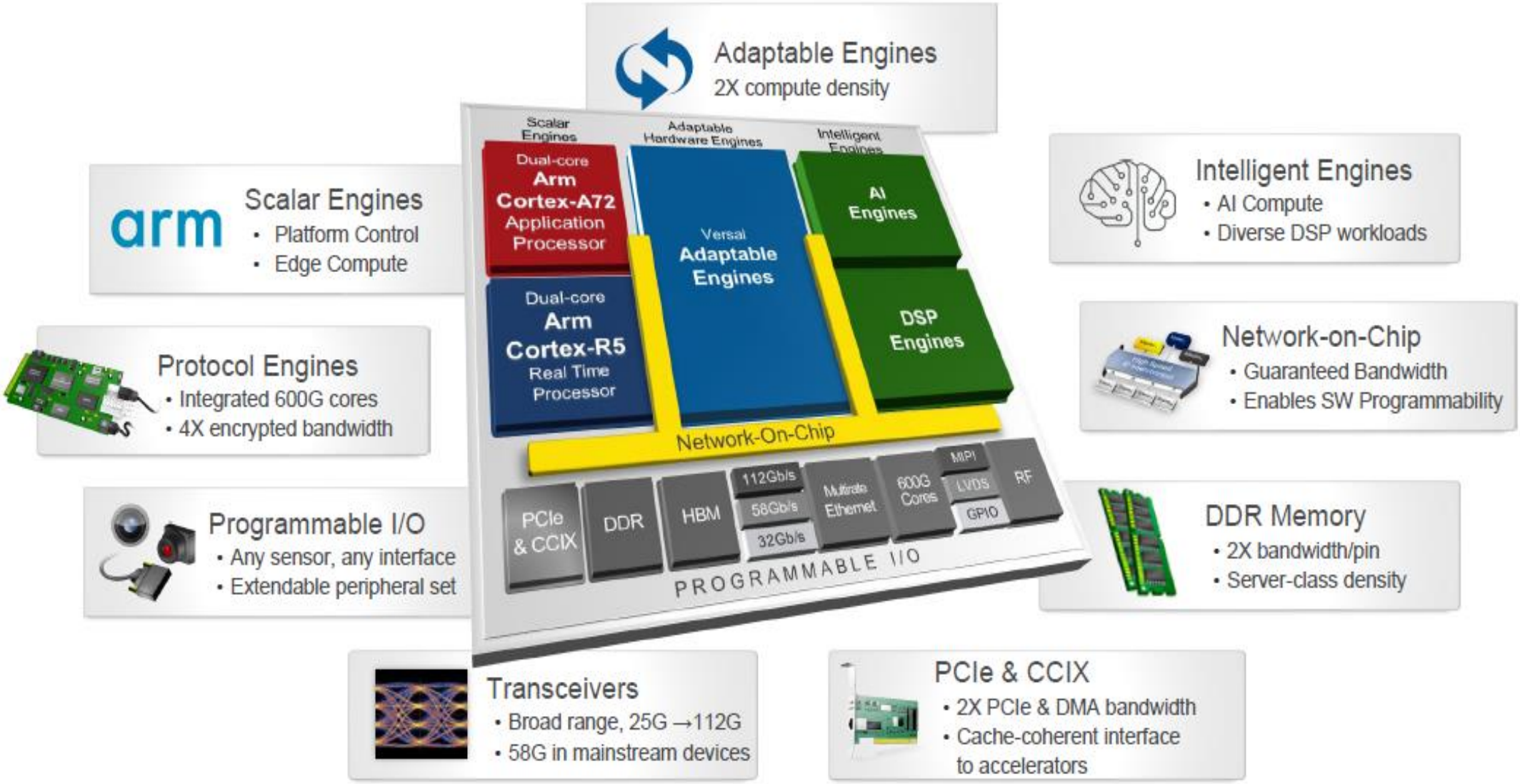
- SRAM-based FPGA, Need a FLASH for boot, Include many DSP blocks
- Very useful for high speed interfaces (HSSL, SERDES…)
- Bring flexibility to boards (reprogrammable)
- Its error rate impose to reprogram it regularly
- Available stock from ADS

Using COTS (commercial) FPGA for Space applications is possible thanks to deep knowledge of radiation effects and skills to implement of the best mitigation strategy at FPGA & Board level

# Zynq UltraScale+

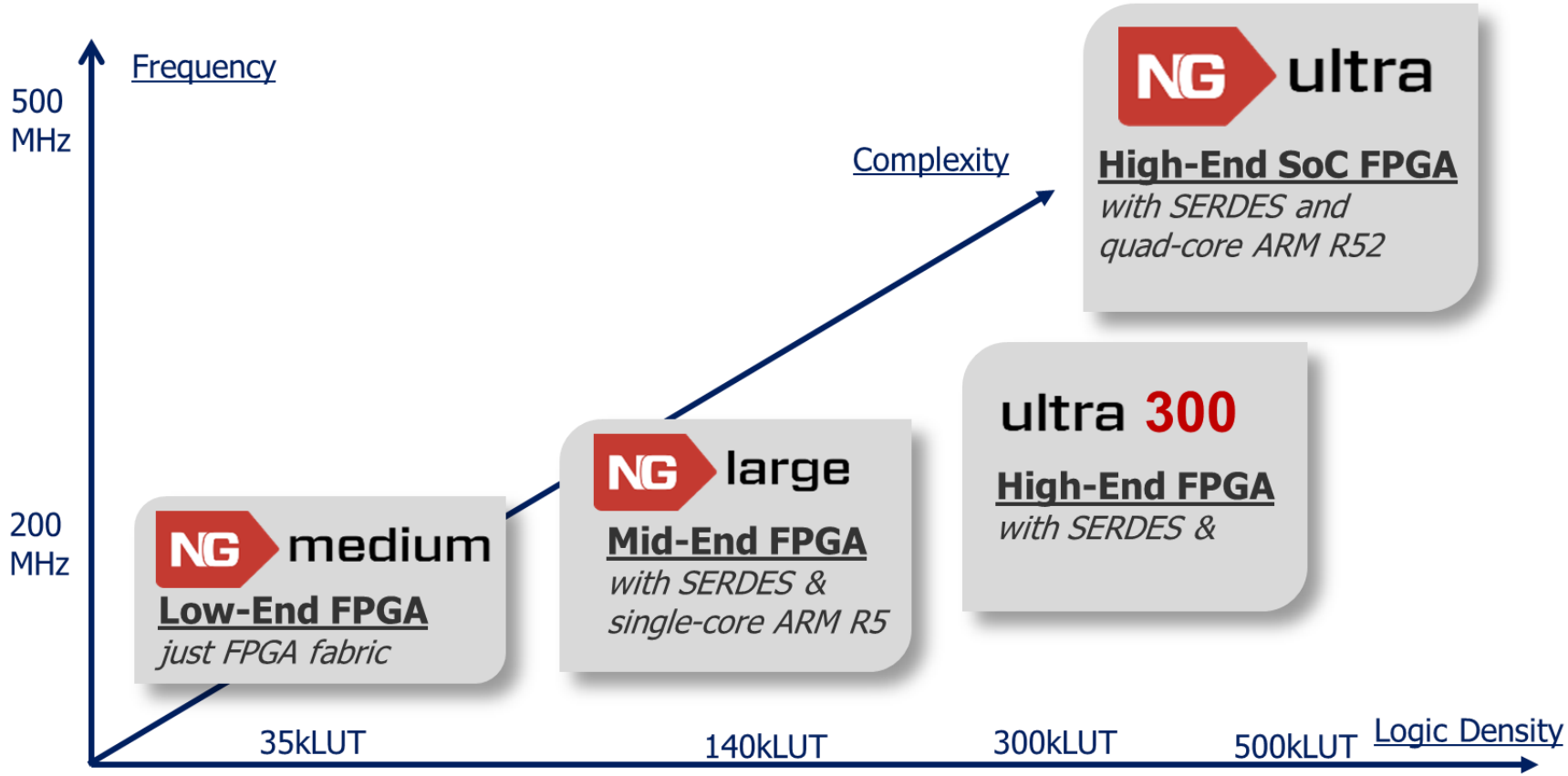


# Versal


Adaptable Engines
2X compute density
Scalar Engines
Adaptable Hardware Engines
Intelligent Engines
Dual-core Arm Cortex-A72 Application Processor
Dual-core Arm Cortex-R5 Real Time Processor
Versal Adaptable Engines
AI Engines
DSP Engines
Network-On-Chip
PCIe & CCIX
DDR
HBM
112Gb/s
58Gb/s
32Gb/s
Multirate Ethernet
600G Cores
MIPI
LVDS
GPIO
RF
PROGRAMMABLE I/O
arm
Scalar Engines
• Platform Control
• Edge Compute
Intelligent Engines
• AI Compute
• Diverse DSP workloads
Protocol Engines
• Integrated 600G cores
• 4X encrypted bandwidth
Network-on-Chip
• Guaranteed Bandwidth
• Enables SW Programmability
Programmable I/O
• Any sensor, any interface
• Extendable peripheral set
DDR Memory
• 2X bandwidth/pin
• Server-class density
Transceivers
• Broad range, 25G →112G
• 58G in mainstream devices
PCIe & CCIX
• 2X PCIe & DMA bandwidth
• Cache-coherent interface to accelerators

# Reprogrammable FPGA used by Airbus D&S

- **NANOXPLORE**
  - **NG-Medium, NG-Large, NG-Ultra**
  - **Ultra-300**



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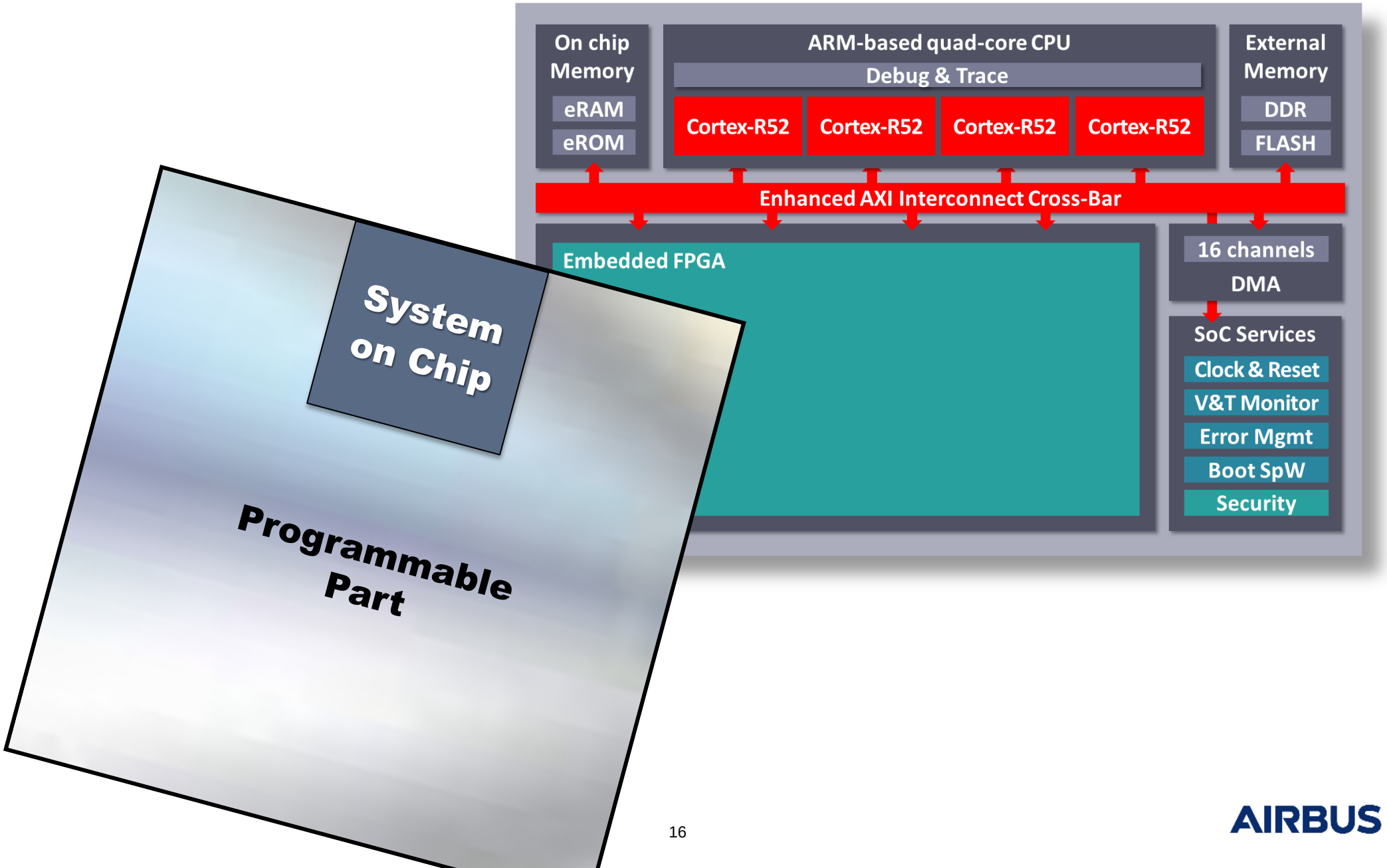
FPGA + SoC

# NG-Ultra → The European Rad-Hard FPGA + SoC



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## The Feedback Challenge

*30 years of FPGA in Airbus in 5 minutes*

## Skills, Process & Development Flow

*Adapting to FPGA evolution… and Pioneering it !*

## What else ?

*Other key topics about how to use FPGA in Space*

## Conclusion

*Not really a conclusion because story will continue…*

# A robust process shall be adapted to the target on which we want to develop

**A robust process shall be adapted to the target on which we want to develop**

**So it’s important to understand the trends driving these targets**

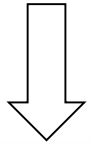
# A long time ago…

*Since their introduction, FPGAs have grown **in capacity** by more than a factor of 10.000 and **in performance** by a factor of 100.*

***Cost** and **energy per operation** have both decreased by more than a factor of 1.000.*

*Advances driven largely by **process technology scaling**, but the real story is much more complex and interesting than simple progression of capacity due to technology scaling.*

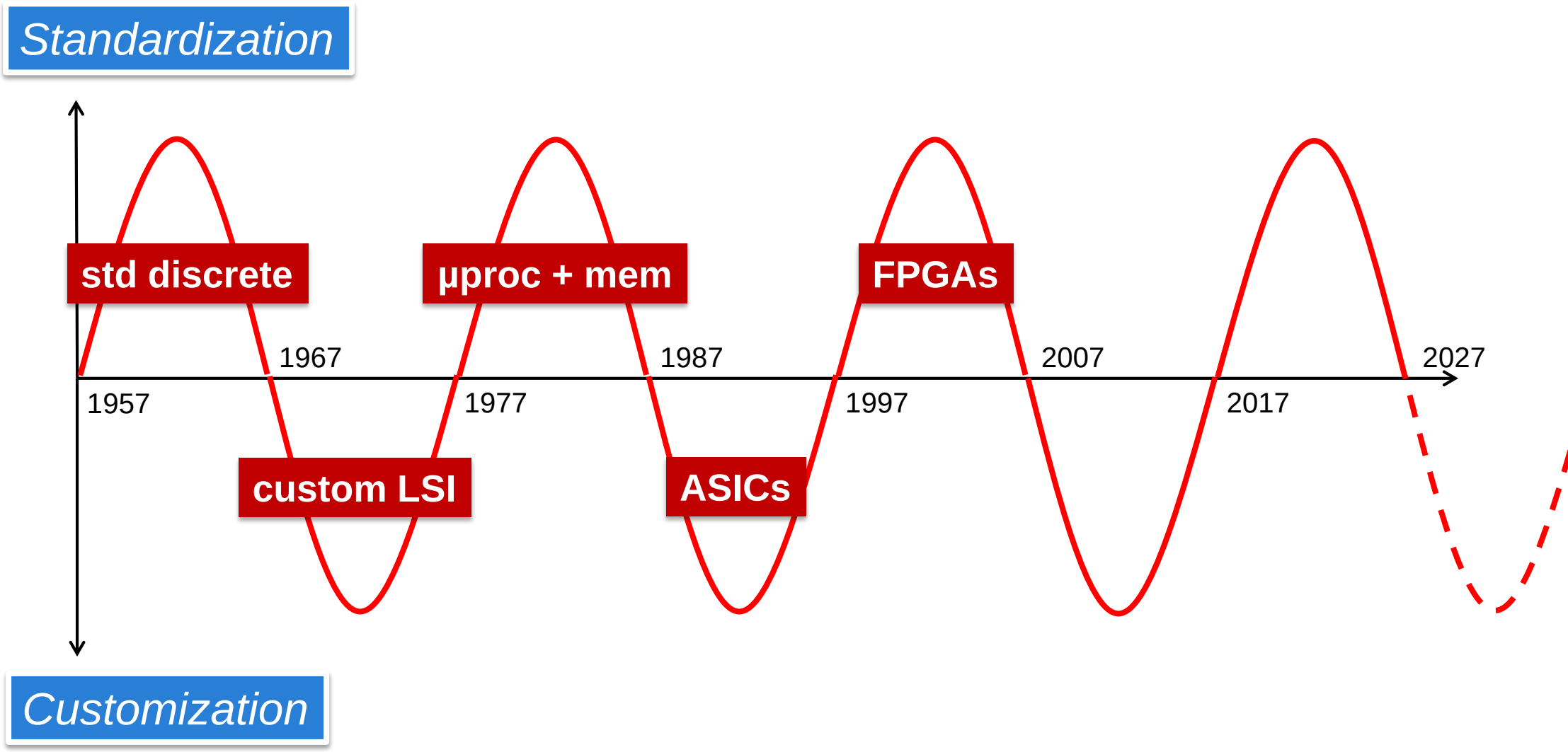
***Quantitative** effects of Moore's Law have driven **qualitative** changes in FPGA architecture, applications and tools*



Qualitative changes means that process technology scaling has not only allowed to have more and more programmable logic / LUTs years after years but also to introduce memories, digital signal processors (DSP), high speed interfaces and now complex multi-core System-on-Chip

(*) Source Steve Trimberger

# ASIC & FPGA trends wave




(*) Source Dr Makimoto



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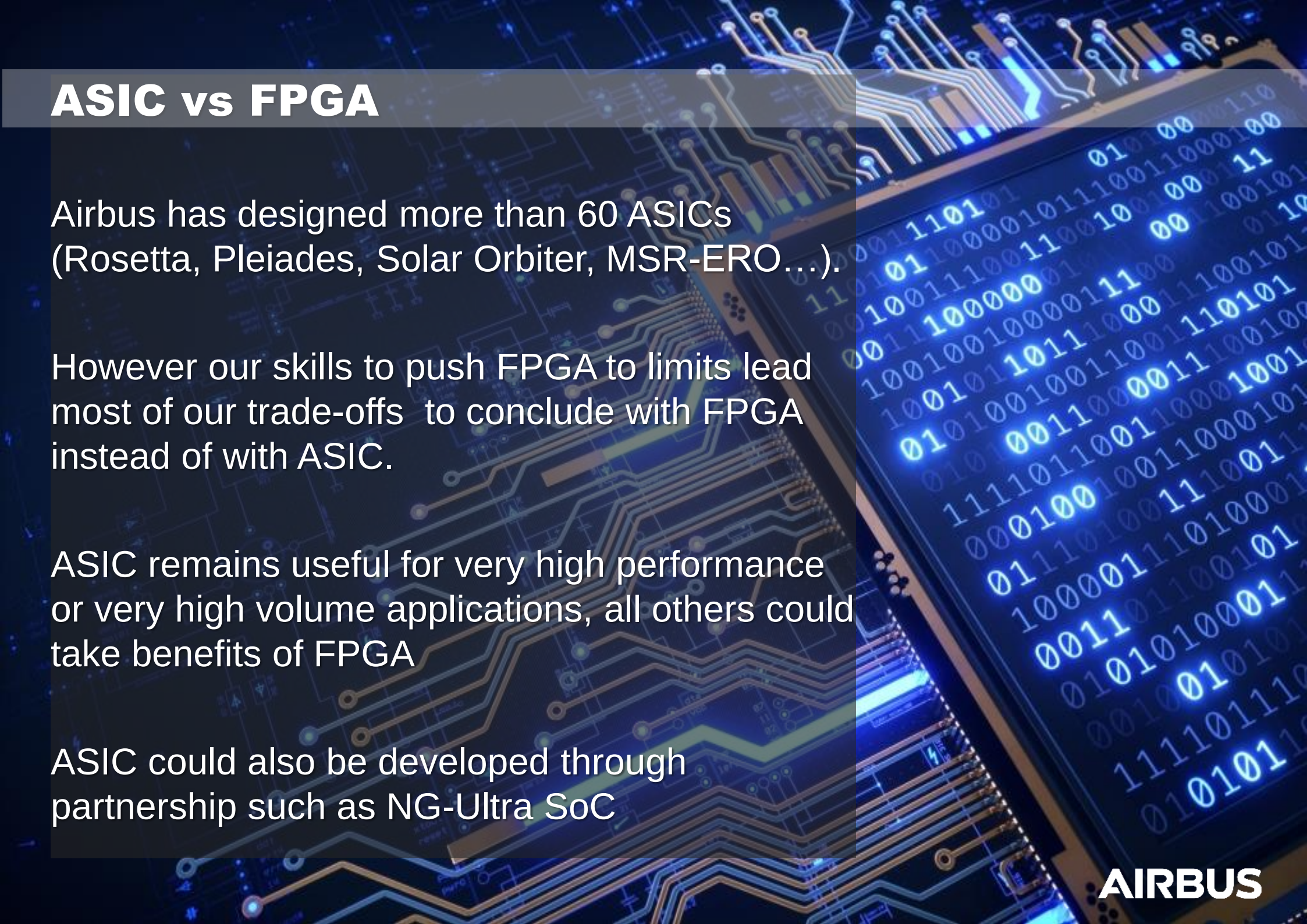
# ASIC vs FPGA

Airbus has designed more than 60 ASICs (Rosetta, Pleiades, Solar Orbiter, MSR-ERO…).

However our skills to push FPGA to limits lead most of our trade-offs  to conclude with FPGA instead of with ASIC.

ASIC remains useful for very high performance or very high volume applications, all others could take benefits of FPGA

ASIC could also be developed through partnership such as NG-Ultra SoC



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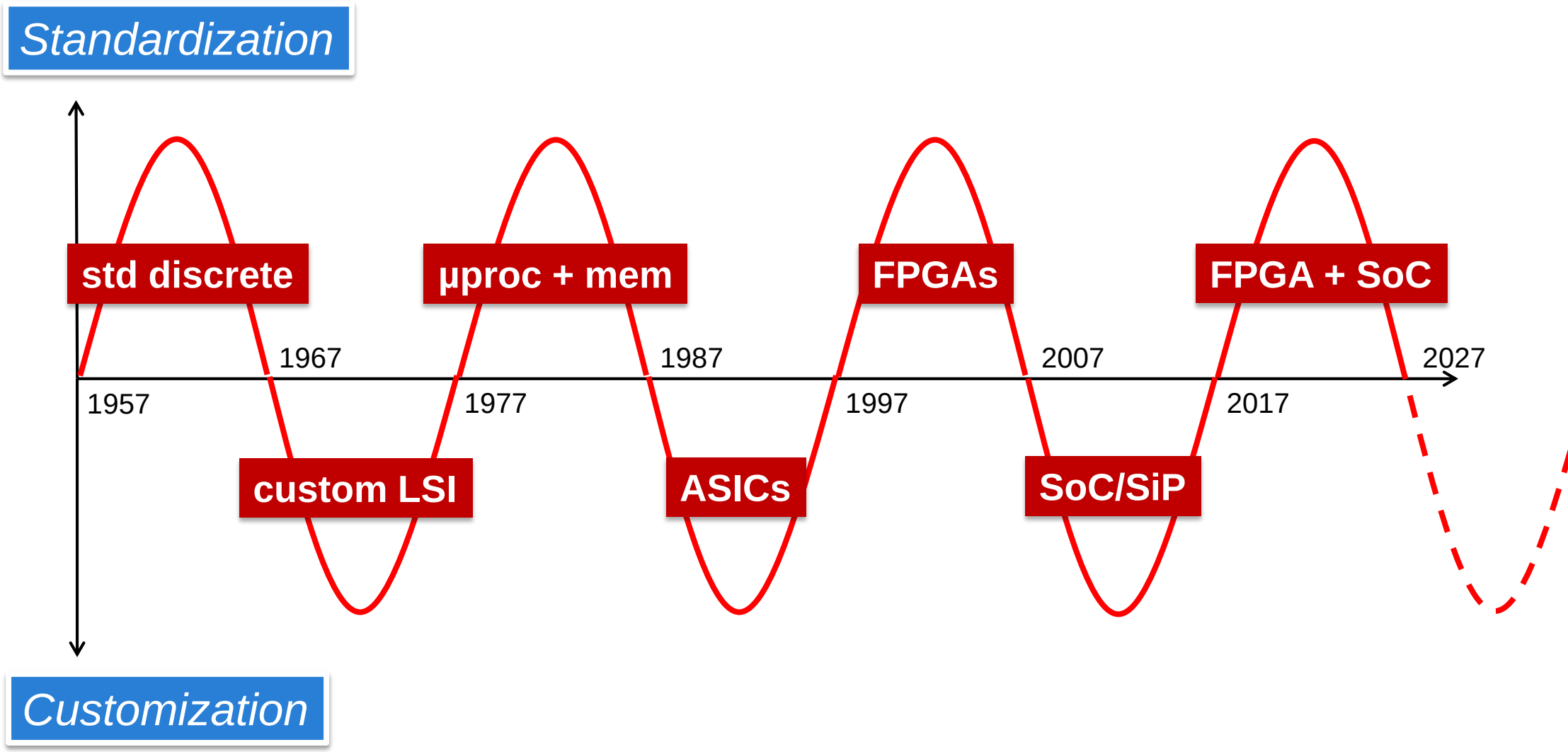
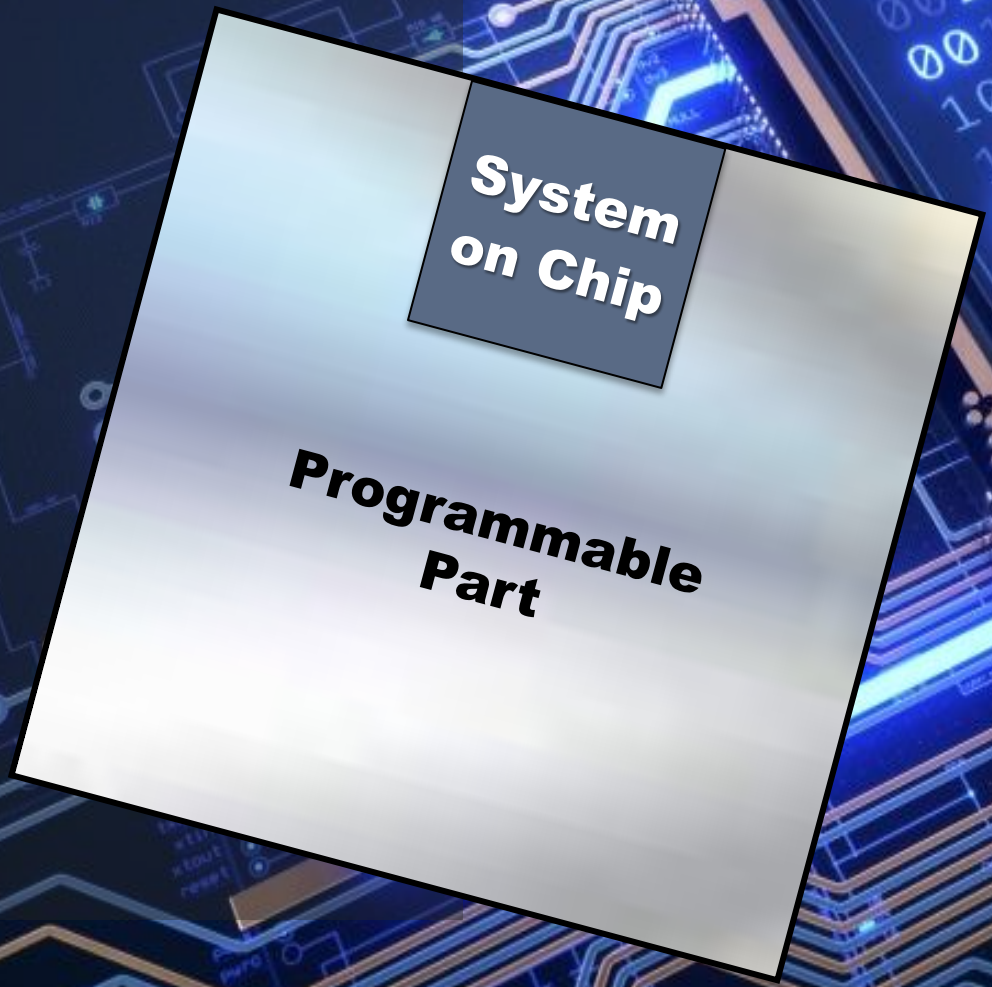



(*) Source Dr Makimoto

# FPGA + SoC

Hardware AND software skills are now required to manage FPGA components

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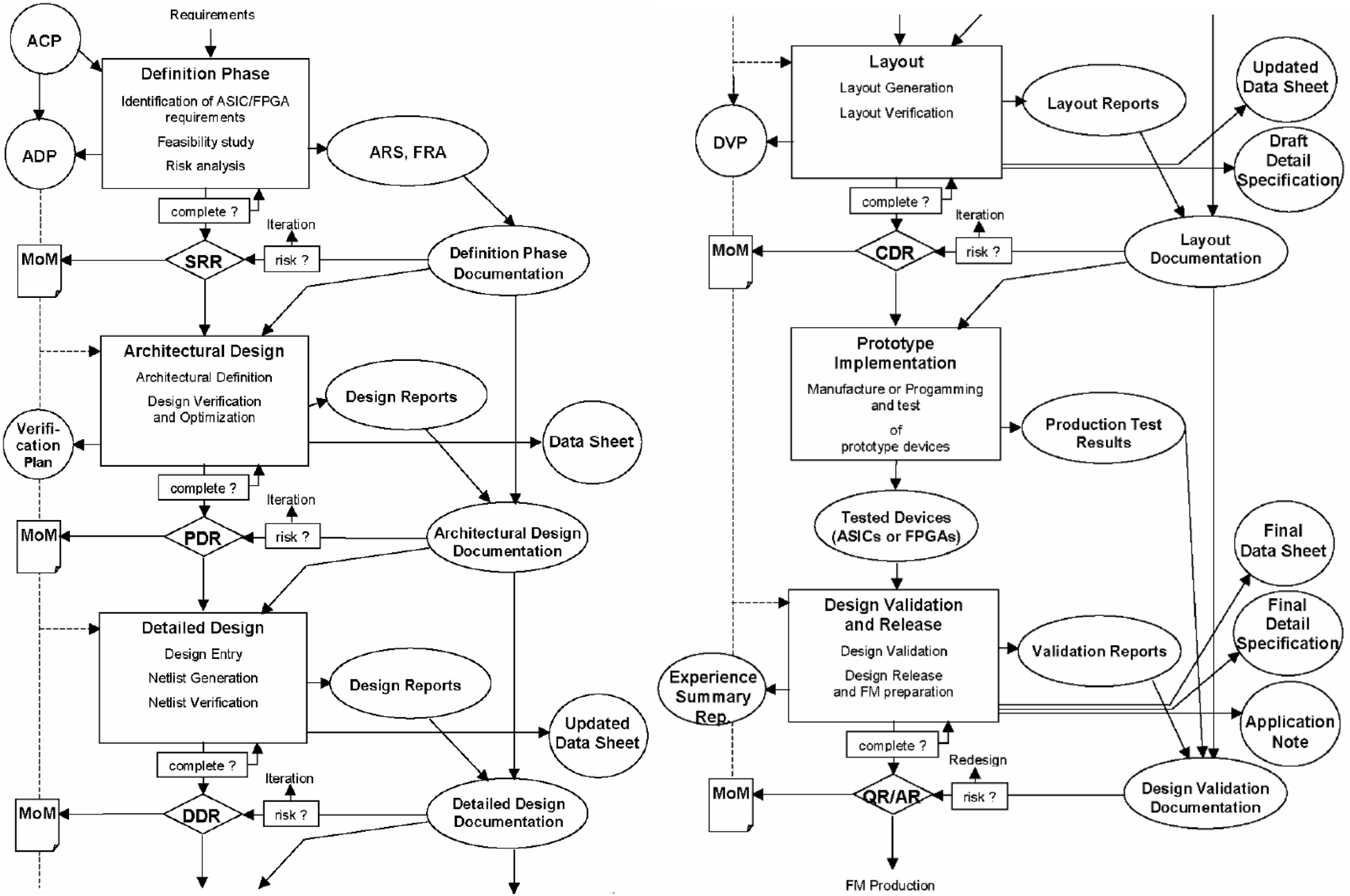
# A robust process shall be adapted to the target on which we want to develop

# Currently one ECSS standard ECSS-Q-ST-60-02C

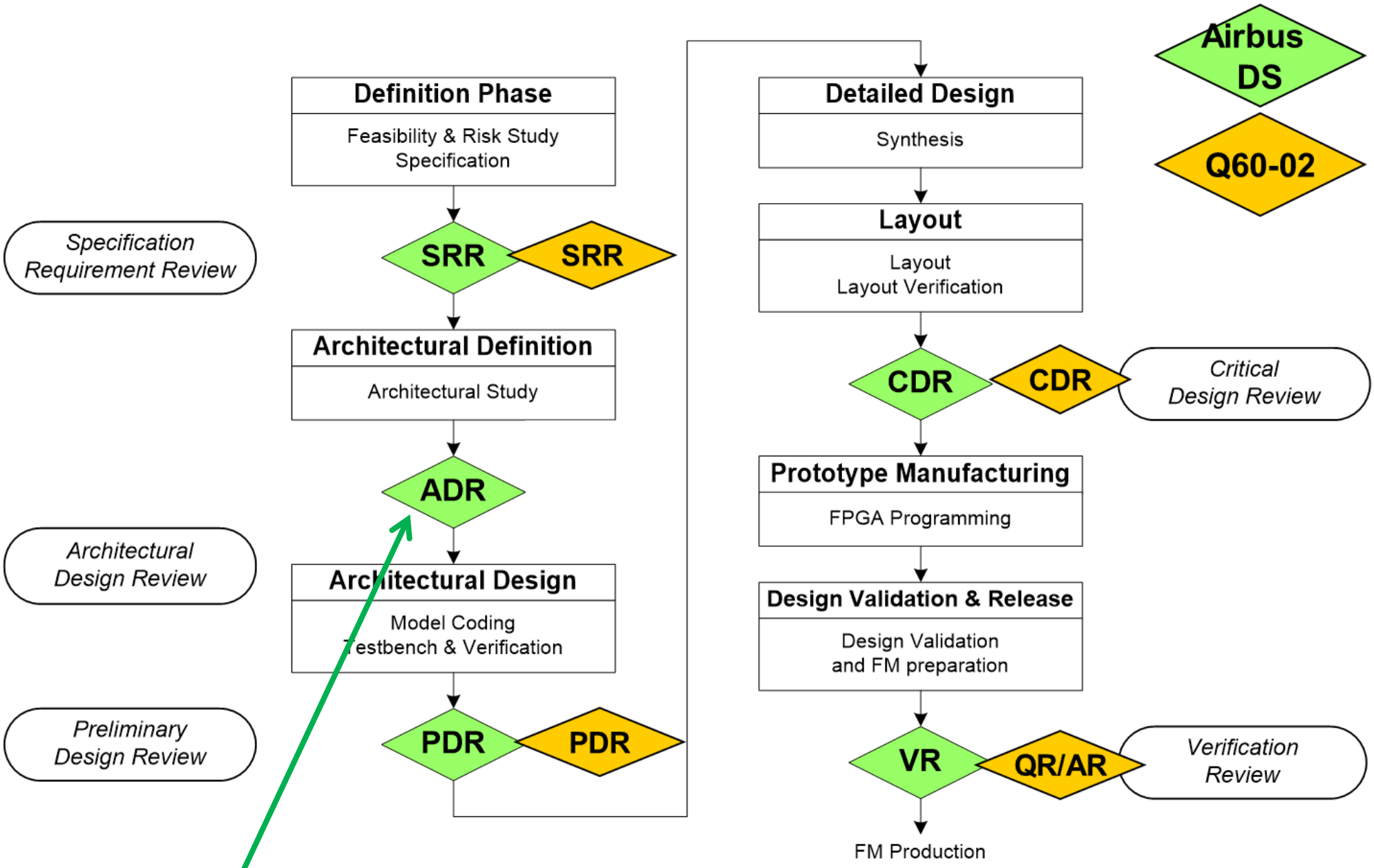
# ECSS-Q-ST-60-02C development flow





# Airbus D&S FPGA development flow






Airbus recommends an additional Architectural Design Review (ADR)

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# Airbus D&S strongly involved in *future* FPGA development flow

Two documents will define this future development flow

- ECSS-Q-ST-60-02C (evolution of previous standard)
- *Space product assurance - ASIC, FPGA and IP Core product assurance*

- ECSS-E-ST-20-40C
- *Space engineering – ASIC, FPGA and IP Core engineering*

- These future standards shall NOT impose quality requirements for FPGA similar to SW quality requirement. It would complicate too much future FPGA developments (already complex !).

# Airbus D&S applicable document : ADS.E.878

## *FPGA & ASIC Design, Validation & Production Requirements*

- Document exposing « good practice » rules and recommandations about clocks, timing domains, resets, state machines, asynchronisms, interfaces, FPGA programming…

- This document is applicable since many years to all internal FPGA developments but also to all FPGA developed by our suppliers
- It really helps to ensure robustness of designs

# Airbus D&S development flow – key points

- Internal process successfully proven on both antifuse and reprogrammable targets since more than 30 years

- ADS has pioneered to be part of FPGA reviews with suppliers (*)
- FPGA experts involved on each review (internal or external)
- Teams can rely on detailed RETEX checklists

- Strong know-how to develop on rad-tolerant and COTS targets, for projects from New Space to CQ1, and now for FPGA+SoC

(*) it has to be reminded that during years, we had very few visibility on FPGA development implemented inside equipement developed by suppliers, FPGA had to be considered as « black box » !

# Design Reuse : IP core management

Take benefits of IP cores is now a key point

- external IPs
- internal IPs
- shared (e.g. SpW-RMAP-Astrium IP on ESA website)



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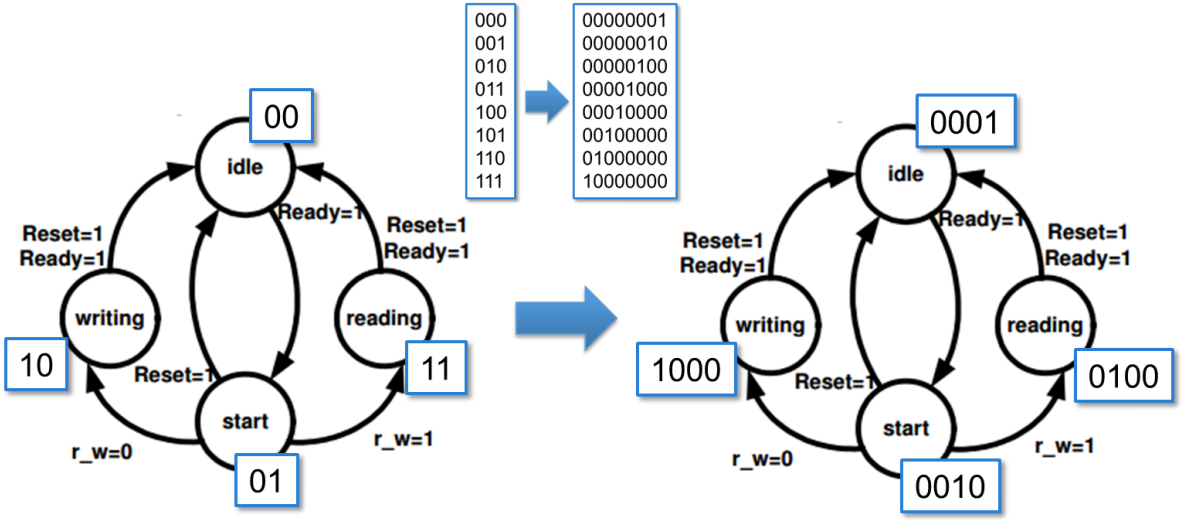
# One last point : “Robust” VHDL Coding !

Robust way of coding, associated to appropriate synthesis constraints, allow to have designs more robust to failures such as SEU.

Examples for FSM design : when others instruction mandatory + onehot encoding



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## The Feedback Challenge

*30 years of FPGA in Airbus in 5 minutes*

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*Adapting to FPGA evolution… and Pioneering it !*

## What else ?

*Other key topics about how to use FPGA in Space*

## Conclusion

*Not really a conclusion because story will continue…*

# FPGA are more complex and diversified than before

It requires

- to master **more diversified development tools**
- to have **complete teams** as we had teams for equipment before
- to put in place a **modular design flow**
- to use **interconnect** for FPGA similar to ASIC interconnect
- to increase interaction between **HW & SW**
- …

It modifies the way of working and importance of some tasks

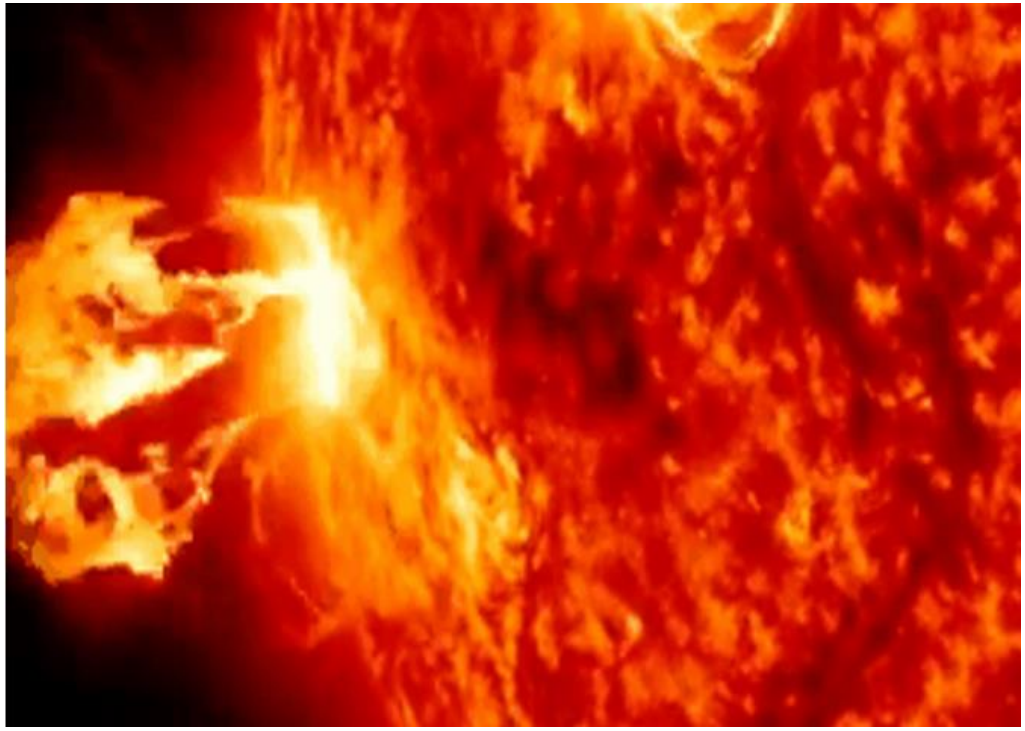
- Verification
- Place & Route
- HW/SW integration
- …

# Mastering a (new) FPGA is not as simple as it could be

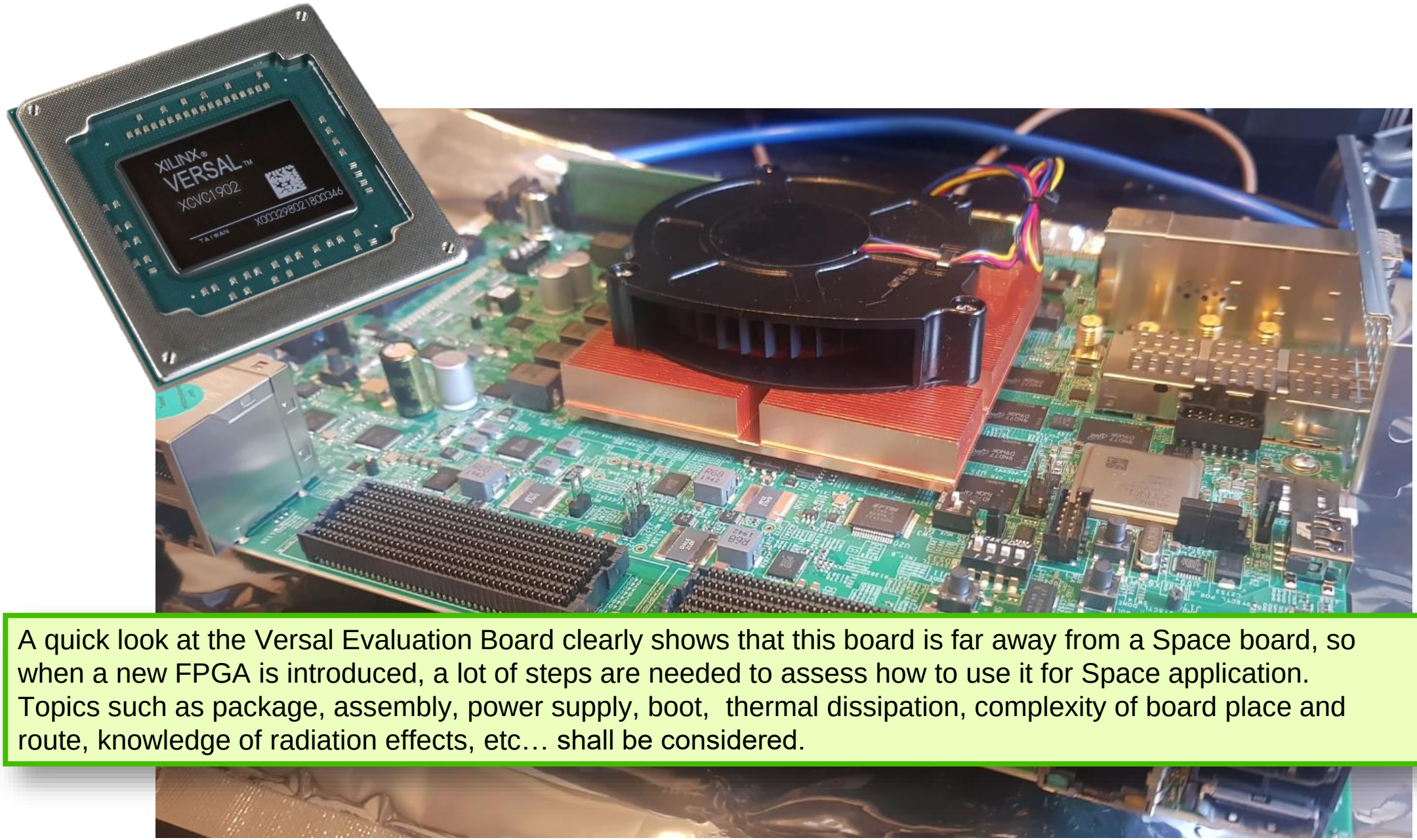
Radiation effects shall be well considered for the design

- (1) clearly know these radiation effects with best accuracy
- (2) establish mitigation strategy (local, global…) and apply it

RETEX is an asset

# Ex : introducing Xilinx Versal




A quick look at the Versal Evaluation Board clearly shows that this board is far away from a Space board, so when a new FPGA is introduced, a lot of steps are needed to assess how to use it for Space application. Topics such as package, assembly, power supply, boot,  thermal dissipation, complexity of board place and route, knowledge of radiation effects, etc… shall be considered.

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# Key messages

- A robust development flow is mandatory, with adaptation according to High Rel or New Space applications
- Introducing a FPGA in a digital board is not only managing FPGA development process but also managing its implementation
- This requires highly skilled teams to manage the global picture

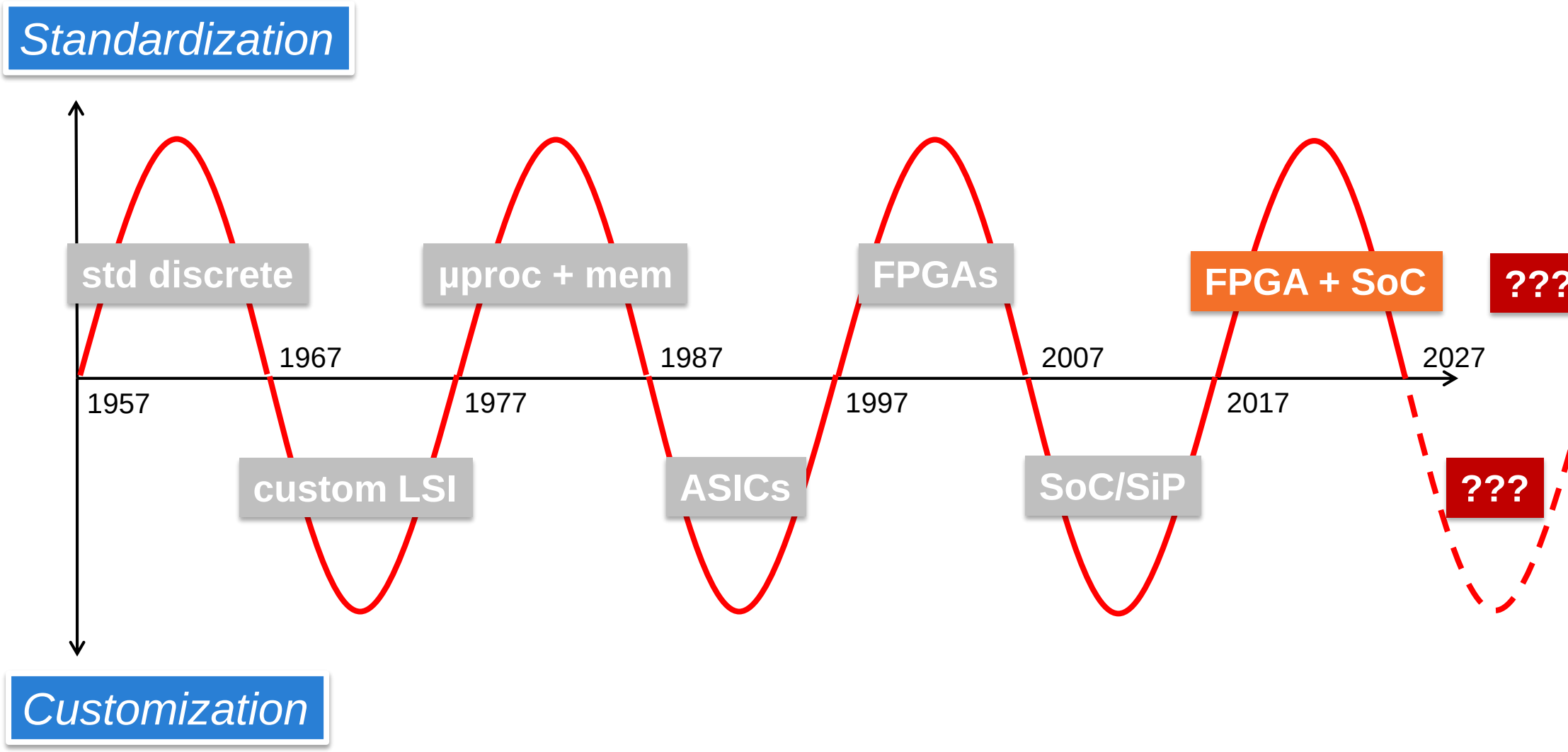
# Key messages

- Airbus has always been able to adapt its way of working and its skills to face the new challenges offered by FPGA evolution

- More than adapting, Airbus pioneered topics around FPGA domain
  - FPGA process improvement initiative
  - Spartan 6 qualification assessment
  - unprecedented performances obtained with RTG4
  - key player for design of the NG-Ultra component
  - …

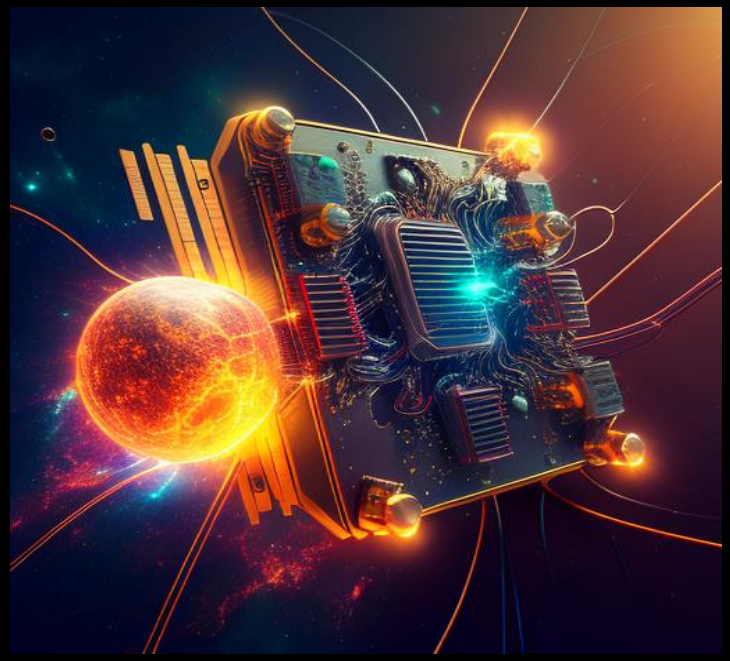
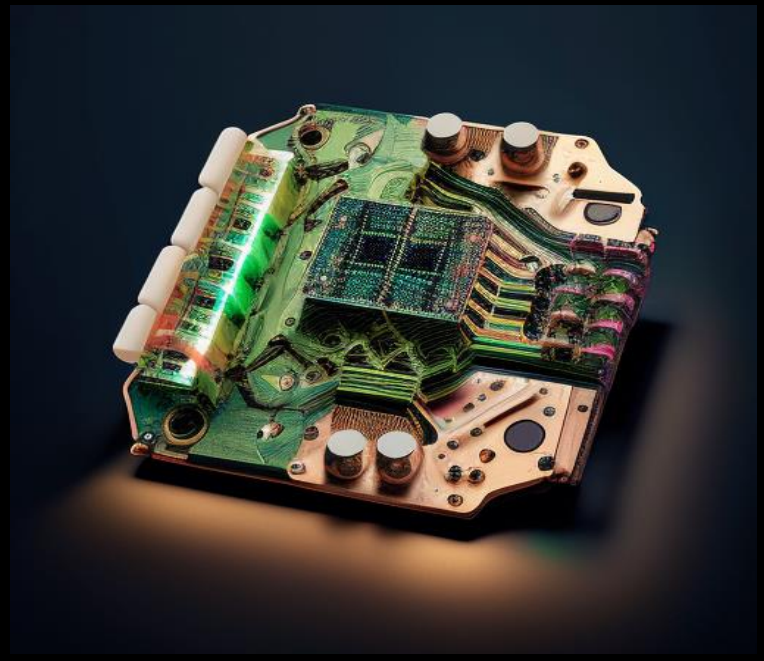
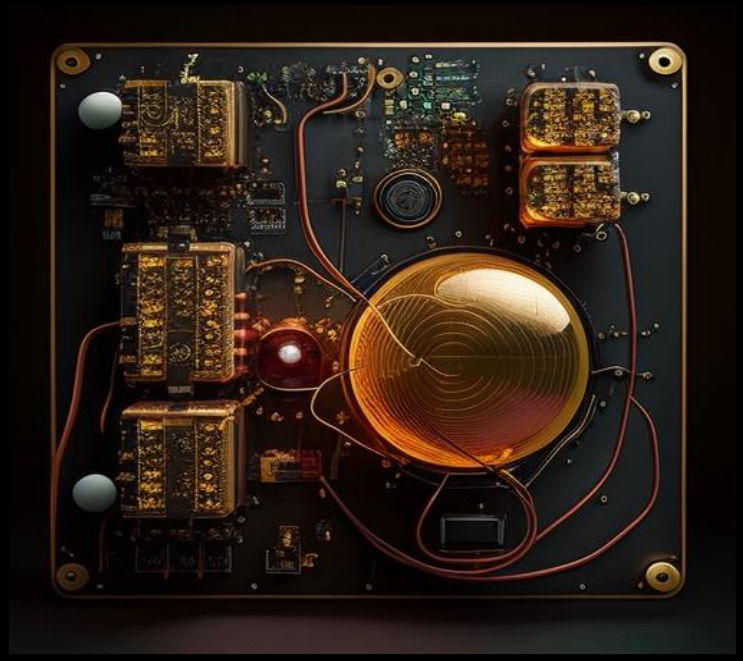
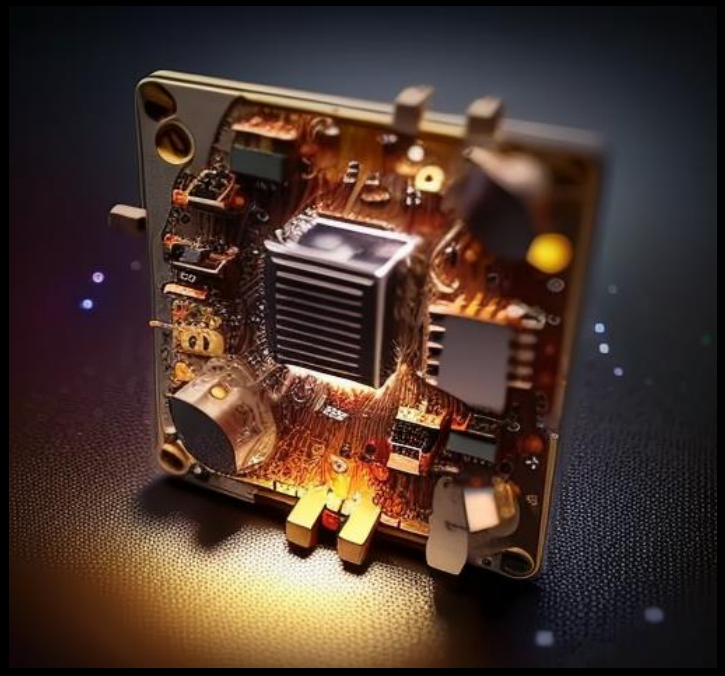
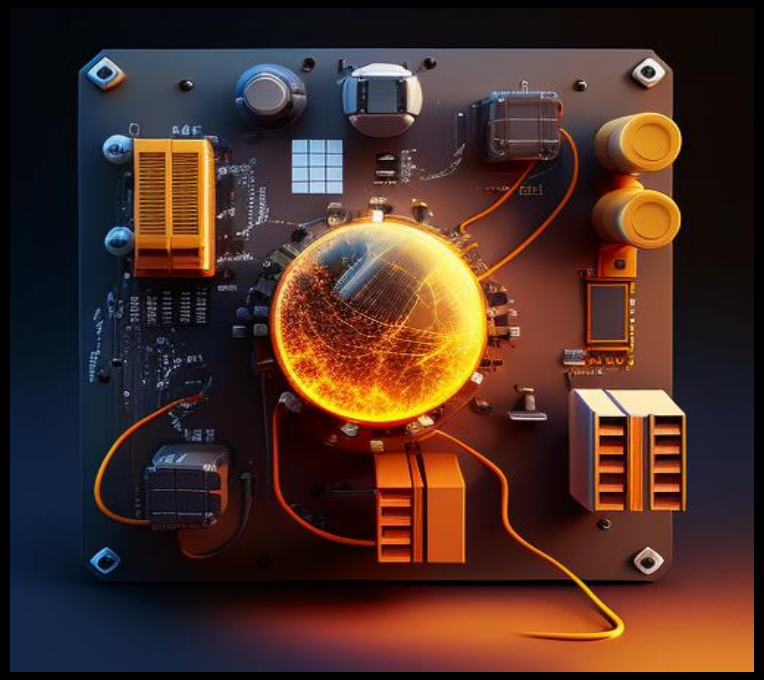
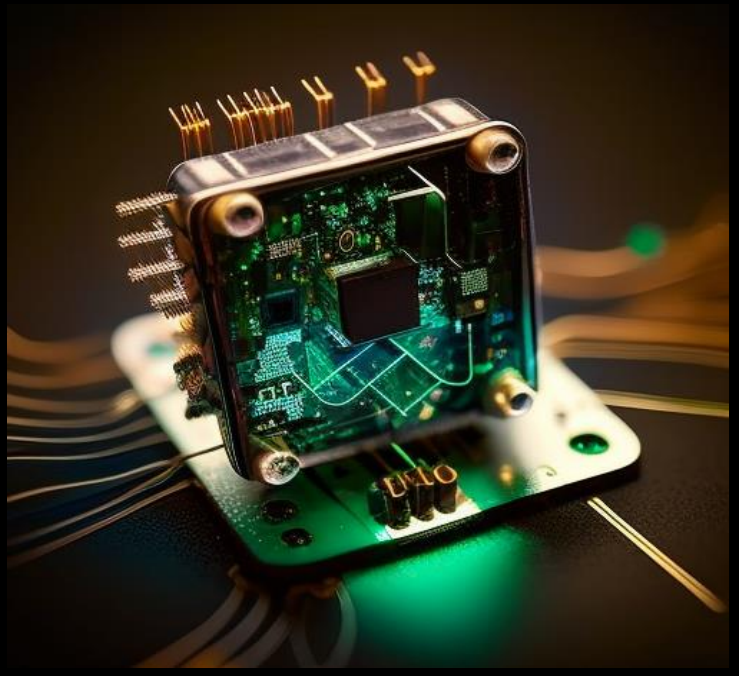
# So, what will be the next step ?

# ASIC & FPGA trends wave




(*) Source Dr Makimoto

# Whatever it will be, Airbus is ready for the next step

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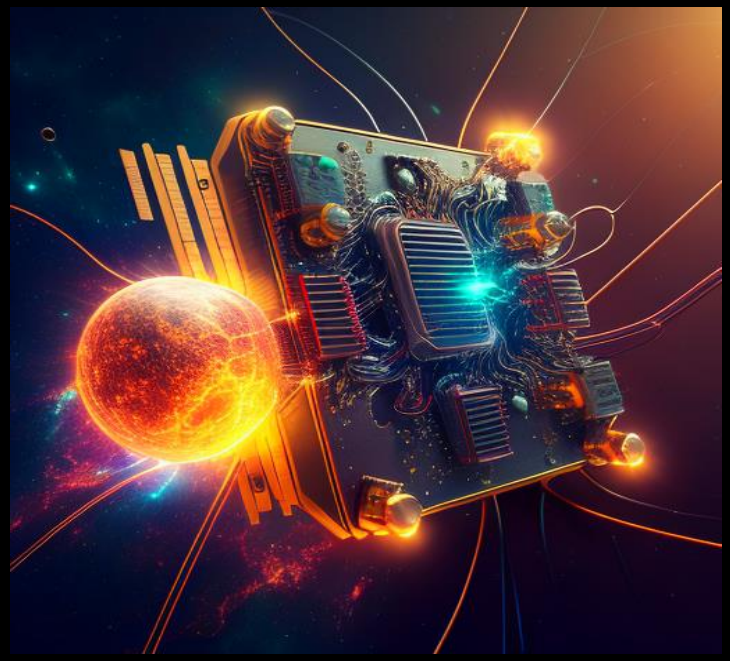
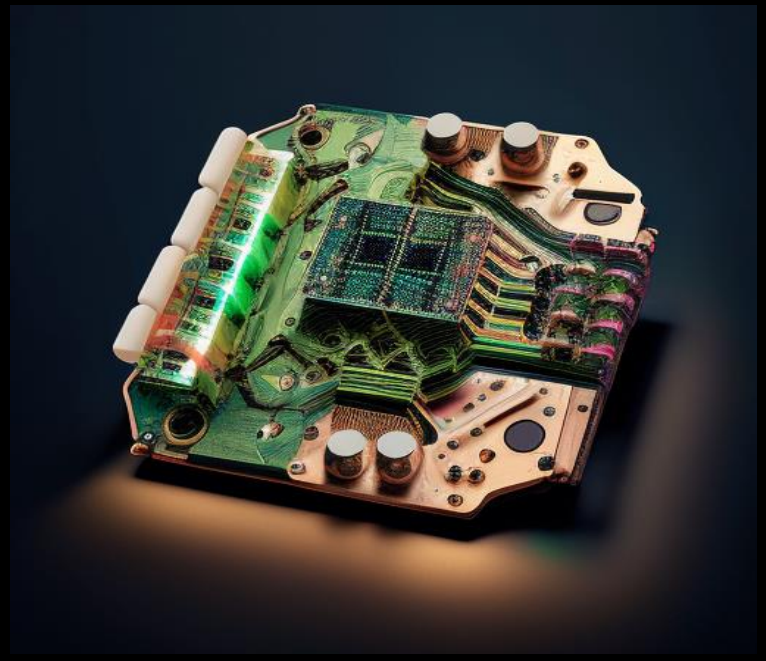
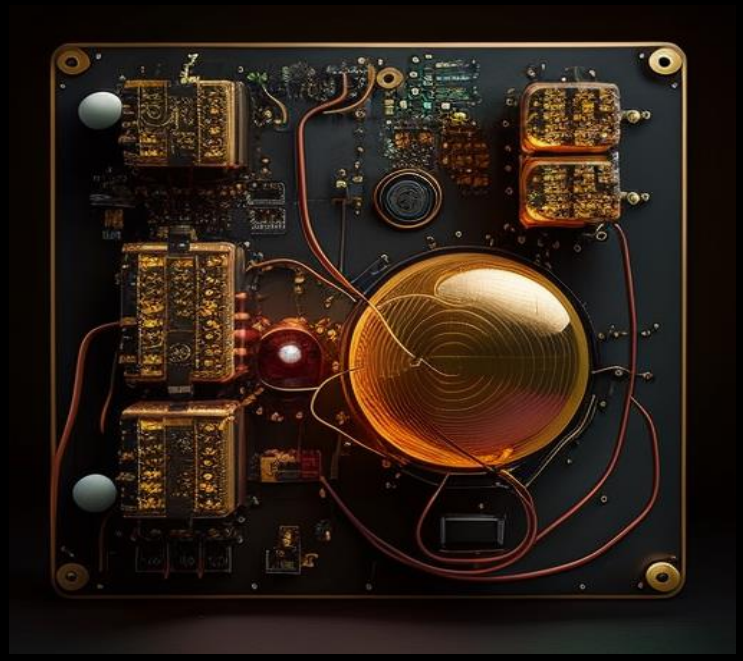
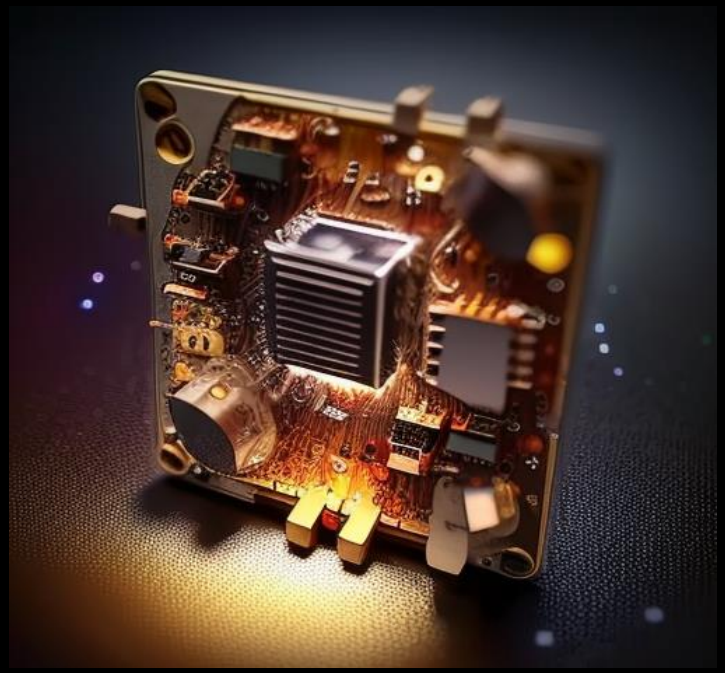
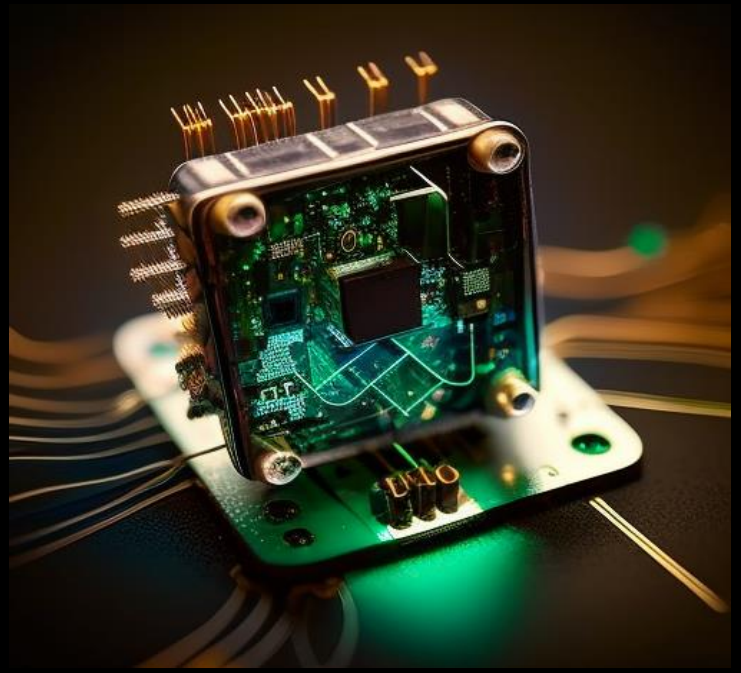
# Questions ?



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