PRACTICAL AND ECONOMIC CONSIDERATIONS FOR IMPROVING THE RELIABILITY OF FPGA-BASED CONTROL SYSTEMS FOR SPACE APPLICATIONS USING A HYBRID DESIGN APPROACH

Introduction

Radiation in space and other extreme environments can have a catastrophic effect on integrated circuits (ICs). HARDSIL® technology mitigates these radiation effects. VORAGO's HARDSIL® technology is an easily implementable add-on module to conventional IC manufacturing processes. HARDSIL® protects integrated circuits from both Single-Event Effects (SEE) and Total Ionizing Dose (TID) degradation. Unlike other radiation-hardening approaches, HARDSIL® does not depend on expensive custom "hardened" cell libraries, exotic materials or non-standard process equipment to harden integrated circuits. HARDSIL® improves radiation immunity without increasing size or power consumption or reducing the performance of the integrated circuit. When extreme radiation immunity is a requirement, HARDSIL® can be combined with Radiation Hardened-by-Design (RHBD) libraries and techniques to provide higher radiation immunity than achievable using either RHBD or HARDSIL® alone.

VORAGO's existing HARDSIL® hardened products have extensive and ever-growing flight heritage in low earth orbit (LEO), geosynchronous/geostationary orbit (GEO), and lunar orbit missions. VORAGO HARDSIL® products have also been chosen as part of the electronics systems in NASA's next-generation space suits.

Although to date, HARDSIL® has been utilized in low-voltage digital and mixed-signal CMOS devices, VORAGO is working with partners to expand the use of HARDSIL® to additional processes and application areas. New target application spaces include Edge Computing using rad-hard Artificial Intelligence/ Machine Learning (AI/ML) architectures and rad-hard high-performance processors, rad-hard Non-Volatile Memory (NVM), and highly- integrated rad-hard Systems-on-Chip (SoCs) and Microcontroller Units (MCUs) fabricated using HARDSIL®-enhanced Bipolar-CMOS-DMOS (BCD) processes to enable on-board high-voltage functionality.

HARDSIL® is implemented using existing baseline process modules and standard foundry process equipment. VORAGO has successfully deployed HARDSIL® in multiple process nodes. HARDSIL® readily scales with process technology and can be applied to both planar and 3-D (FinFET, etc.) structures. VORAGO is currently working with multiple U.S.-based trusted foundries to implement HARDSIL® in planar and FinFET technology nodes to create new rad-hard products and harden existing products without costly re-design. Figure 1 (planar) and 2 (FinFET) provide comparative commercial and HARDSIL® process cross-sections. As shown, the added HARDSIL® structures are next to and beneath the already-existing commercial devices, allowing them to protect these devices without altering their physical structure, electrical behavior and required design infrastructure. This enables retrofitting HARDSIL® to existing designs without changing their electrical characteristics.

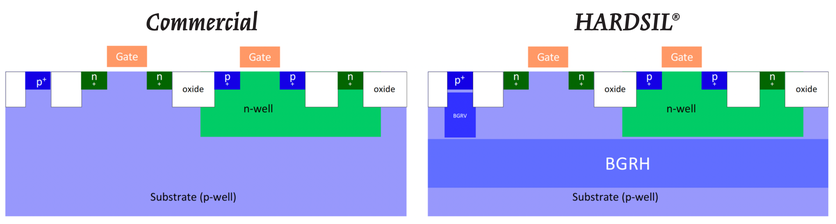

Figure 1: Commercial vs. HARDSIL® for Horizontal Processes

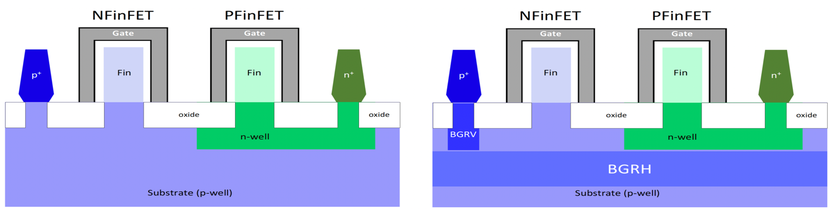

Figure 2: Commercial vs. HARDSIL® for FinFET Processes

Energetic Particle Strikes and Single-Event Effects (SEE)

When energetic particles travel through an integrated circuit, they leave trails of electron-hole pairs in their wake. Some of these electron-hole pairs recombine in the substrate, but a large fraction of charge generated near circuit nodes can diffuse into both directly-struck and nearby nodes, disrupting the operation of the circuit. The size of the affected region and the amount of charge injected into the affected circuit nodes is proportional to the particle Linear Energy Transfer (LET). This generated charge can cause multiple types of single-event effects:

1. ***Single-Event Upset (SEU)*** *- storage nodes holding binary data (SRAMs, Registers / Latches, etc.) can have the data flipped to the opposite value.*
2. ***Single-Event Transient (SET)*** *- a glitch can be inserted into a combinatorial logic data path.*
3. ***Single-Event Latch-up (SEL)*** *- injected charge can trigger cross-coupled parasitic bipolar devices found in all bulk substrate ICs to turn on, creating a self-sustaining low-resistance, potentially destructive short between the power and ground supplies of the device.*

For commercial processes, the area of upset can extend many microns away from the center of the particle strike, making it difficult to mitigate SEU and SET using only design techniques like memory error correction, or cells with multiply redundant critical nodes. For example, Dual Interconnected Cell (DICE) latches.

In comparison, HARDSIL® has been shown to dramatically reduce the area of upset, significantly increasing both the ease of implementation and effectiveness of EDAC and DICE latches in mitigating SEU and SET. Figure 3 shows the measured relative size of upset regions as a function of process and particle LET for devices manufactured on commercial and HARDSIL®-enhanced processes.

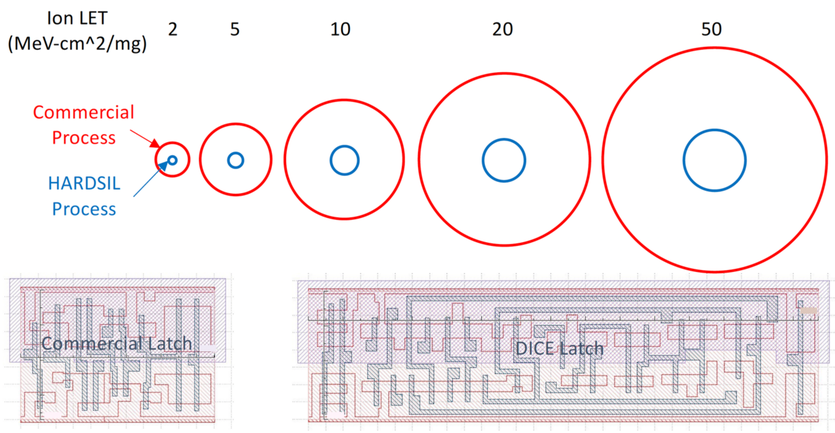

Figure 3: Particle Strike Upset Region vs. Process by Ion LET Compared to Latch Cell Areas

This figure illustrates layouts of commercial and Dual Interconnected Cell (DICE) latches for comparison. As can be seen from the figure, for the commercial process, the region of upset from particles with LET >= 2 MeV-cm^2/mg is sufficient to upset the commercial latch design. Even the DICE latch, when manufactured on the baseline commercial process, has a high probability of being upset by particles with LET
> ~ 5 MeV-cm^2/mg since enough nodes can be simultaneously by the strike.

HARDSIL® exhibits dramatically smaller regions of upset. Conventional commercial latch designs are, therefore, much less likely to be upset by lower LET (< 10 MeV-cm^2/mg) particle strikes and DICE latches will be immune to upset from strikes by even very high LET (> 50 MeV-cm^2/mg) particles.

In addition to improving SEU and SET immunity, HARDSIL® dramatically improves the immunity of the IC to latch-up, regardless of the stimulus (voltage spike, elevated temperature, ionizing radiation or some combination of the three). Figure 4 shows measured electrical latch-up characteristics for the same structure manufactured on both commercial and HARDSIL®-enhanced processes.

HARDSIL® prevents latch-up, evidenced by the lack of any snapback in the HARDSIL® sweeps in comparison to the snapback at the Trigger Point in the curves for the structures fabricated in the commercial process. HARDSIL®'s superior SEL performance has also been directly confirmed through heavy ion SEL testing of various devices and ICs manufactured on HARDSIL®-enhanced processes at multiple foundries.

HARDSIL®-enhanced ICs are not only protected against SEL, they are also capable of operating at higher temperatures than their commercial non-HARDSIL® counterparts. ICs become much more vulnerable to latch-up as the operating temperature rises and the latch-up immunity conferred by HARDSIL® enables HARDSIL®-enhanced ICs to function reliably at high temperature. HARDSIL® devices have undergone extended-duration tests and stresses at temperatures up to 250°C. VORAGO HARDSIL® products are currently being used in high-temperature applications like down-hole drilling.

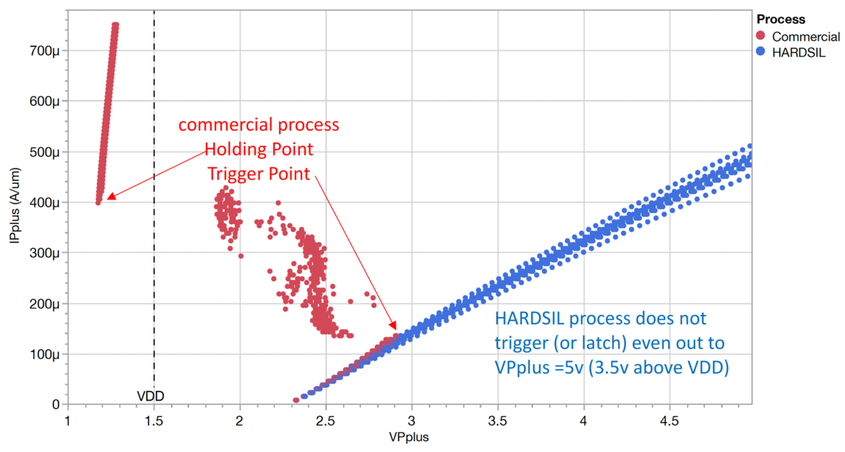

Figure 4: Typical Latch-Up for Commercial and HARDSIL® Enhanced Process at 300 K

Total Ionizing Dose (TID)

When ionizing radiation passes through a dielectric, it generates electron-hole pairs. The electrons are more mobile and, under an applied electric field, some will separate from the holes before the pairs recombine, exiting the dielectric and leaving a surplus of holes behind. Some holes will become fixed positive charge trapped in the dielectric while some will be trapped at the dielectric/Silicon interface. Over the duration of the irradiation, the density of fixed and interface charge rises. The charge build-up is greatest in thick dielectrics, like the dielectric regions intended to isolate individual transistors from each other. Charge build-up in the thick dielectric and at the interface can ultimately activate leakage pathways in the circuitry. This leads to increased power consumption and disrupting the functionality of the device.

HARDSIL® is designed to significantly raise the threshold voltage of the parasitic devices (without altering the characteristics of the active devices). Increasing the parasitic device threshold voltage significantly increases the amount of trapped charge and, therefore, total ionizing dose, required to turn these parasitic devices on. Figure 5 shows the much lower TID induced standby current of a device manufactured on a HARDSIL®-enhanced process in comparison to a commercial process.

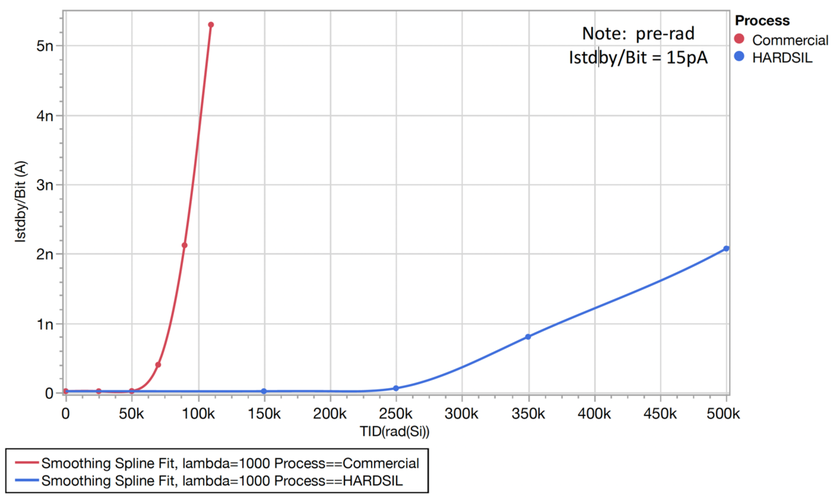

Figure 5: Typical Standby per Bit vs. TID for Commercial and HARDSIL® Enhanced Devices

Adaptability and Ease of Use

Figures 1 and 2 illustrate that the added HARDSIL® structures are external to the transistors and other circuit devices. This allows the existing design infrastructure for the baseline commercial process (layout rules, SPICE models, standard cell libraries, etc.) to be re-used for the HARDSIL®-enhanced version of the process flow. This removes the additional costs and resources required to build and maintain the separate rad-hard design infrastructure to create rad-hard ICs, as is usually necessary for Radiation-Hardening-By-Design (RHBD) and other RHBP methods. Figure 6 shows how the commercial design infrastructure is used with HARDSIL® to create a rad-hard product. It also shows that the same IC design can be manufactured with the standard baseline process flow to create a Commercial-Off-The-Shelf (COTS) IC and with the HARDSIL®-enhanced flow to create a radiation-hardened version of the IC with the same functionality. This makes designs portable between commercial and rad-hard flows. Implicitly, Figure 6 also shows that pre-existing designs can be hardened once the HARDSIL® process modules are installed in the semiconductor fab since additional HARDSIL® mask layers can be generated from the pre-existing design database. This can significantly accelerate the creation of rad-hard versions of commercial ICs with desirable functionality without the expense and delay of re-designing each individually.

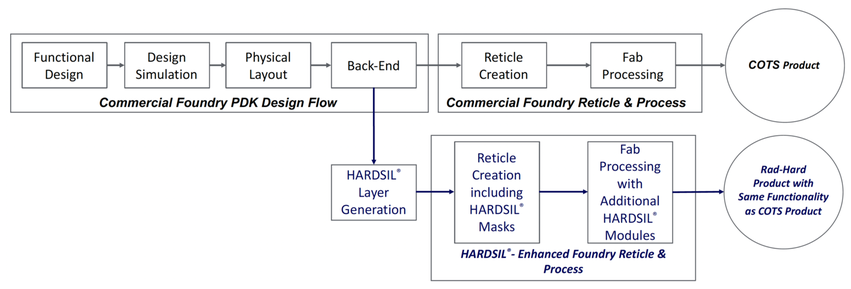

Figure 6: Example High-Level IC creation flow showing the use of the same design infrastructure to create both standard commercial and rad-hard products and the ability to manufacture the same IC in both commercial and rad-hard versions

Conclusion

The HARDSIL® process modules can easily be implemented in conventional wafer fabs to create rad-hard products and products capable of operation at high temperatures with only these simple additions to the commercial process. It is effective across various lithographic nodes, including FinFET nodes. The physical HARDSIL® structures allow the re-use of existing design infrastructure, decreasing the cost of implementation and time to IC creation. The applicability of the existing design infrastructure enables retrofitting of HARDSIL® to existing COTS products, providing hardening without altering functionality. HARDSIL® application areas are expanding to address areas like rad-hard Edge Computing, high functionality SoCs and hypersonic applications.

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