SEFUW: SpacE FPGA Users Workshop, 5th Edition

Tuesday, 14 March 2023

Design Flow - Erasmus High Bay (12:00 - 12:50)

-Conveners: Alberto Urbón Aguado; Florent Manni

time	[id] title	presenter
12:00	[5] Getting Started with OSVVM, VHDL's #1 Verification Methodology (SynthWorks Design)	Mr LEWIS, Jim
12:25	[37] Verification of a CCSDS121-based data compression IP core through fuzzing (U. Palmas de Gran Canaria / U. Autonoma Barcelona)	SANCHEZ, Antonio J.

Thursday, 16 March 2023

Design Flow - Erasmus High Bay (14:25 - 15:15)

-Conveners: Alberto Urbón Aguado; Florent Manni

time	[id] title	presenter
14:25	[18] UVVM: A game changer for efficient FPGA verification and good FPGA quality (EmLogic)	TALLAKSEN, Espen
14:50	[23] Verification Strategy of Multi-FPGA Systems (Airbus CRISA)	Mrs HIDALGO, Isabel