Lessons learned for SDRAM testing

QEC Final Presentation Days 2023

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26/06/2023

Context

IPN 506: “Stuck bits in SDRAMs observed in-flight on several spacecraft”, raised in March 2018.

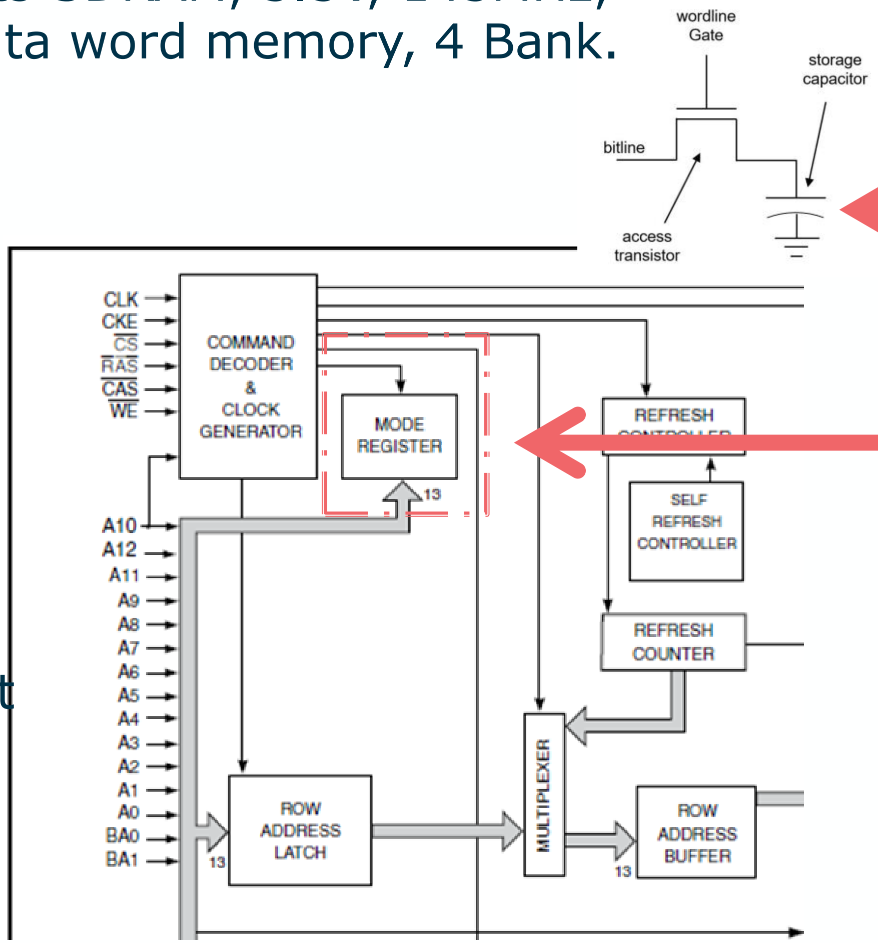
Stuck-bits (SB) and Intermittent Stuck-bits (ISB) have been detected in orbit in several missions. Impacted memory: ELPIDA EDS5104ABTA.

Investigation of radiation effects on the ISSI SDRAM. Parts were provided from two lots by 3D+.

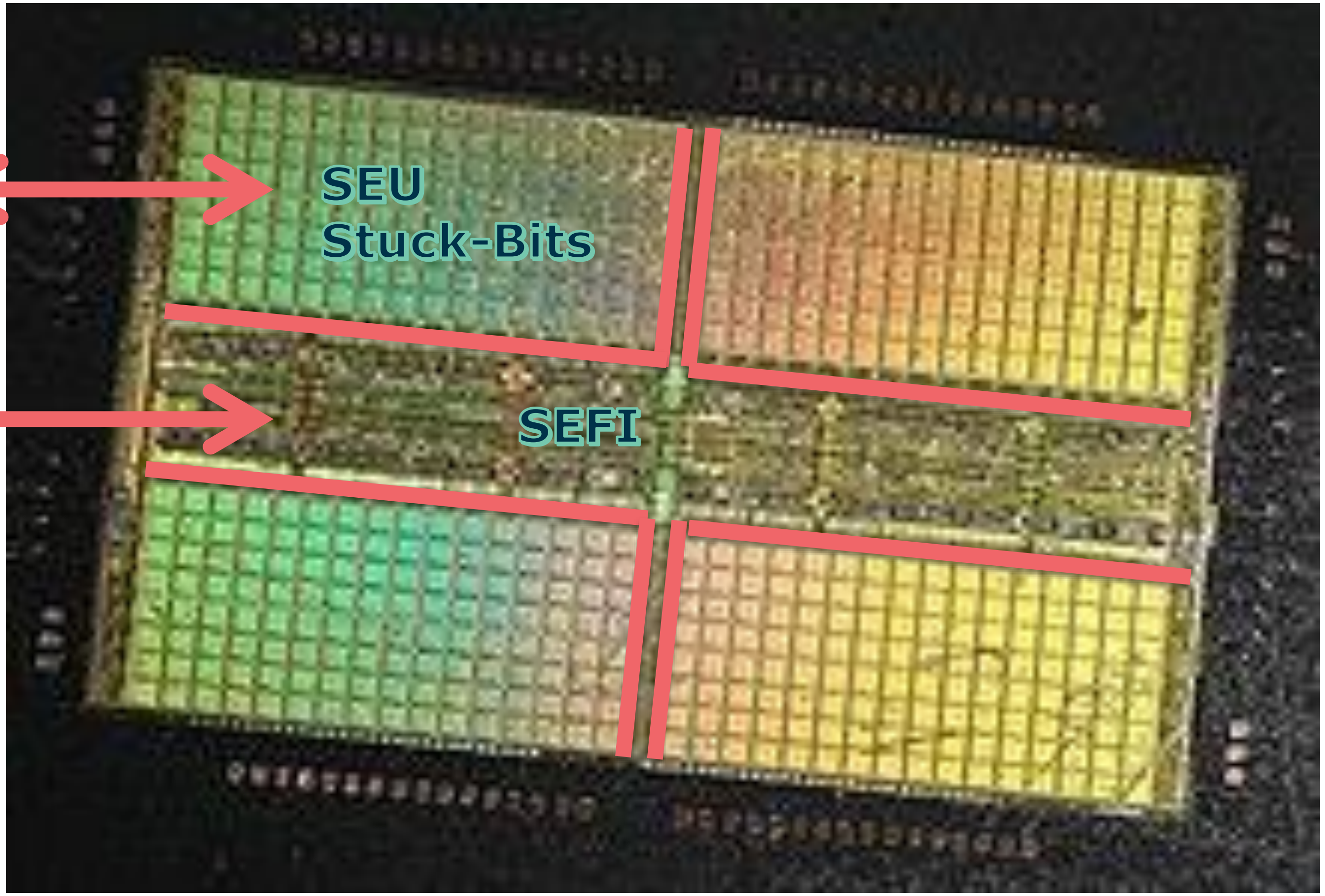
Outcome:
- Testing guidelines.
- SEE (SB/SEU/SEFI) sensitivity screening of the ISSI SDRAM.

Functional block diagram

512Mbits SDRAM, 3.3V, 143MHz,
8-bit data word memory, 4 Bank.



ISSI
datasheet



Die example of a Samsung SDRAM

Stuck-bit, SEU/MCU/MBU, SEFI detection can be all implemented in the same test routine.

DRAM Retention Time (RT)

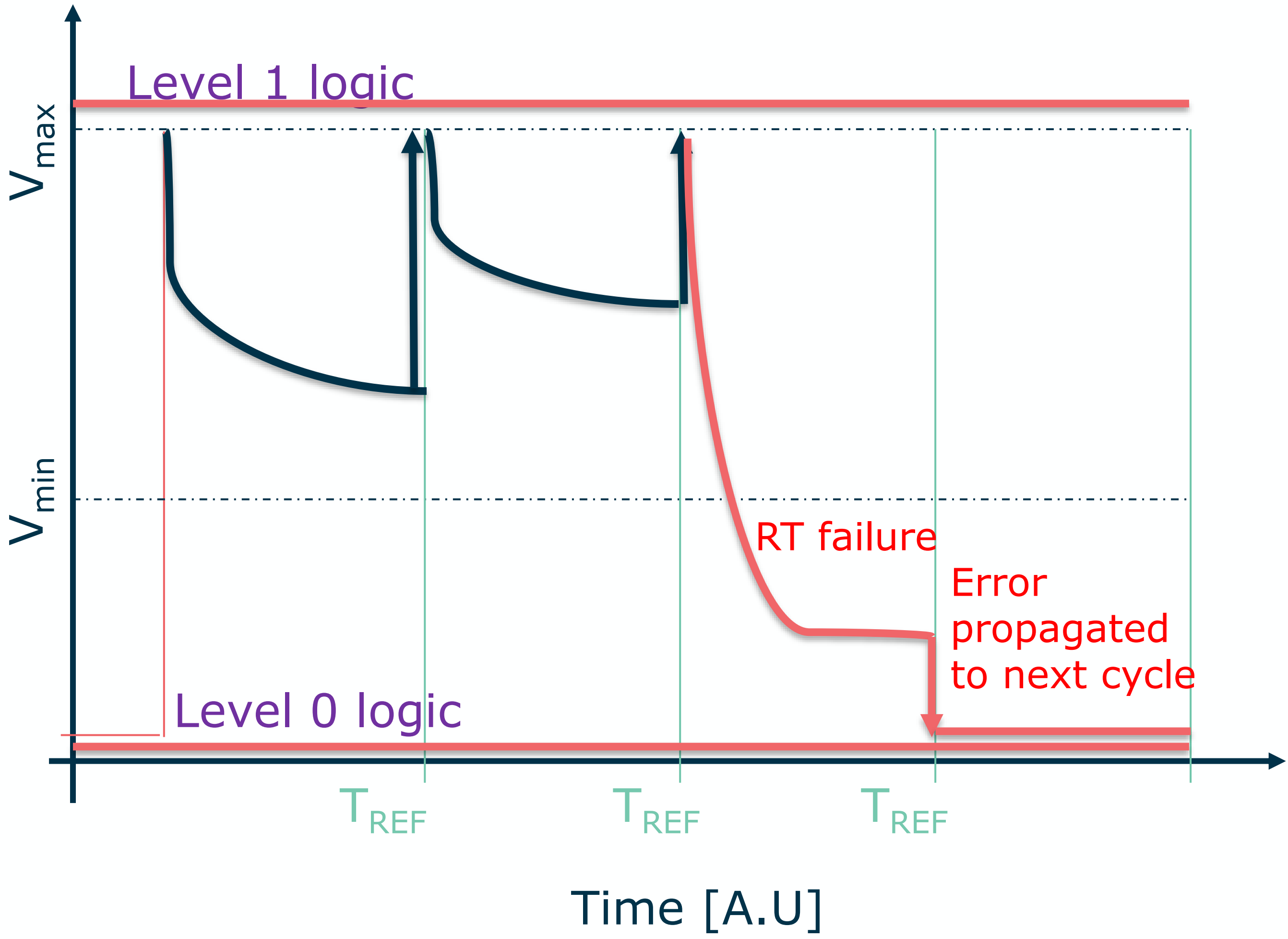
If the bit's RT gets lower than the refresh period, an error occures at the next refresh cycle.

If not cleared, risk of events accumulation and impact at system level.
Scientific data corruption, telemetry saturation, reset..

Self-refresh will only perpetuate the error.

Error is cleared if:
- Memory content is re-written, but subject to error if persistent .
- Discard the faulty row/bit.
- An EDAC strong enough is implemented.

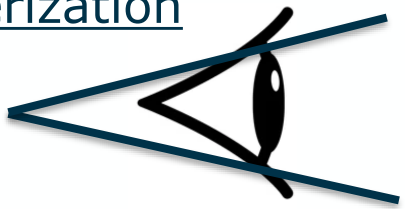
Except specified otherwise, stuck-bits here are given for a RT_{TH} of 64ms and ambient room temperature.



Abstraction level vs technology information

Problem: Different technologies, proprietary information.
How to construct an efficient testing strategy independently of the DRAM tested.

<u>High level characterization</u>



- Temperature
- Retention Time screening
- Pattern
- Irradiation source
- In-situ measurement follow-up

SW/HW interface

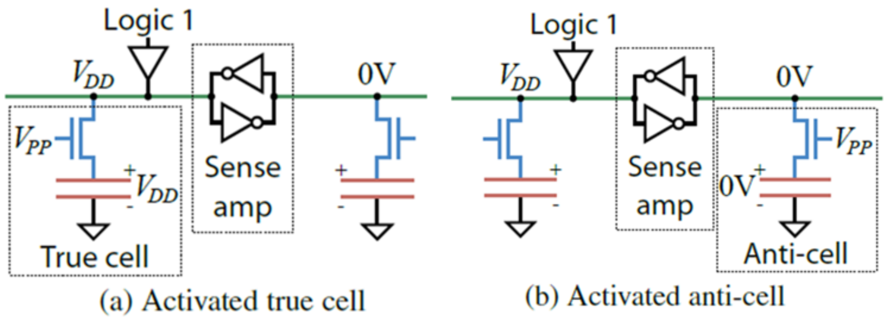
Logic

Devices

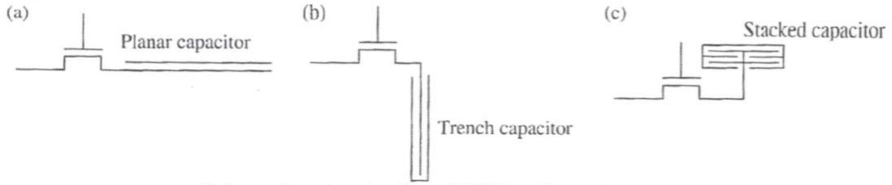
Electrons

-> SB rate for a given mission.

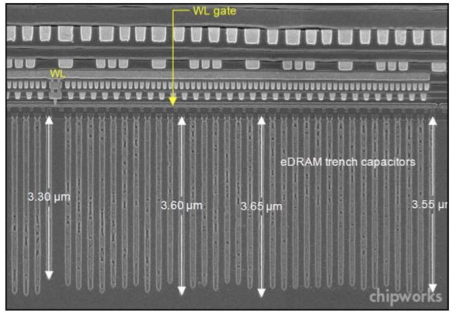
-> Will my EDAC be strong enough?



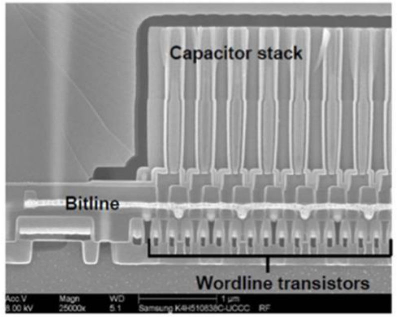
J. Liu, ISCA 2013



Schematics showing three DRAM cell structures



Trench structure capacitor (IBM)



Stacked structure capacitor (Samsung)

What factors influence the Retention Time - Reliability

Non exhaustive list of parameters.

1) Temperature
   - When temperature rises, SB count will rise too.

   -> Importance to test at your operating temperature.

2) Manufacturing process
   - Margin to the 64ms threshold **can be of a few hundreds of ms** to few seconds.

   -> Importance of pre-screening parts.

3) Inter-cell interference
   - A bit ability to store its information is by its bit's content **and** neighbouring write/read operation.

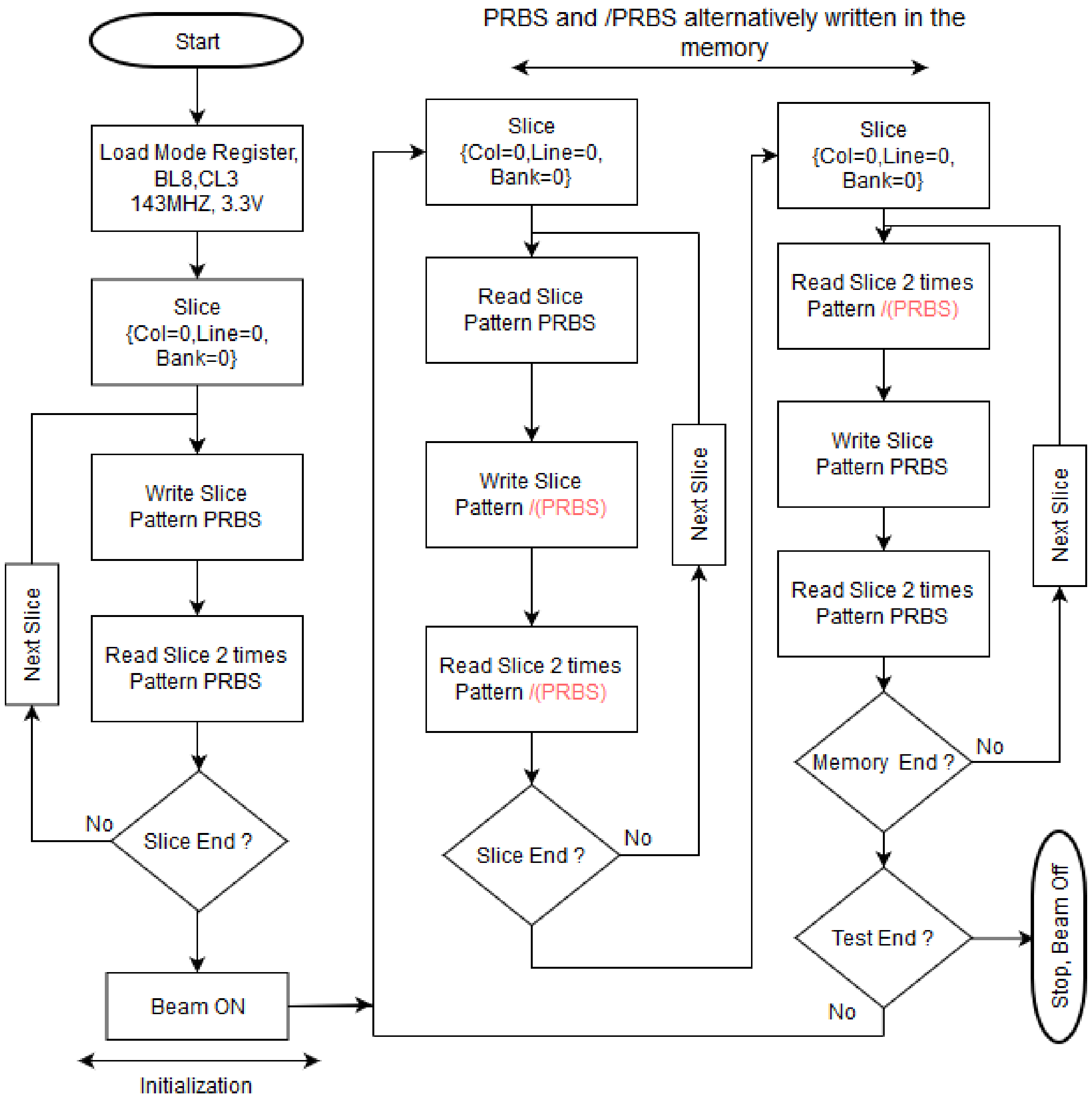
   -> Importance of testing different pattern, search for the worst case pattern.

4) Radiation
   - TID/Proton/Heavy-Ion are all found to create stuck-bits. They are observed in space and in ground experiment.

Dynamic sliced algorithm using a PRBS pattern Beam On

- Going through the whole memory.
- Per slice of 100 lines.
- Repeated write/read operation to trigger and catch SEFIs.
- PRBS and /PRBS pattern alternatively written in the memory.

Daughter Board   Cables, 2 * 1.5m   ATE   Ethernet cable   Laptop



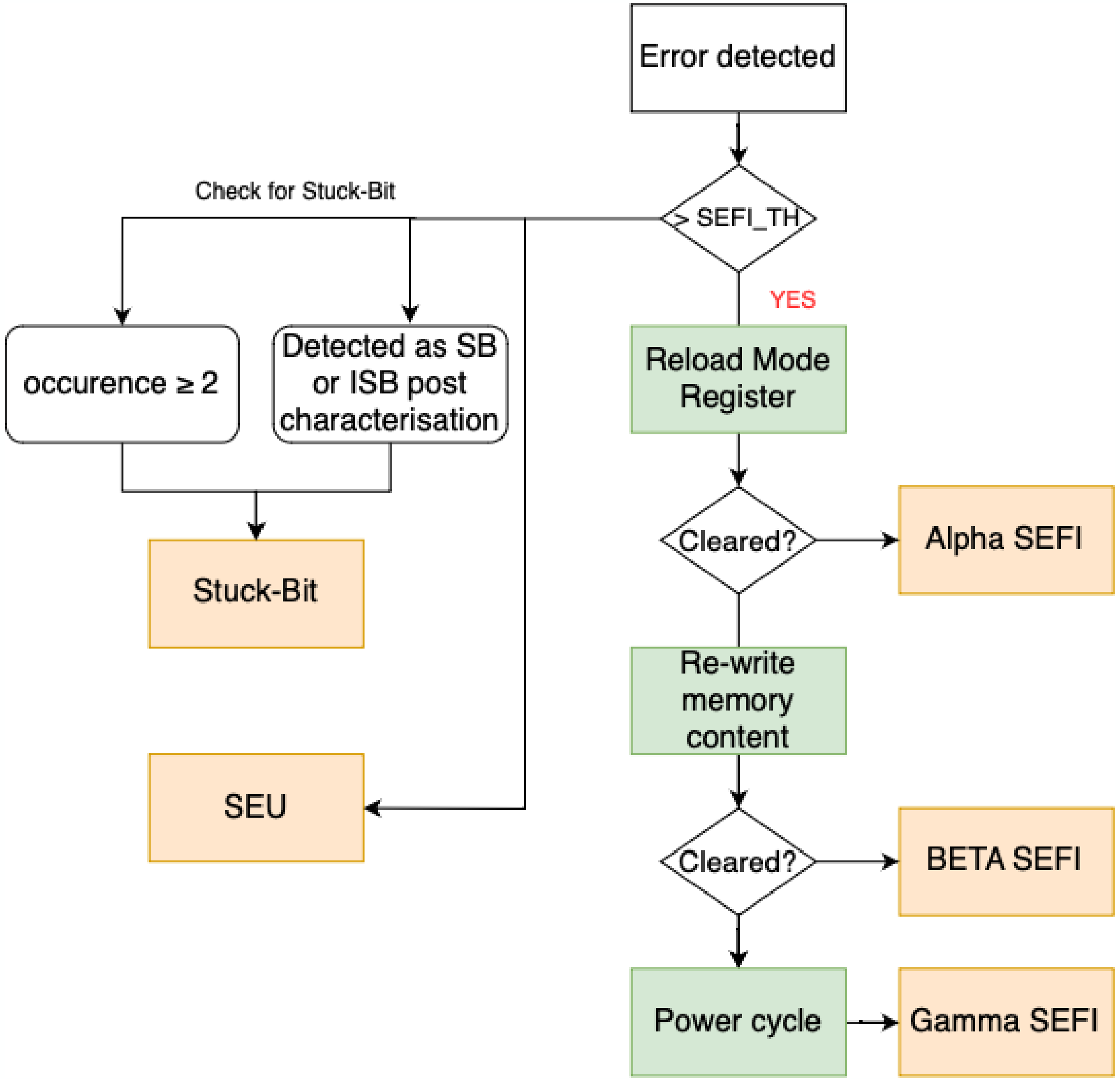
Error classification procedure - Beam ON

- SEFI_TH = 50

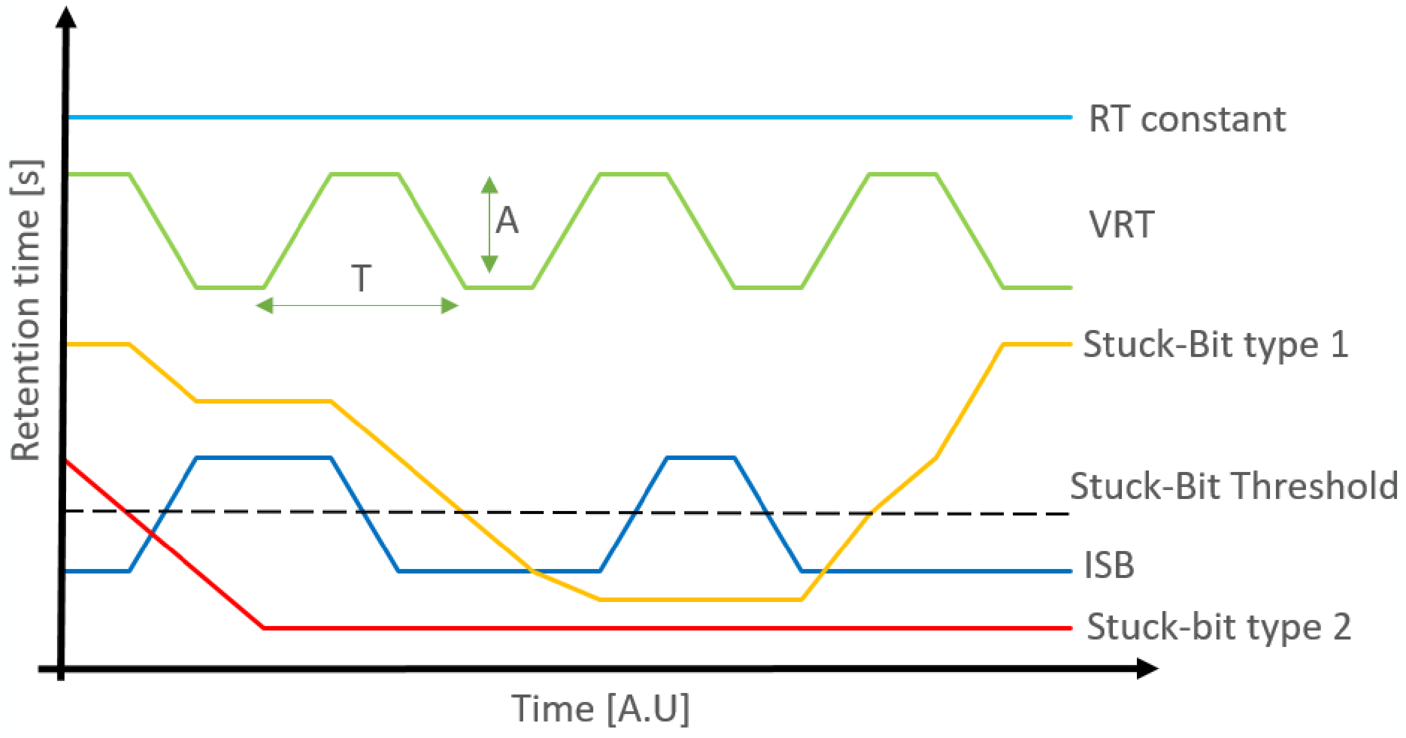
- Each time errors are recorded in a slice, a recovery procedure is applied to discriminate events.

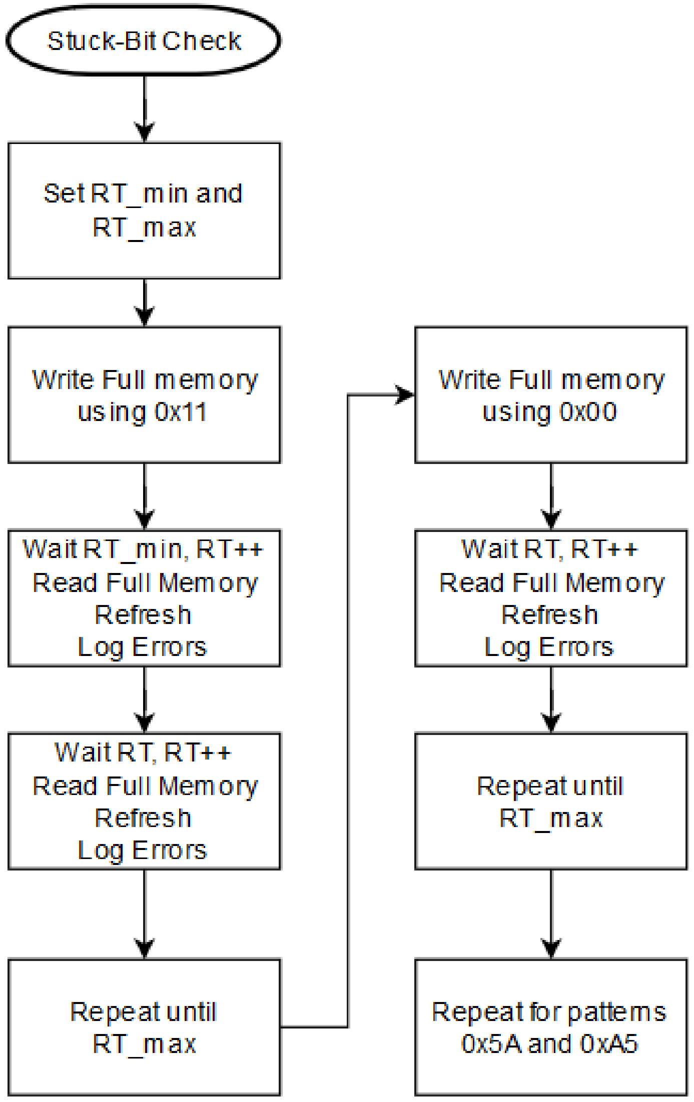
- If a given bit, is recorded 2 times or more in error during a run, or later found stuck, it is removed from the SEU cross-section and labeled as stuck-bits.

- SEFI recovery procedure is based on the JPL classification.

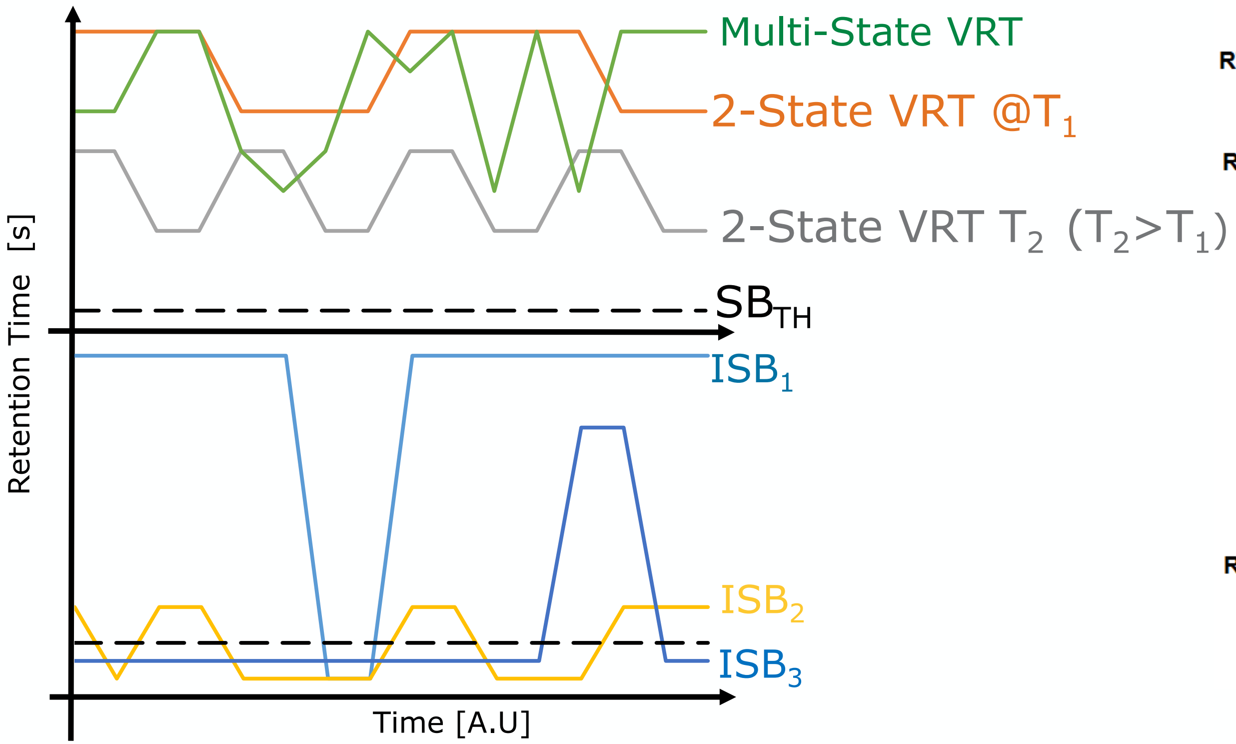


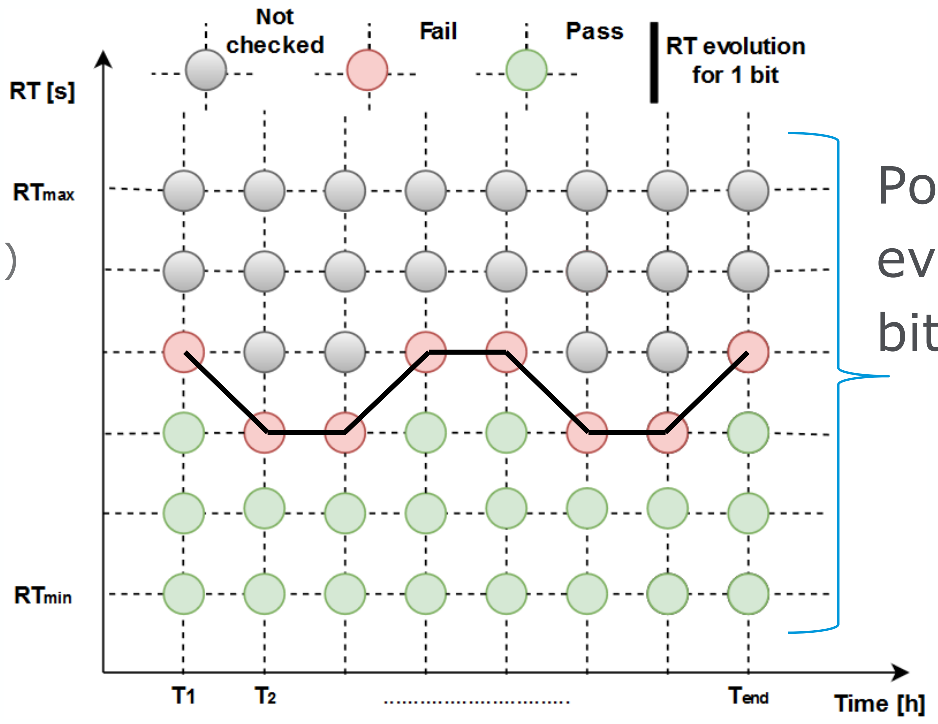
SB characterization procedure – Beam off





VRT and ISB characterization procedure – Beam off

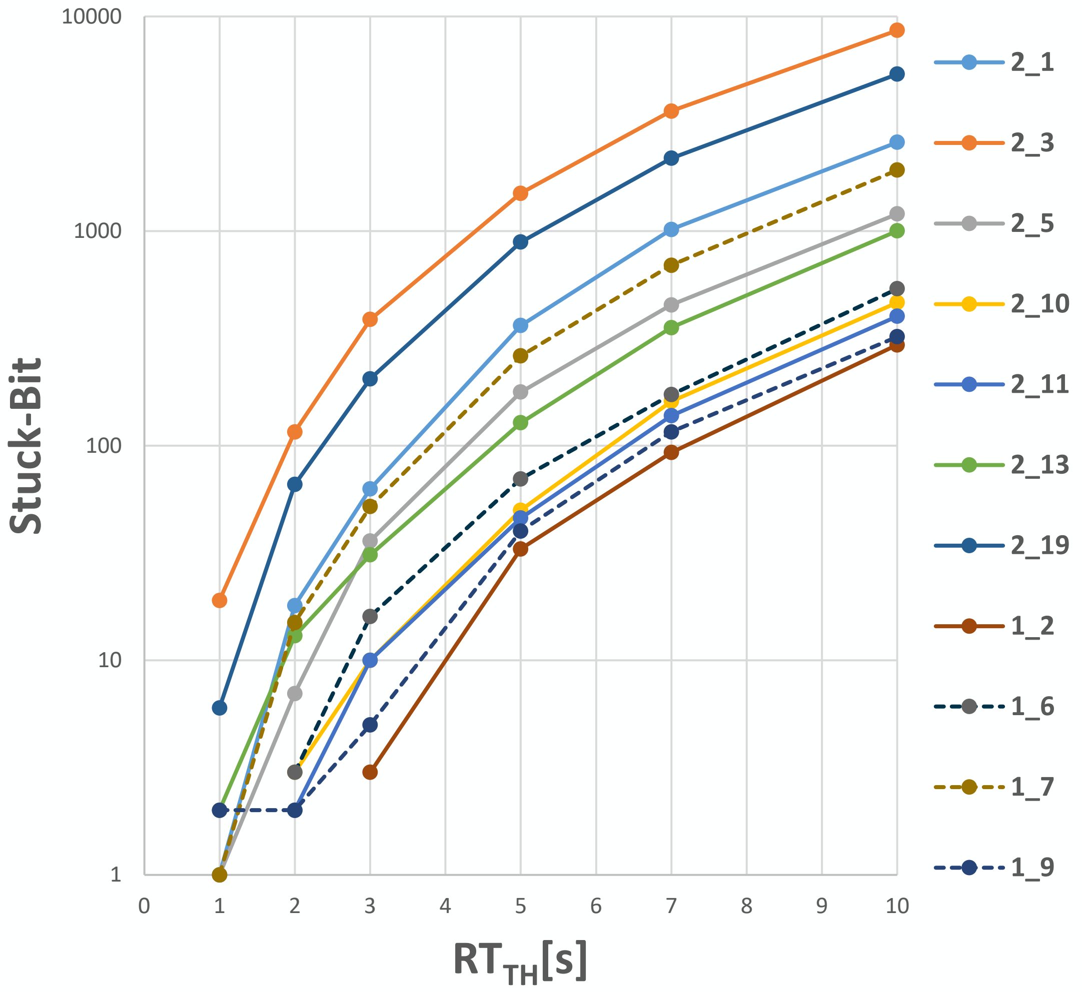


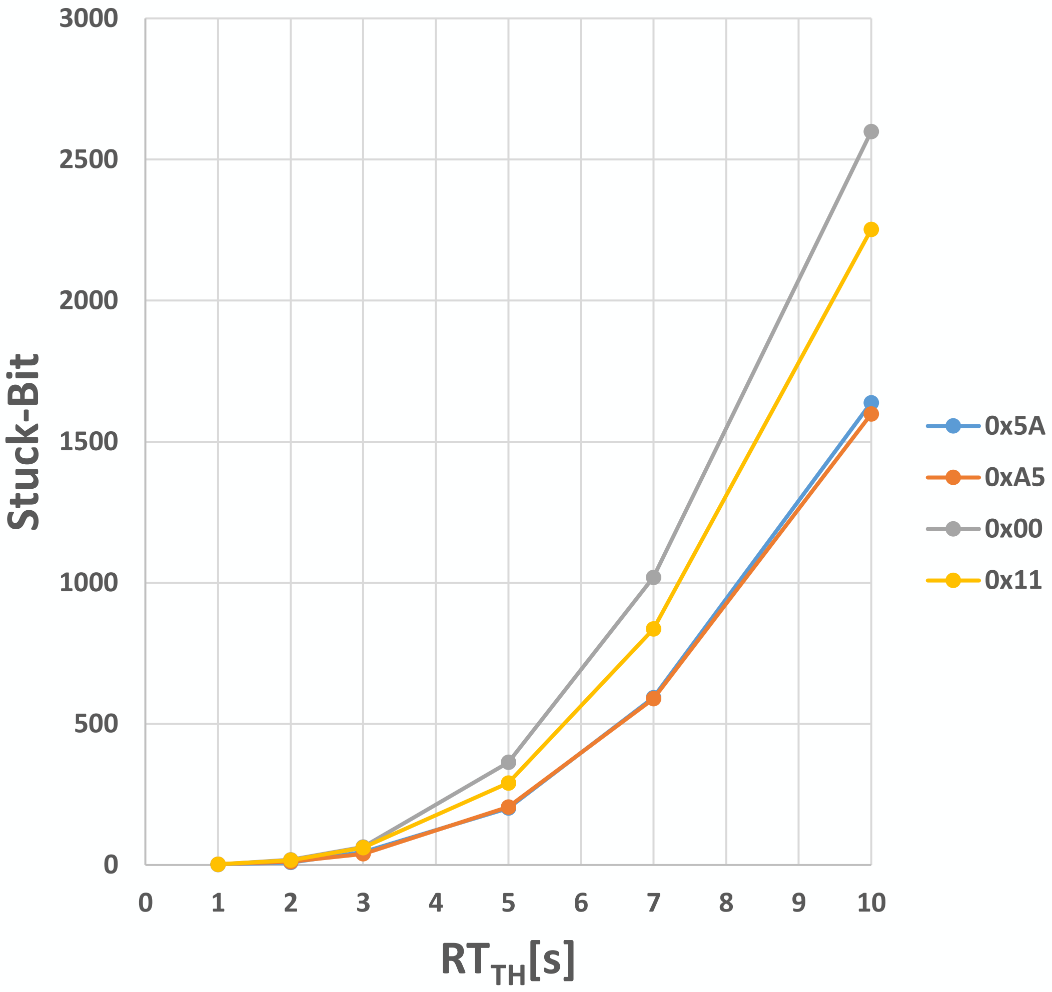


Post-Analysis RT evolution for one bit reconstruction

Pre-Irradiation characterization

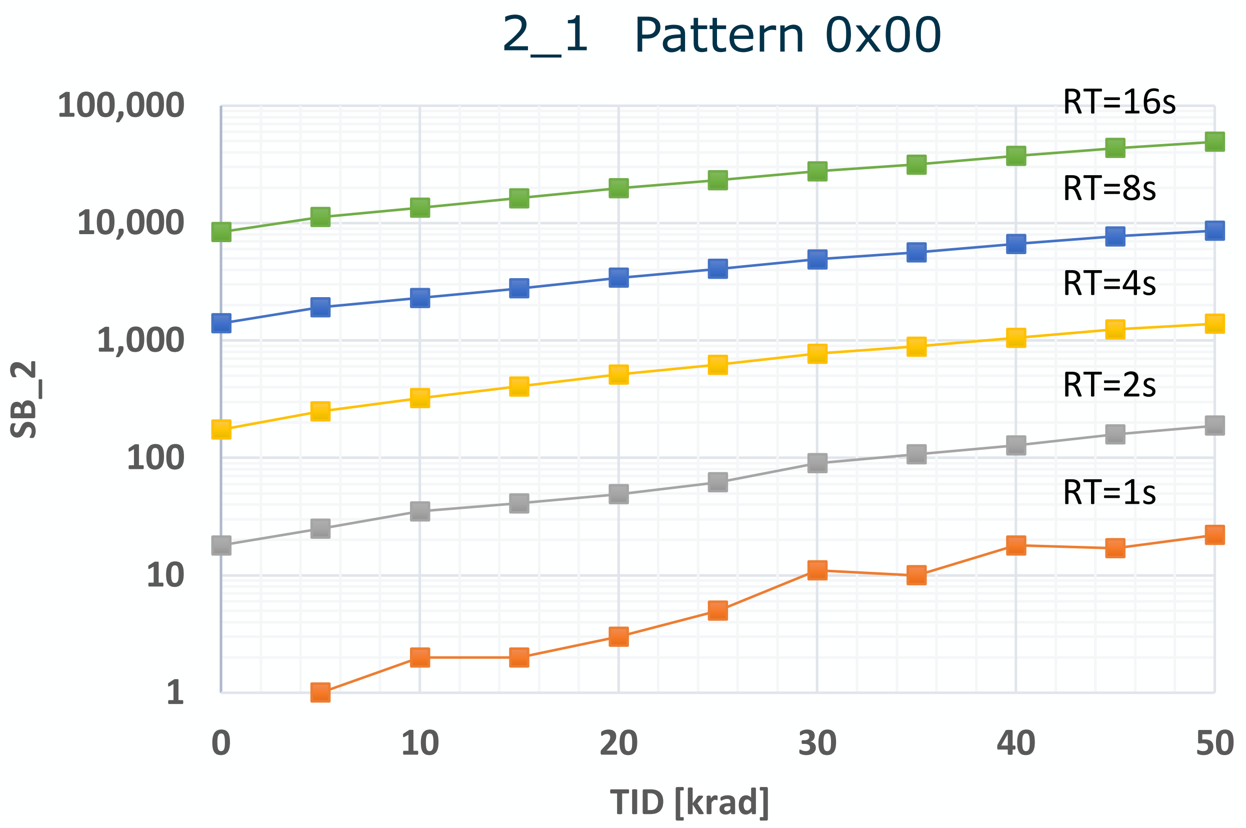
Lot_DUT





TID characterization

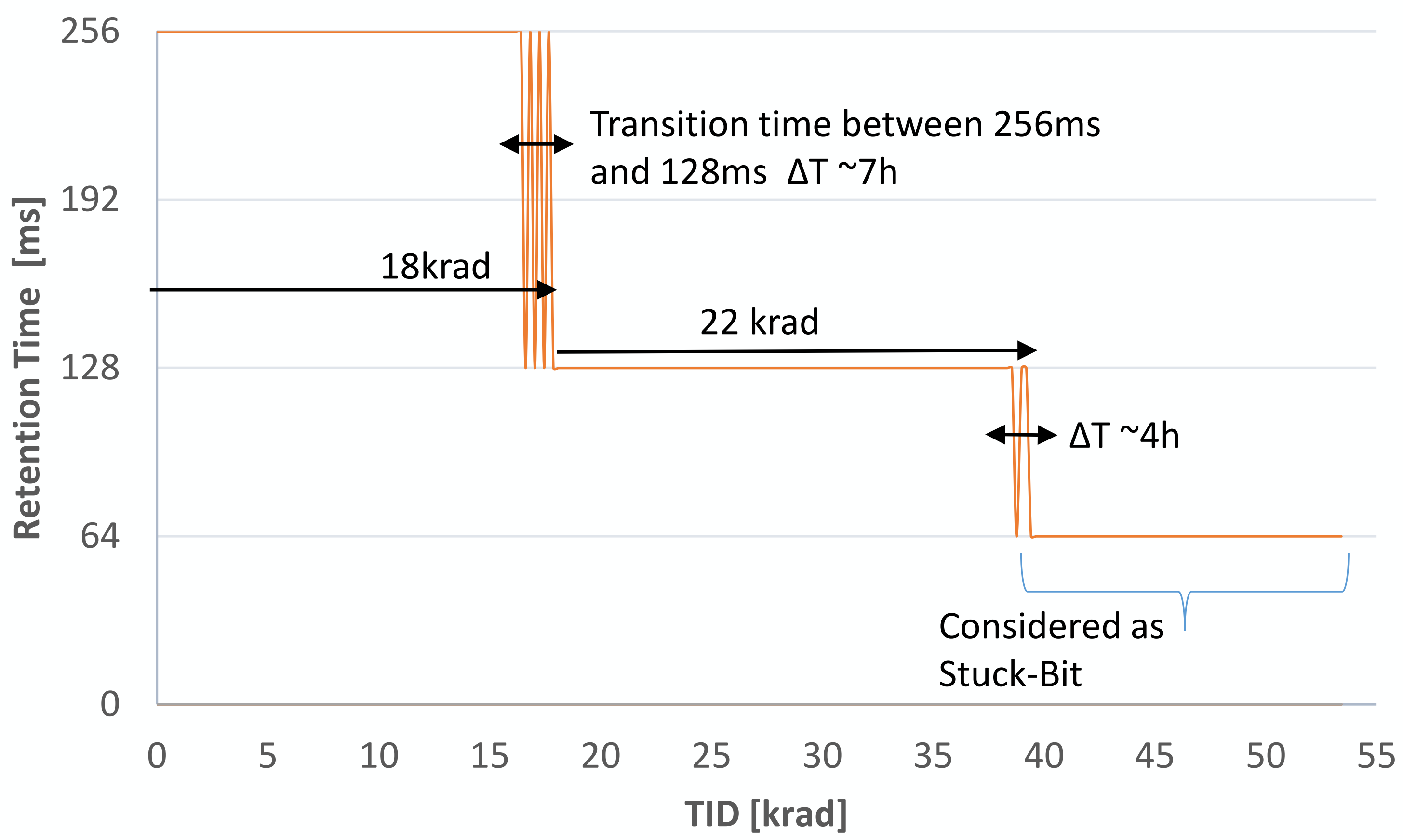
Lot_DUT	Dose Rate [krad/h]	TID [krad$_{(SI)}$]	Bias
2_1	210	53	ON
2_10		35	
2_11		35	



TID created Stuck-Bit

❌ SB can't be created by TID.

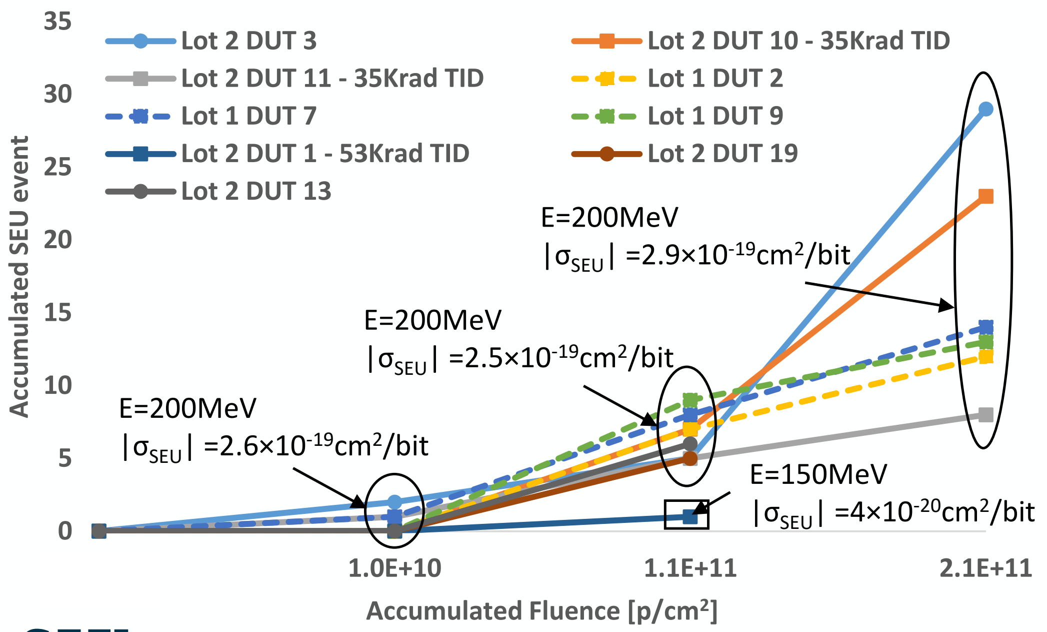
- 1 weak cell was present in the DUT 2_1.
- Its RT value was divided by 2 each ~20krad.
- After 40krad it couldn't hold its value after 64ms.
- This specific bit was only sensitive to the pattern 0xA5, it was fine for 0x5A, 0x00 and 0x11.



-> Only 1 bit out of 3 * 512MBits SDRAM
But there was also only 1 weak cell

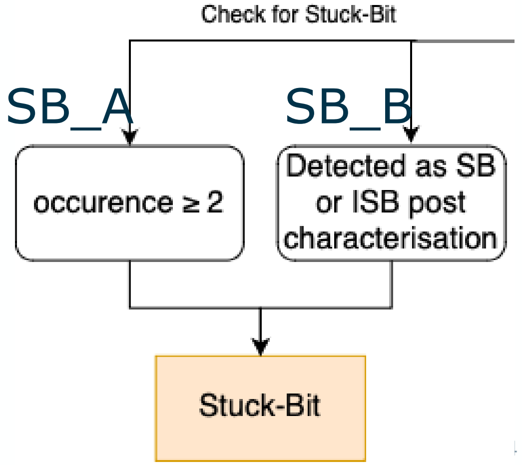
Proton SEE characterization

Lot_DUT - TID	Flux [p/cm2.s]	Fluence [p/cm2]	Accumulated Fluence [p/cm2]	SB_A	SEU_0	SB_B	SEU= SEU_0 - SB_B
2_3	1×10^{8}	5×10^{9}	5×10^{9}	0	2	2	0
	5×10^{7}	5×10^{9}	1×10^{10}	0	2	0	2
	5×10^{7}	1×10^{10}	2×10^{10}	0	1	0	1
	5×10^{7}	1×10^{10}	3×10^{10}	0	0	0	0
	1×10^{8}	7×10^{10}	1×10^{11}	3	5	2	3
	2×10^{8}	1×10^{11}	2×10^{11}	96	43	19	24
2_10 - 35krad	5×10^{7}	1×10^{10}	1×10^{10}	0	0	0	0
	2×10^{8}	1×10^{11}	1.1×10^{11}	18	13	6	7
	2×10^{8}	2×10^{11}	2.1×10^{11}	44	27	11	16
2_11 - 35krad	5×10^{7}	1×10^{10}	1×10^{10}	0	1	0	1
	2×10^{8}	1×10^{11}	1.1×10^{11}	2	4	0	4
	2×10^{8}	2×10^{11}	2.1×10^{11}	1	4	1	3
1_2	5×10^{7}	1×10^{10}	1×10^{10}	0	0	0	0
	2×10^{8}	1×10^{11}	1.1×10^{11}	25	27	20	7
	2×10^{8}	2×10^{11}	2.1×10^{11}	11	39	34	5
1_7	5×10^{7}	1×10^{10}	1×10^{10}	1	1	0	1
	2×10^{8}	1×10^{11}	1.1×10^{11}	35	18	11	7
	2×10^{8}	2×10^{11}	2.1×10^{11}	130	17	11	6
1_9	5×10^{7}	1×10^{10}	1×10^{10}	0	0	0	0
	2×10^{8}	1×10^{11}	1.1×10^{11}	13	14	5	9
	2×10^{8}	2×10^{11}	2.1×10^{11}	46	18	14	4
2_1 - 53krad	9×10^{7}	1×10^{11}	1.1×10^{11}	2	2	1	1
2_19	1×10^{8}	1×10^{11}	1.1×10^{11}	0	9	4	5
2_13	2×10^{8}	1×10^{11}	1.1×10^{11}	3	11	5	6



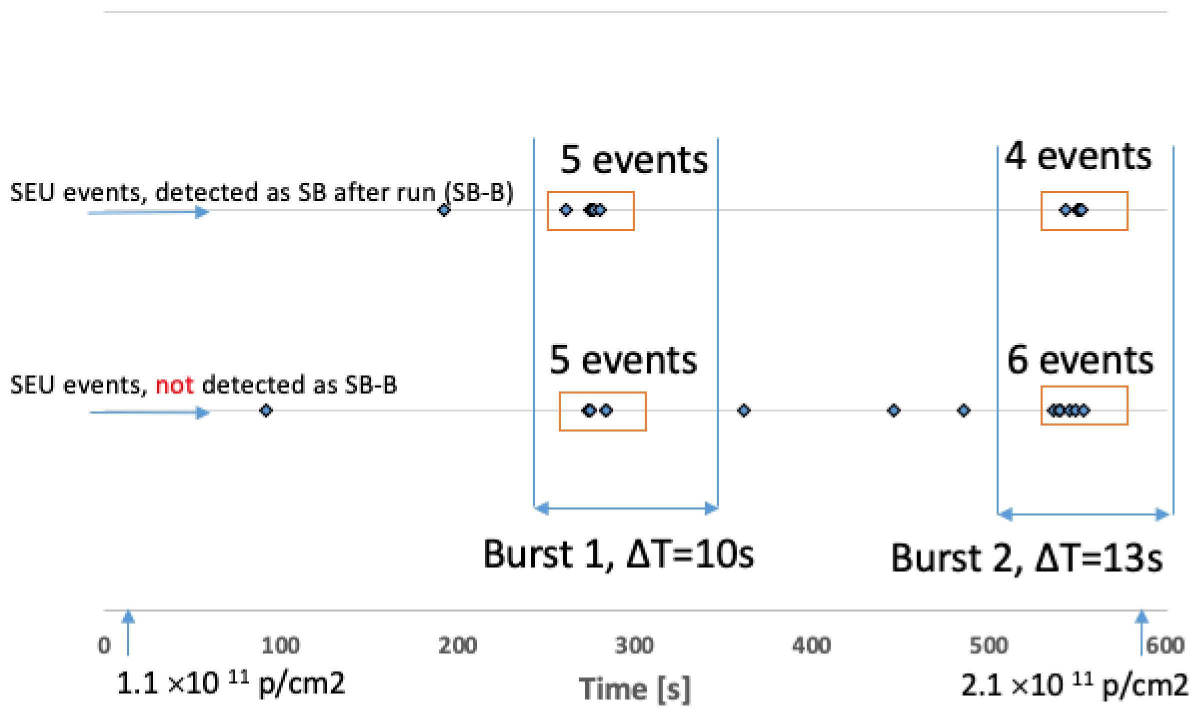
SEFI:
1 A-SEFI
5 B-SEFI

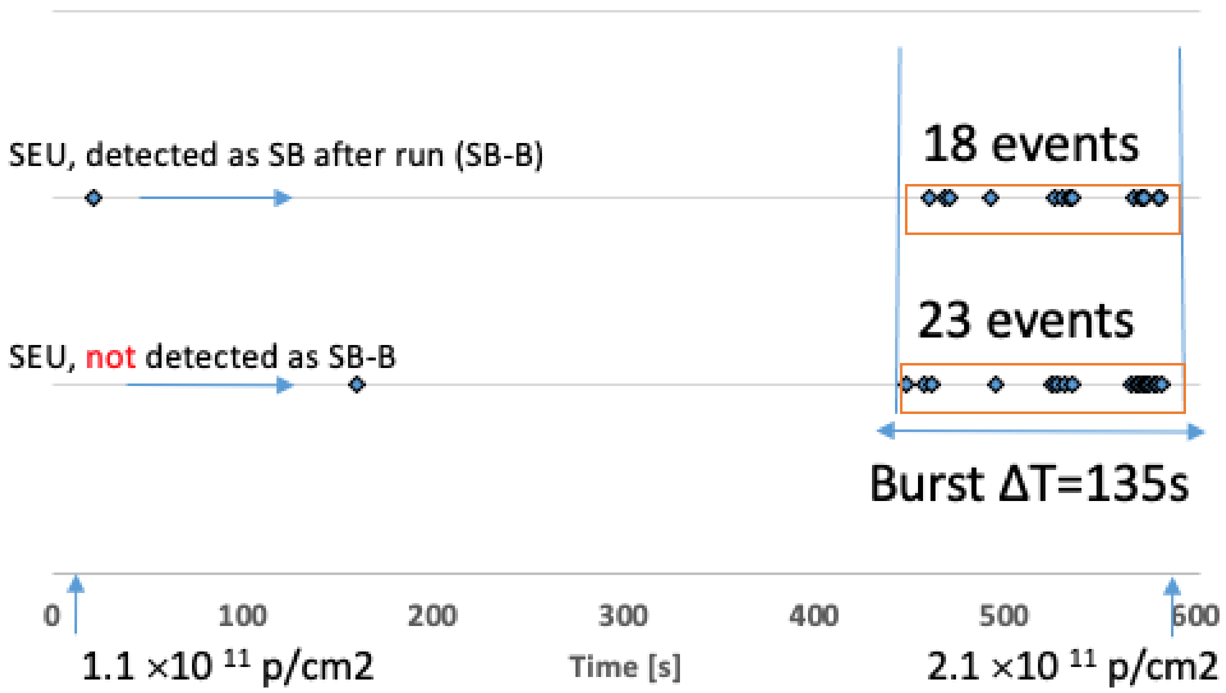
No difference between pristine device and TID pre-irradiated.



Proton SEE event timeline

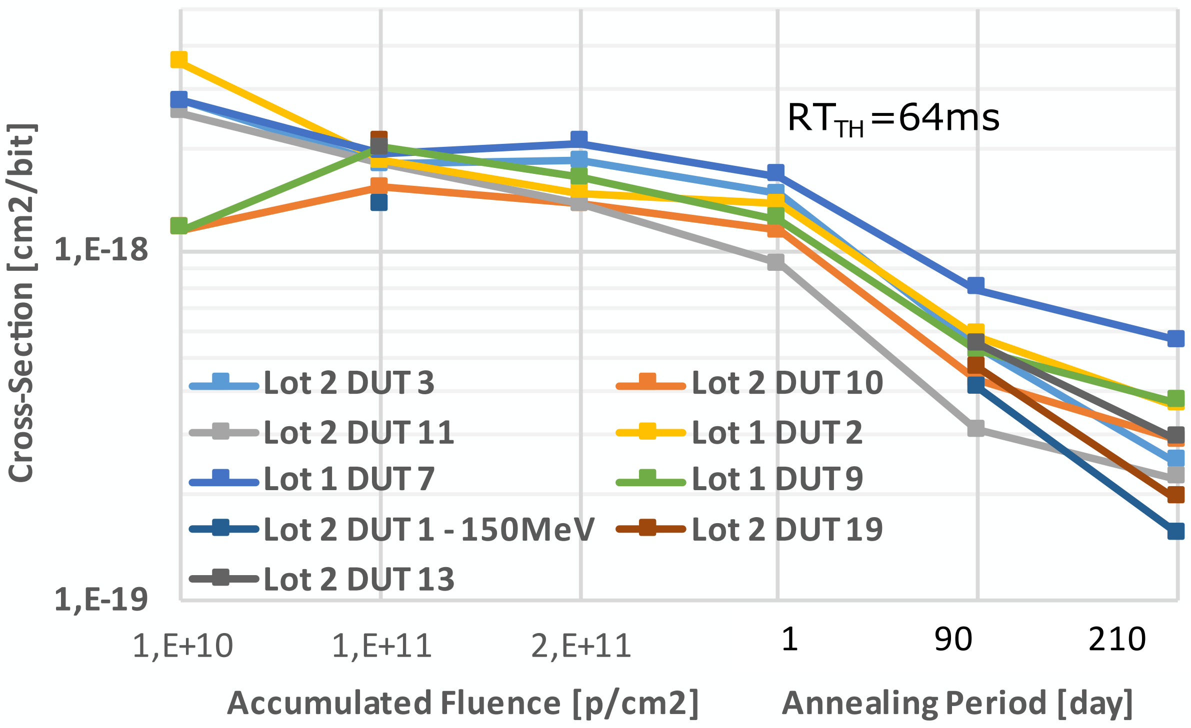
Burst of events, with a mix of detected SB and SEU.



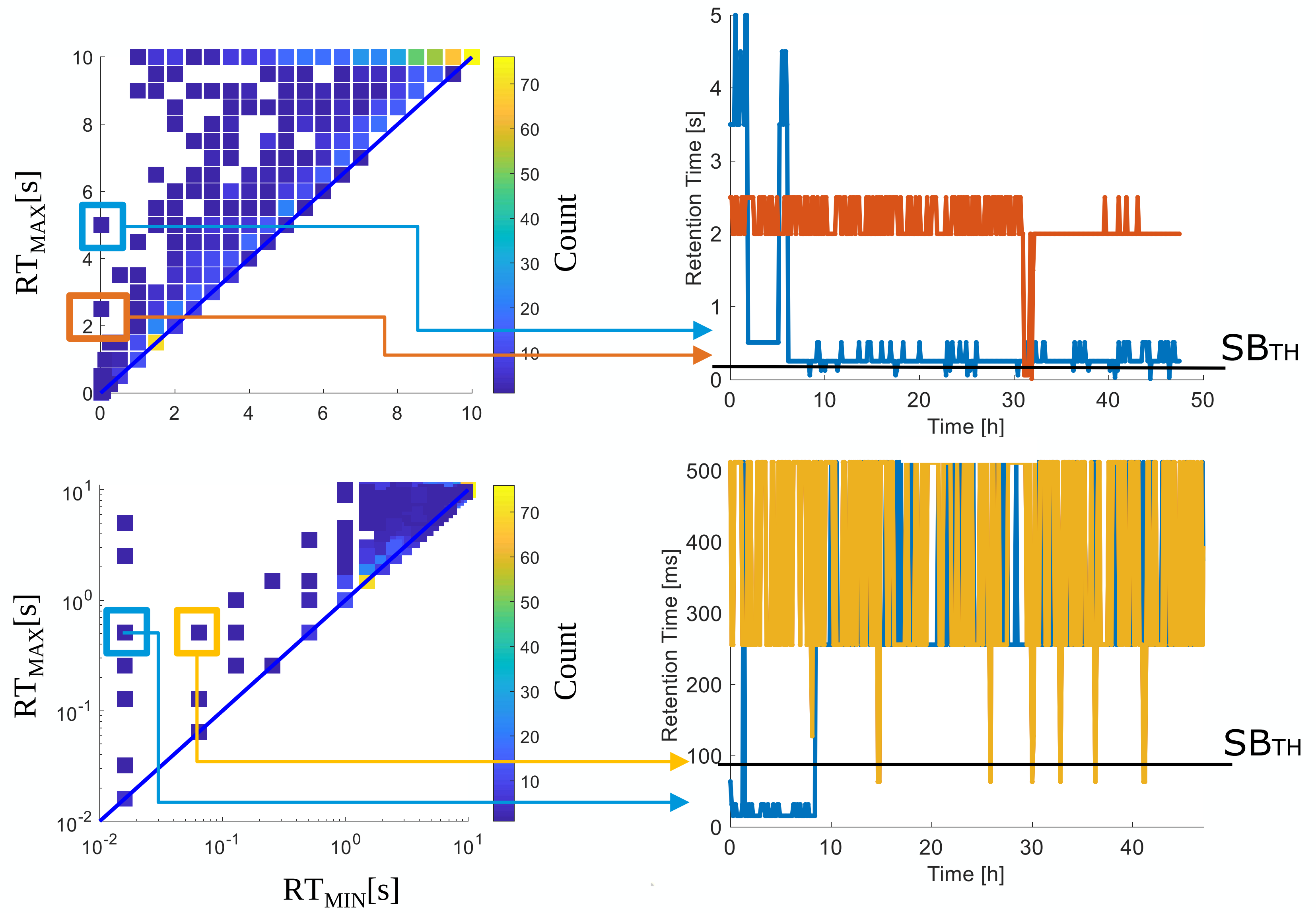


Proton SB cross-section and annealing

- SB cross-section is flat along the accumulated fluence.
- Higher variability at low accumulated fluence due to a lower amount of SB created.
- Annealing measurement after 1, 90 and 210 days (unbiased at ambiant temperature) have been recorded.
- SB created are persistent over time.
- Not much variation from lot to lot.

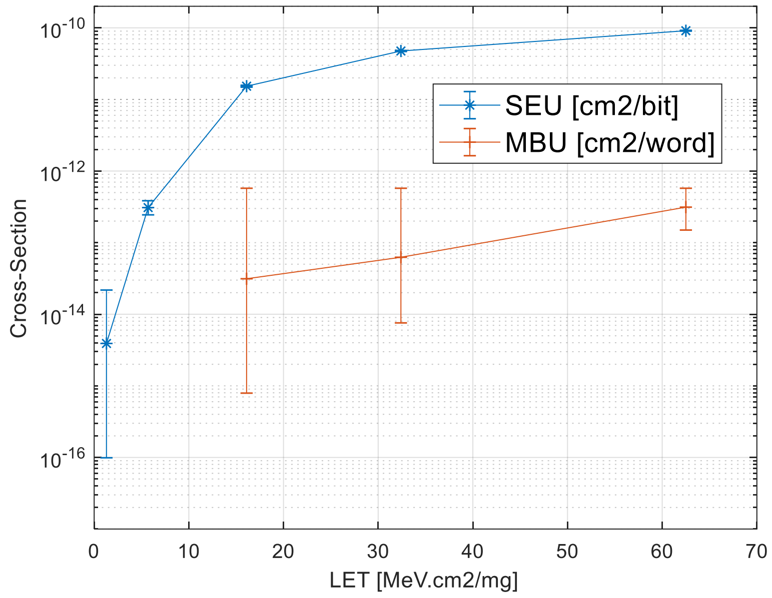


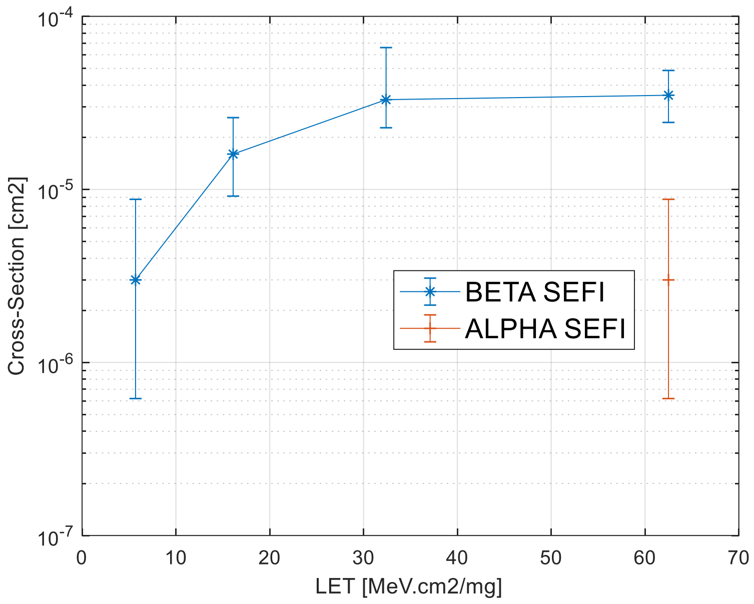
Proton induced ISB



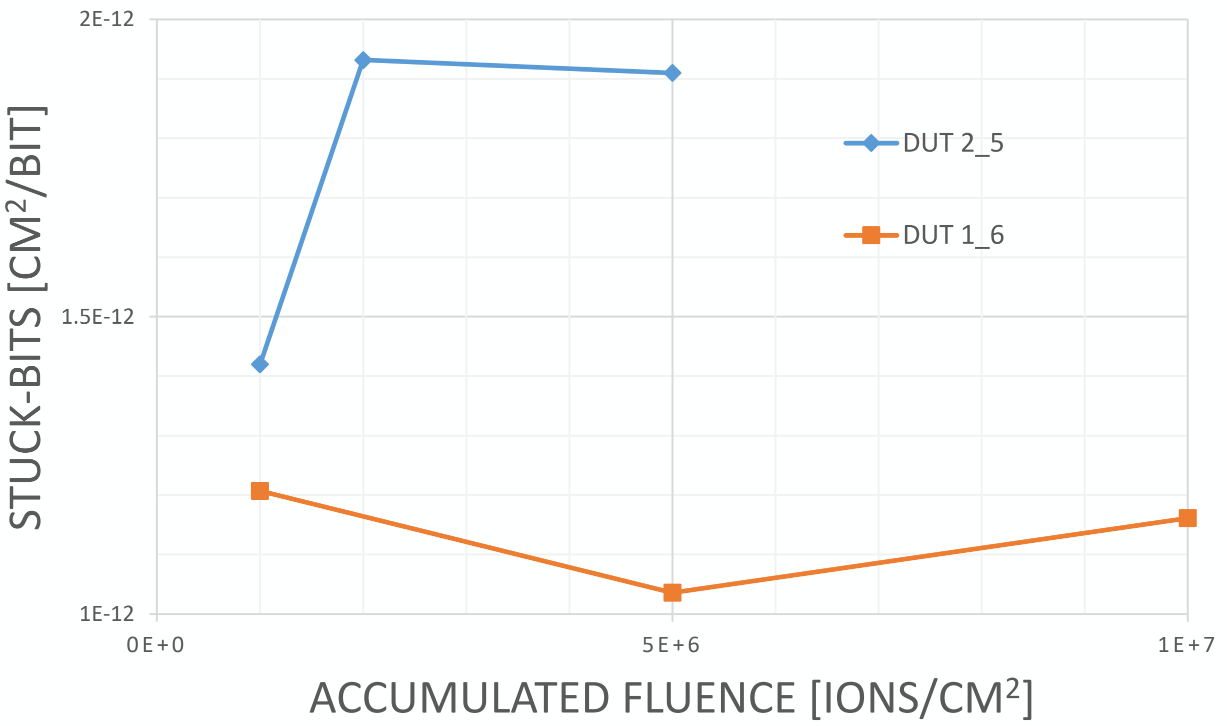
Heavy-Ion SEE test

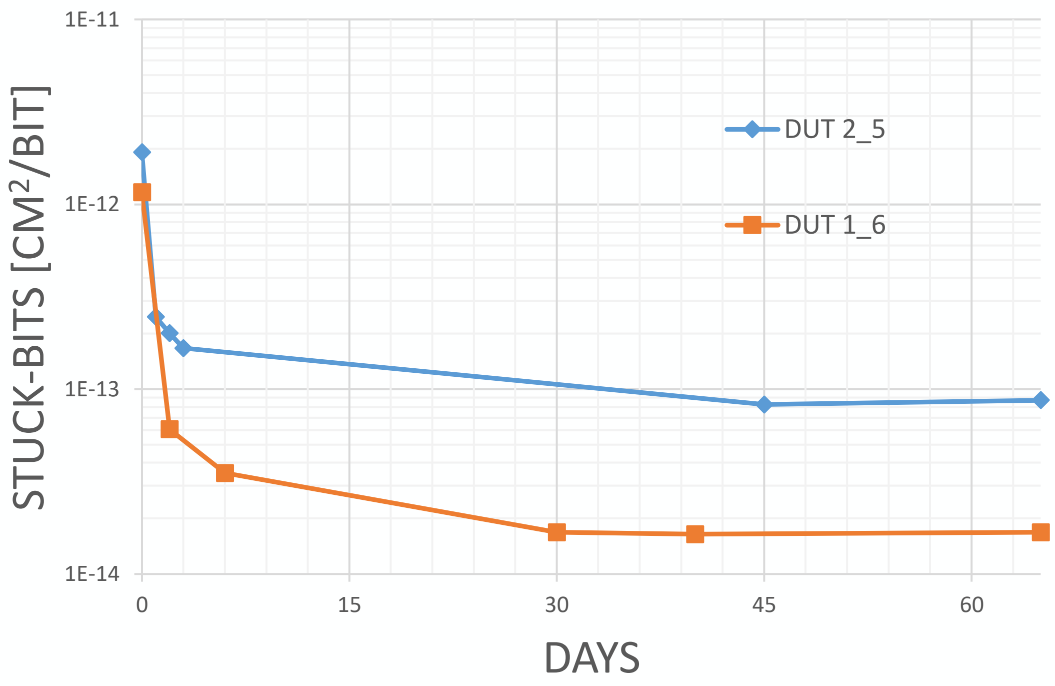
Lot_DUT	Flux [ions/cm^2]	Ion	LET(Si) [MeV.cm^2/mg]	Fluence [cm^{-2}]
2_5 Full device in Use	250	Xe	62.5	10^6
	250	Kr	32.4	10^6
	500	Cr	16.1	10^6
	1×10^3	Al	5.7	10^6
	5×10^3	C	1.3	10^6
	1×10^4	Xe	62.5	3×10^6
	1×10^4	Xe	64.5	10^6
	1×10^4	Rh	46.1	10^6
	1×10^4	Rh	46.1	10^6
1_6 ½ device in use	5×10^3	C	1.3	10^6
	1×10^4	Xe	62.5	10^6
	1×10^4	Xe	62.5	4×10^6
	1×10^4	Xe	62.5	5×10^6



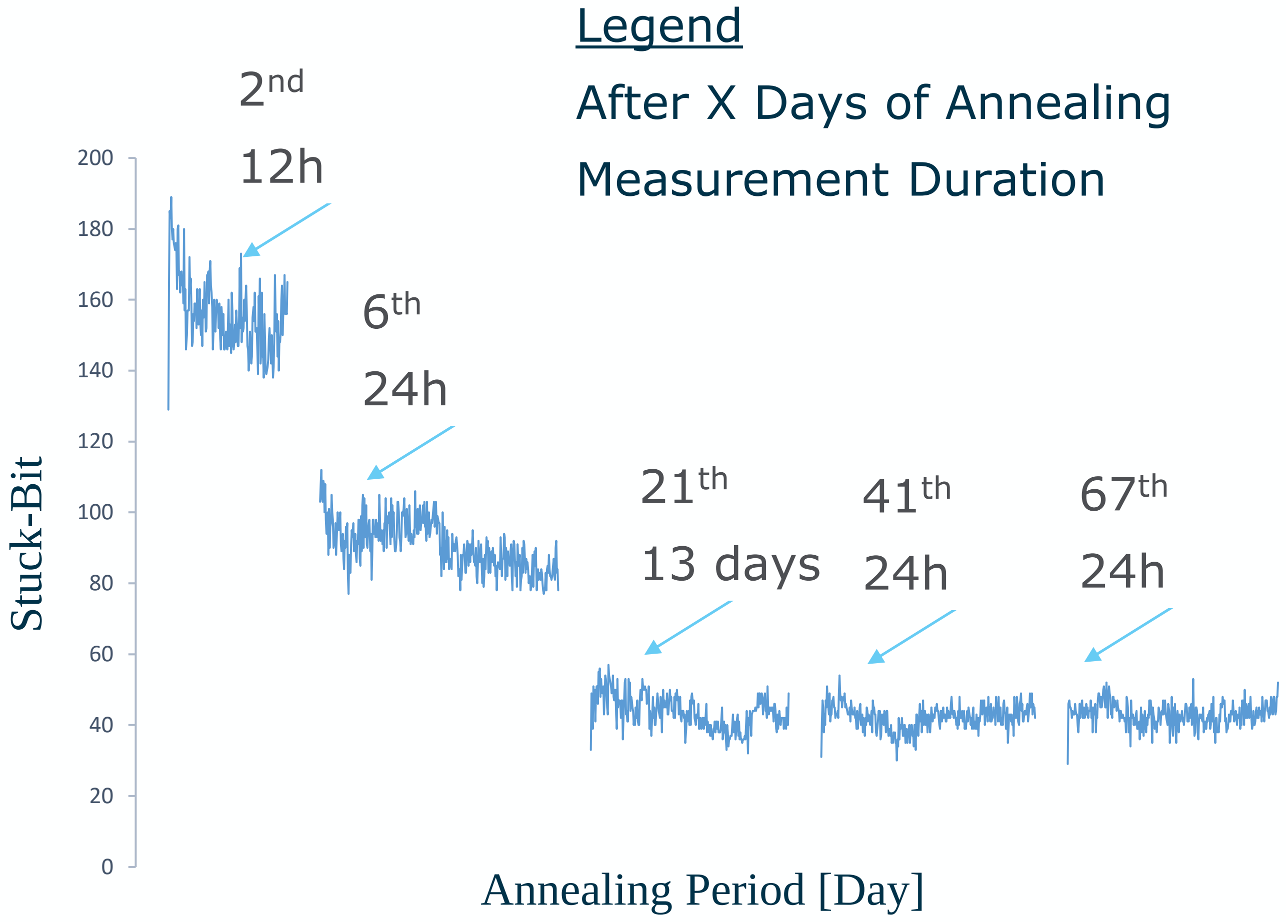


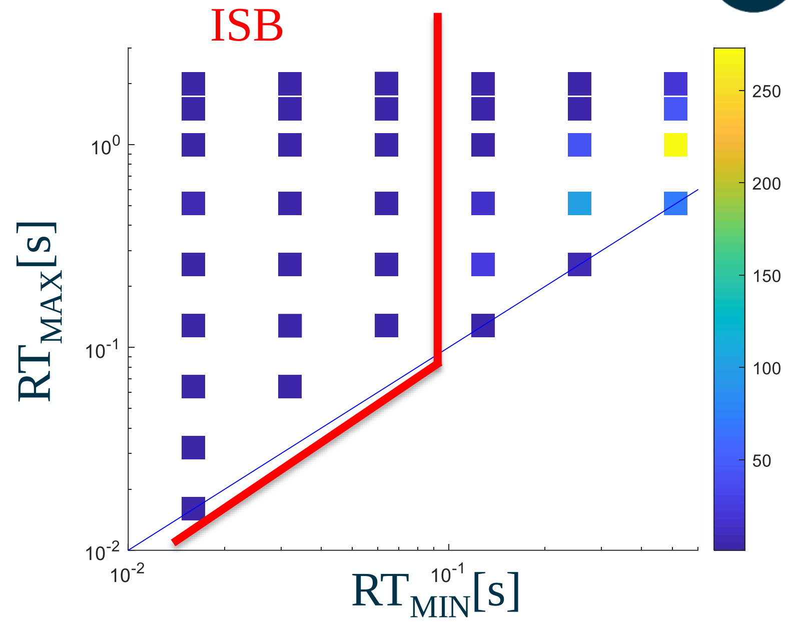
Stuck-Bit cross-Section and annealing

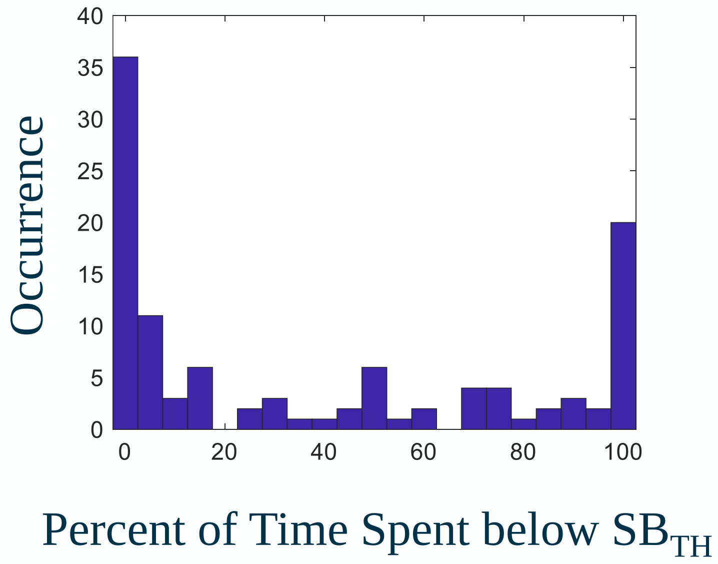




SB and ISB measurement for DUT 1_6







Testing procedure summary

1) Pre Characterization, search for the weakest cell. Temperature measurement.

2) In situ measurement under irradiation, check for SEU/SEFI and SB.

3) Rapid first post characterization, search for stuck-bits using static patterns and RT_{TH} ranging from 16ms to 16s. In between runs.

4) Long term post characterization, annealing effect and ISB 24h measurement. Temperature measurement.

Key take aways

- Proton and Heavy-Ion are a must for SB testing. TID test must be performed if weak cell with low margin regards to the 64ms threshold are present in the device, or high operating temperature.

- Short and long-term measurements are preferred to evaluate annealing effects and compute SB for short and long terms.

- ISB measurement is preferred for a more precise extraction of SB count.

- Do stuck-bits measurement at your operating temperature as it plays a major role in the SB count.

- Test the whole memory under beam to catch as much as possible of SEFIs and with a dynamic PRBS pattern.

- Create a unique list of SB, detected with different patterns. Test two patterns at minimum. Remember that a given bit cell is sensitive with a combination of its written content and in the neighbouring cells.

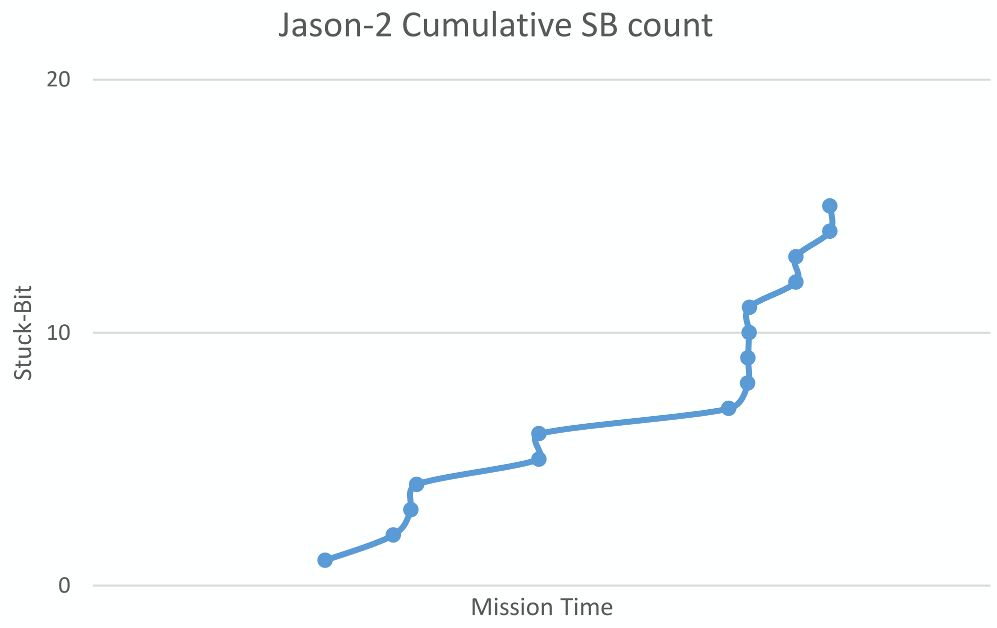
Counter measure for Stuck-Bits

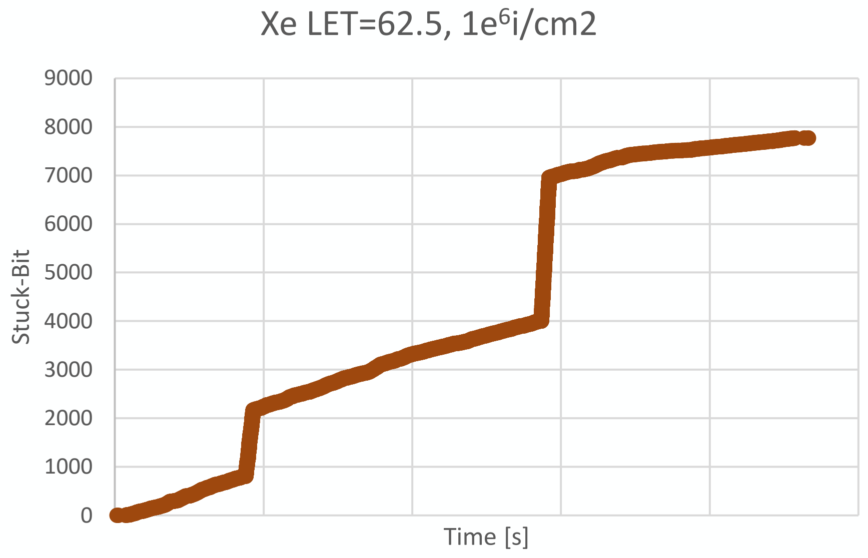
- EDAC implementation but it can be defeated for a SB + 1 SEU in the same word for a SECDED.

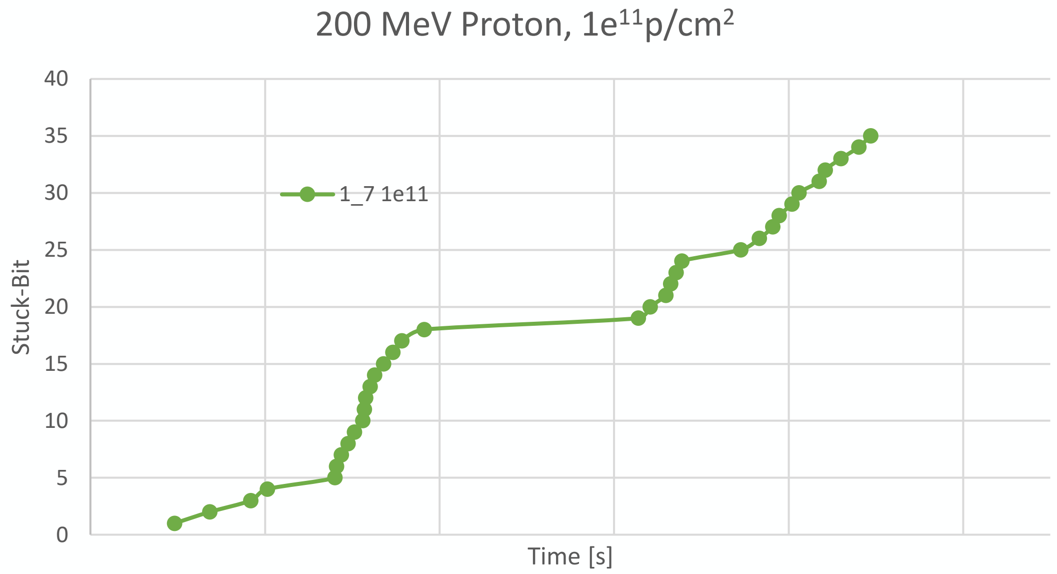
- Use a higher refresh rate. In absence of radiation degradation, the designer can decide to use a much lower refresh rate to save power, but if in presence of SB, one should increase the refresh rate in the faulty row.

- Bit/Row repairs mechanism (remapping the logical bit/row address that points to the faulty bit/row to a spare one).

In-flight data vs ground testing







Atypical shape
Single-event ?
Cumulative?

"Experimental characterization and In-flight observation of weakened cell in SDRAM", Anne Samaras, 2015

More results were presented at NSREC and RADECS 2020