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Fraunhofer Institute for Technological Trend Analysis INT

TEC-QEC Final Presentation Days 2023-06-29

# Radiation characterization and functional verification of COTS components for space applications (RACOCO)

Contract number 4000127569/19/NL/FE

**Michael Steffens**

**ESA TOs: Gianluca Furano, Maris Tali, Marc Poizat**

# Project Structure

- Kicked-off in Summer 2019
- Expected project duration: 36 months (i.e. Summer 2022)

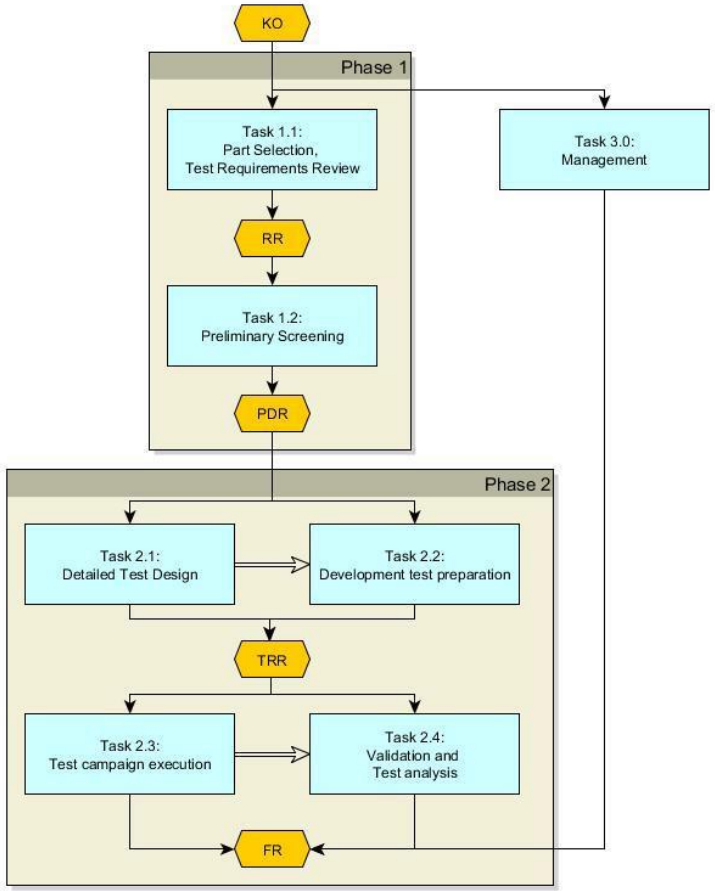
- ESA TOs: Gianluca Furano, Maris Tali, Marc Poizat

**Initial plan for Phase 1**

- Gather input from third parties (Survey, Workshop)
  - Develop the list of components to test
- Procure minimum sample sizes for a preliminary screening campaign
  - Identify „showstoppers“, planned to include Laser-SEE tests
- End phase 1 with a reduced and well established „short“ list of components for detailed testing

**Initial plan for Phase 2**

- Procure larger sample sizes from the „short“ list (if possible complete reels)
- Full TID / SEE characterization of the components from the short list
- Develop guidelines and „lessons learned“ for COTS RHA

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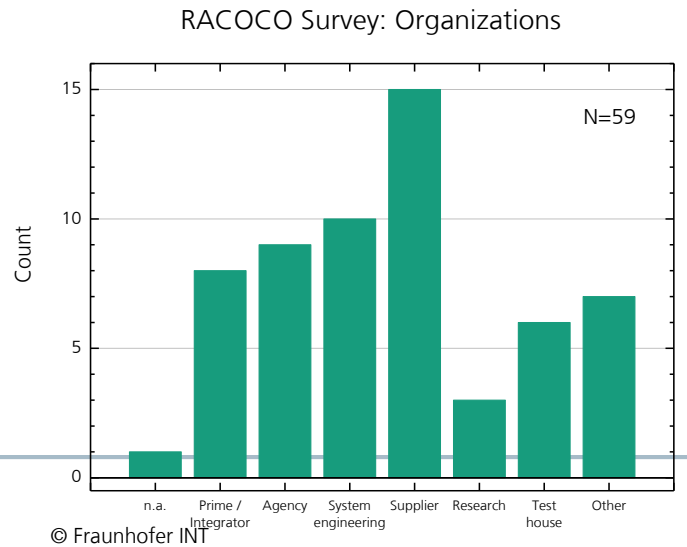
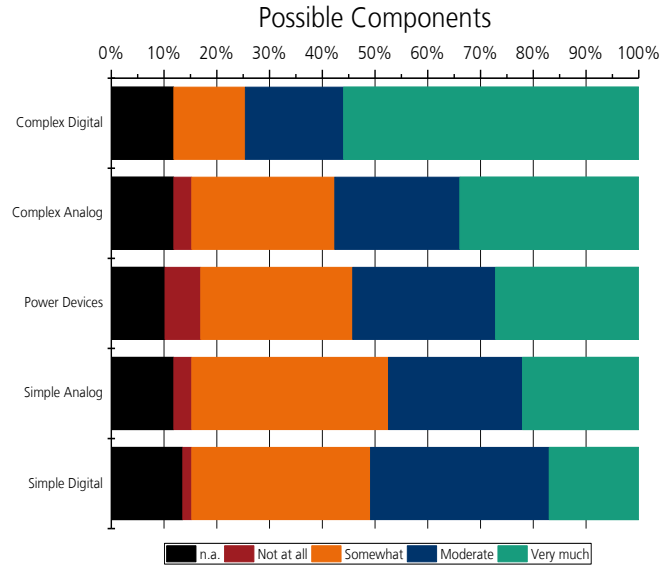
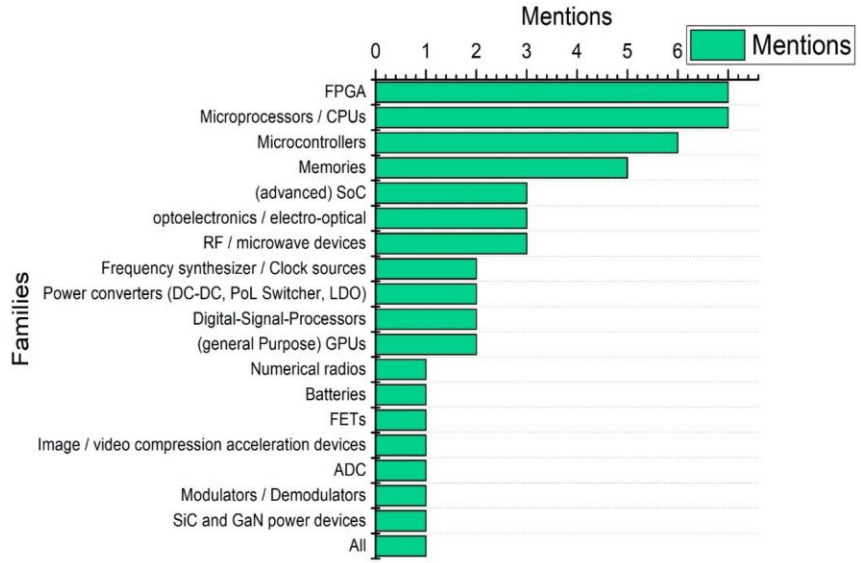
# Gather input from third parties (Survey, Workshop)

- The survey was setup, conducted and advertised
  - 2019-09-16: RADECS, Montpellier (pre-announcement)
  - 2019-09-30: Fraunhofer@ESTEC, Noordwijk (pre-announcement)
  - 2019-11-06/07/08: ACCEDE, Sevilla
  - 2019-11-12 ADCSS, Noordwijk
- Survey was closed early 2020
- 59 completed responses from the community were collected
- Conduction of workshop was discarded
- The „long“ list of components was then developed based on the survey feedback




  **Public information**

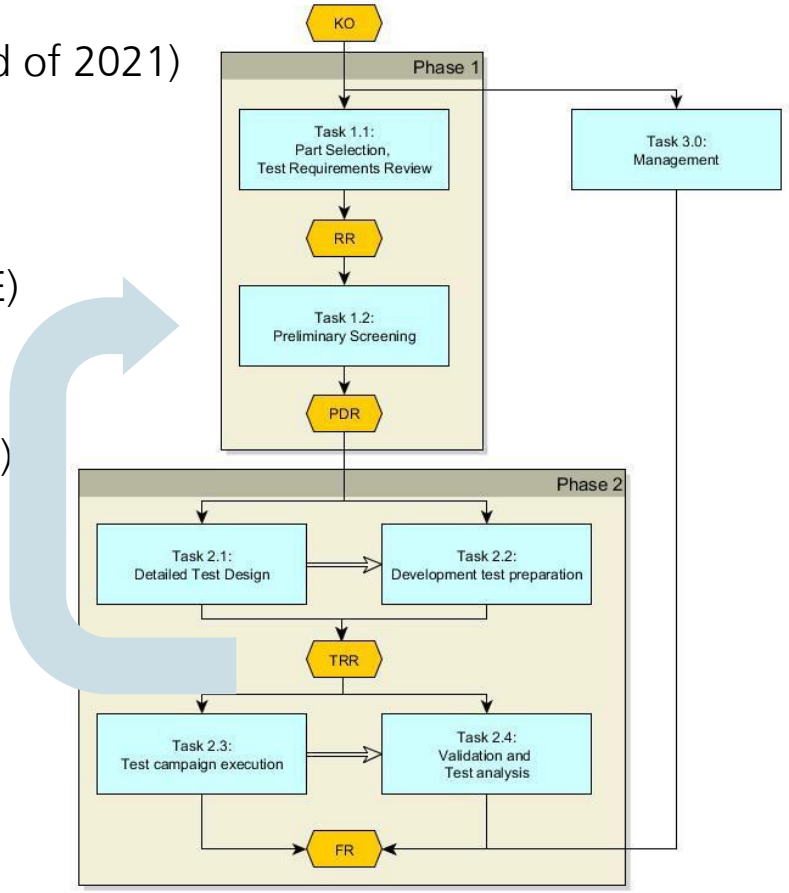
# Re-development of Project Structure

- Large scales events that impacted the further progress (pandemic, „chip crisis“, flood of 2021)
  - Component supplies volatile or non-existant
    - Two-step procurement considered too risky
  - Lab work was difficult or impossible for some time
  - Equipment to be used in the preliminary screening test not available (e.g. Laser-SEE)

**Finding a suitable way to proceed**

- Procure devices that are available on the market (for a long time this excluded MCUs)
  - Procure at least enough samples for TID/SEE testing
- Re-organize test efforts such that
  - TID tests (non-preliminary) are mainly in Phase 1
  - SEE tests are in Phase 2

- Currently these TID tests are still on-going
- → Phase 1 not yet concluded



# Test results

## Overview

- TID-Test results

| Item | Manufacturer | Part Description | | |
|---|---|---|---|---|
| ADUM7440CRQZ-RL7 | Analog Devices | Digital Isolators 4 Channel Digital Isolator, 1kV | ESA high priority | Date Code: 2140 / Lot code*: AV13107.16 |
| INA169QPWRQ1 | Texas Instruments | Current & Power Monitors & Regulators Auto Cat Hi-Side Measurement Mon | ESA high priority | Date Code: 2139 / Lot code*: 1752825MY1 |
| LMG3410R050RWHT | Texas Instruments | Gate Drivers 600-V 50-m GaN with integrated driver and protection | ESA high priority | Date Code: Feb-2022 / Lot code*: L/C2540877T42 |
| TSV992IQ2T | STM | Op-Amp | | Date code: 2148 / Lot code*: GM148CXH |
| TSZ182HYDT | STM | Op Amp | | Date code: 9D2044 / Lot code*: 7B044564VJ7B |
| THS4032MDGNREP | Texas Instruments | Op Amp | | Date code: 2052+5 / Lot code*: 1103866HNA |
| REF5050MDREP | Texas Instruments | Voltage Reference | | Date Code: 2028 /Lot code*: 052912ML0 |
| IRF9540NPBF | Infineon | MOSFET P-Channel 100V 23A TO220AB | | Date Code: P021J / 40RV,<br>Date Code: P124D / LW43,<br>Date Code: P145j / AH99 |

- Tests in preparation

| Item | Manufacturer | Part Description | |
|---|---|---|---|
| TMP423AQDCNTQ1 | Texas Instruments | Temp Sensor | |
| LTC4303IMS8PBF | Analog Devices | I2C buffer | |
| SM72442MTE/NOPB | Texas Instruments | Power Management Specialized - PMIC | ESA high priority |
| MT25QU128ABA8E12-0AAT TR | Micron Technology | NOR Flash | |
| MR2A08ACYS35 | Everspin Technologies | NVRAM | |

* Lot code as provided by the distributor
origin unknown
could be assembly lot, procurement lot…..

# TID-Test approach

- Tests performed at the Co-60 facilities at Fraunhofer INT
- Target dose level: 100 krad(Si)

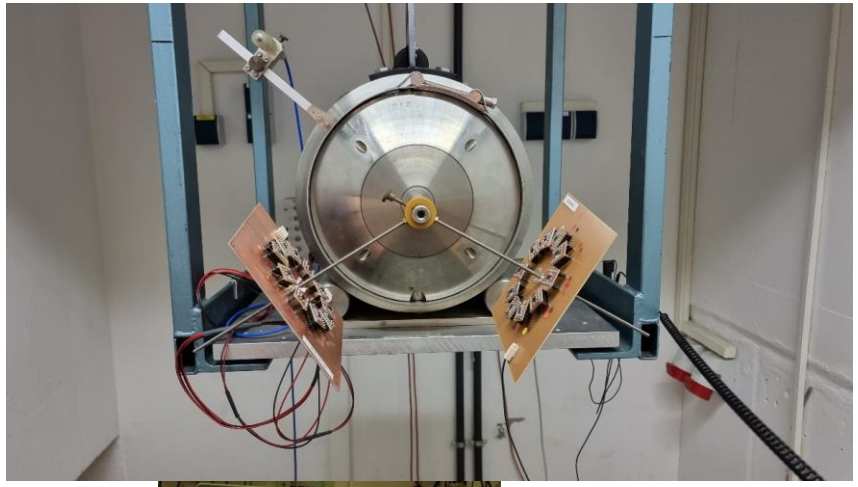
| measurements | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| dose [krad (Si)] | 0 | 5 | 10 | 20 | 30 | 50 | 100 | Annealing RT | Annealing 100°C |

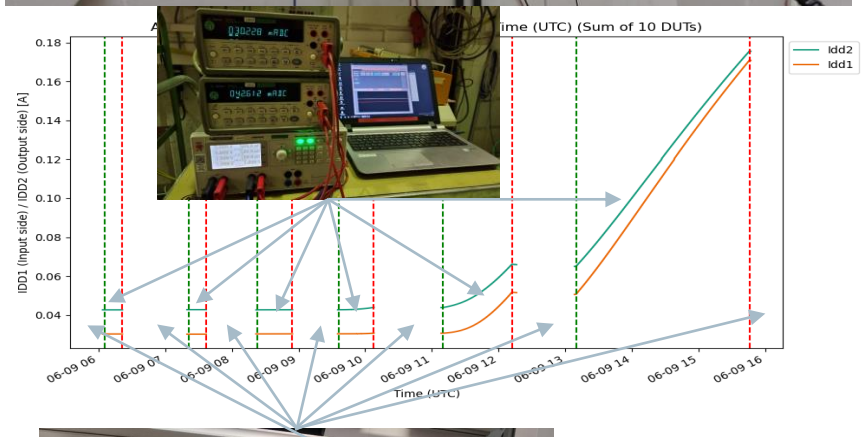
- Dose rate within Window 1 („Standard Rate“): 5-20 krad(Si)/h
  - With exceptions (currently only INA169): additionally tested in Window 2 („Low Rate“)

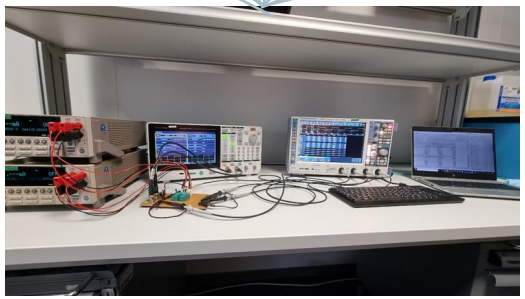
- In-situ tests during irradiation of basic parameters
- Parameteric characterization at first, last and intermediate steps

- Testing of 10 biased and 10 unbiased samples
  - With exceptions:
    - LMG3410R050RWHT: 5 biased + 5 unbiased samples
    - IRF9540NPBF: 3 date codes

      Per Date Code: 10 biased / 10 unbiased





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# ADUM7440CRQZ-RL7 TID-Test Results

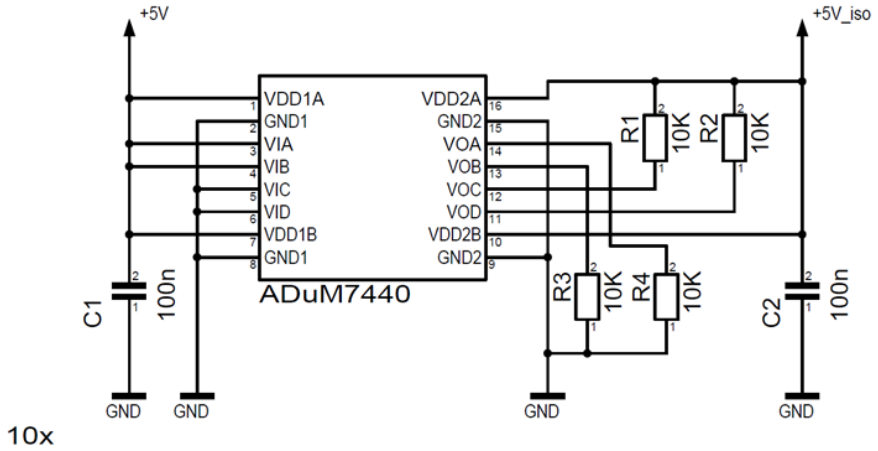
## 4 Channel Digital Isolator, 1kV

The Analog Devices ADUM7440CRQZ-RL7 is a 1kV 4-channel Digital Isolator transmitting input signals coming into the input side to output via Analog Devices' iCoupler® monolithic air core technology.

The device supports unidirectional communication up to 25 Mbps at 3.3 V and 5 V operation.

The datasheet indicated bidirectional communication. This however only applies to the ADuM7441 and 7442 and not the 7440.

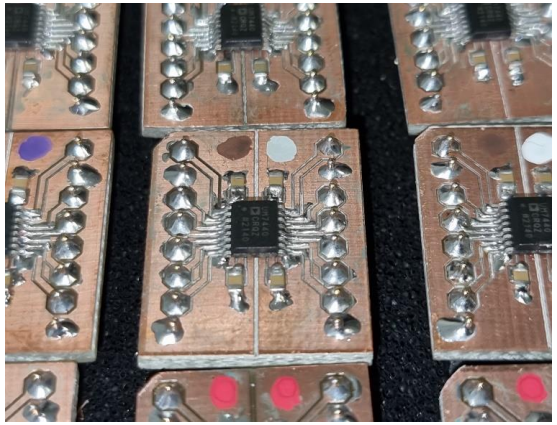
STATIC




10x

| Bias Configuration: Static |
|---|
| VDD1 = 5 V, VDD2 = 5 V |
| 2 input channels connected to +5V, |
| 2 input channels connected to GND |

| Unbiased |
|---|
| All Pins grounded |

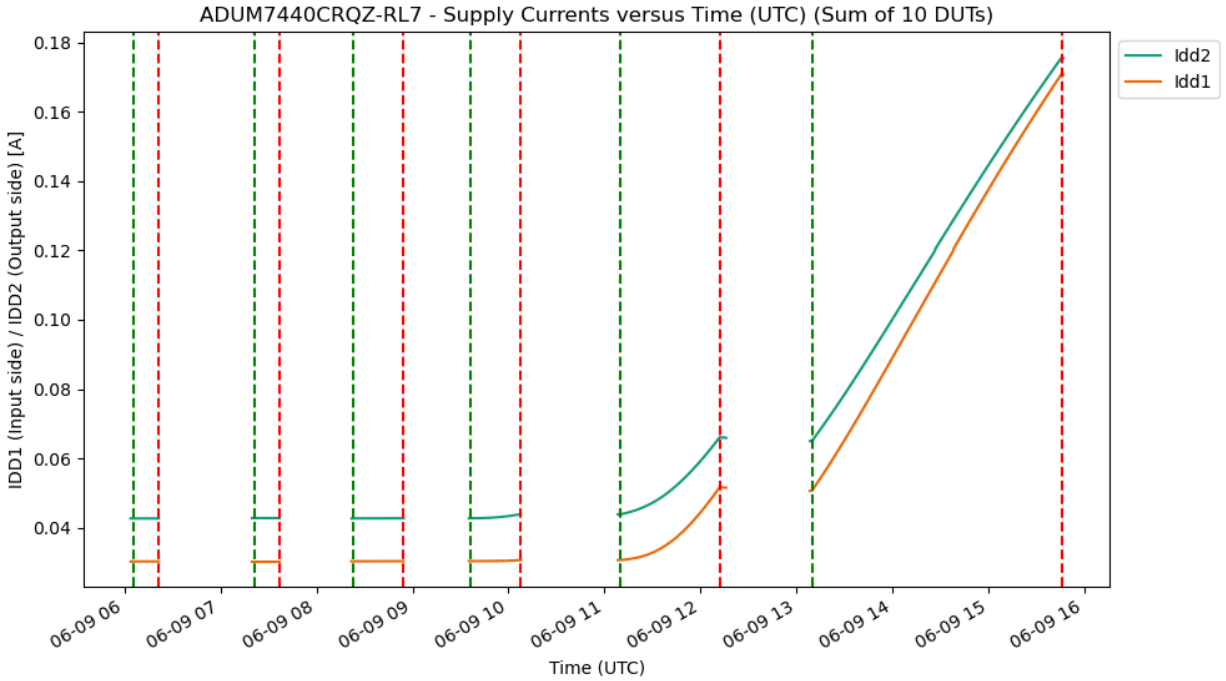


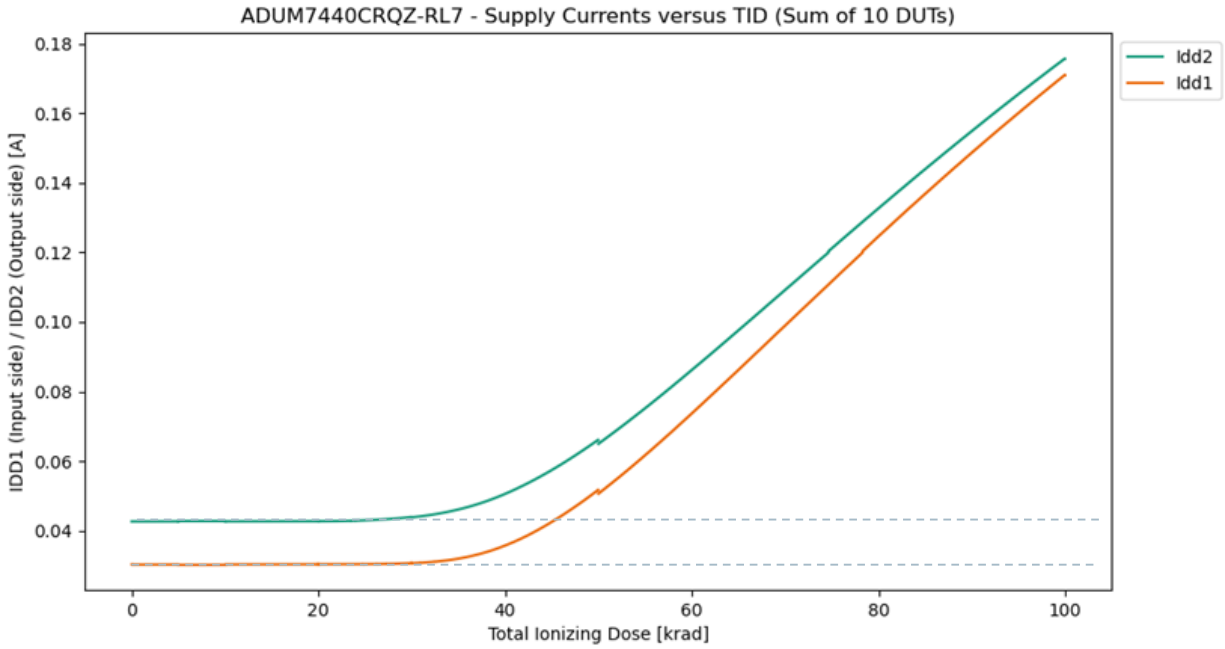
# ADUM7440CRQZ-RL7 Test Results

## 4 Channel Digital Isolator, 1kV

In-situ measurement of supply currents

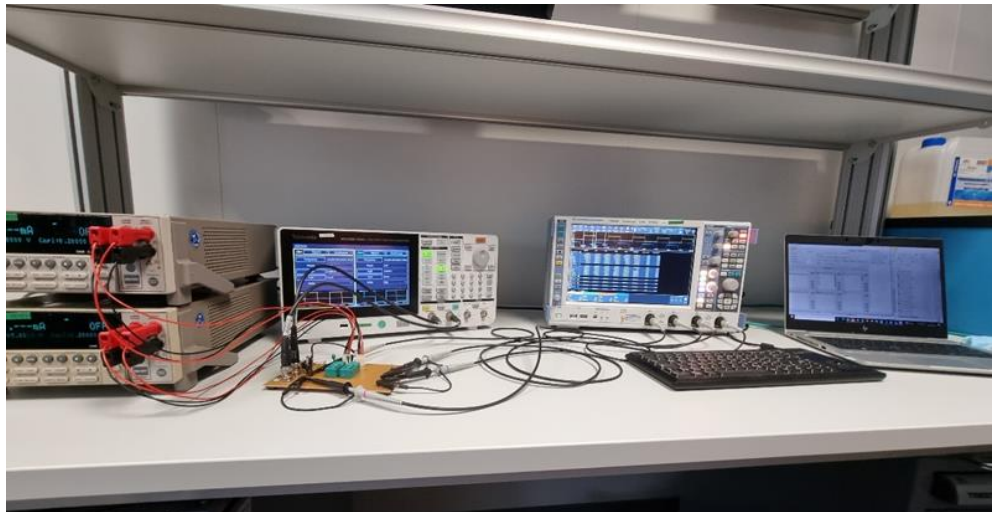
Significant degradation from ~30 krad(Si)

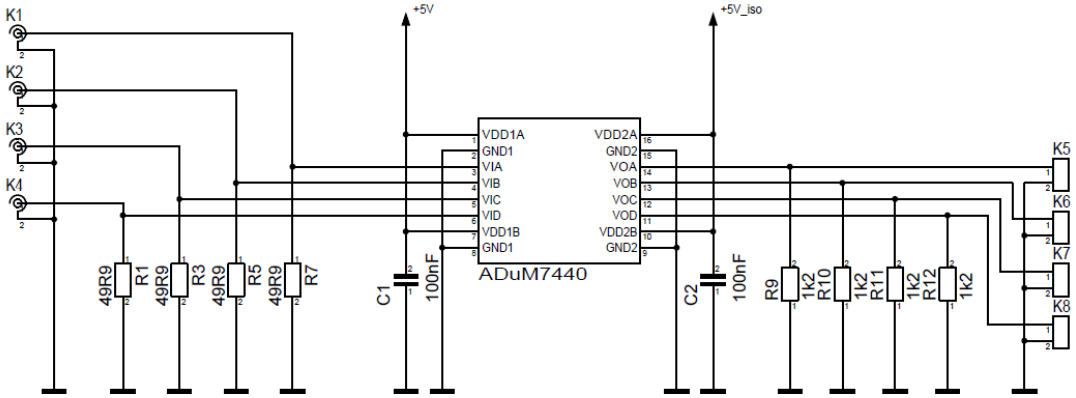


# ADUM7440CRQZ-RL7 Test Results

## 4 Channel Digital Isolator, 1kV





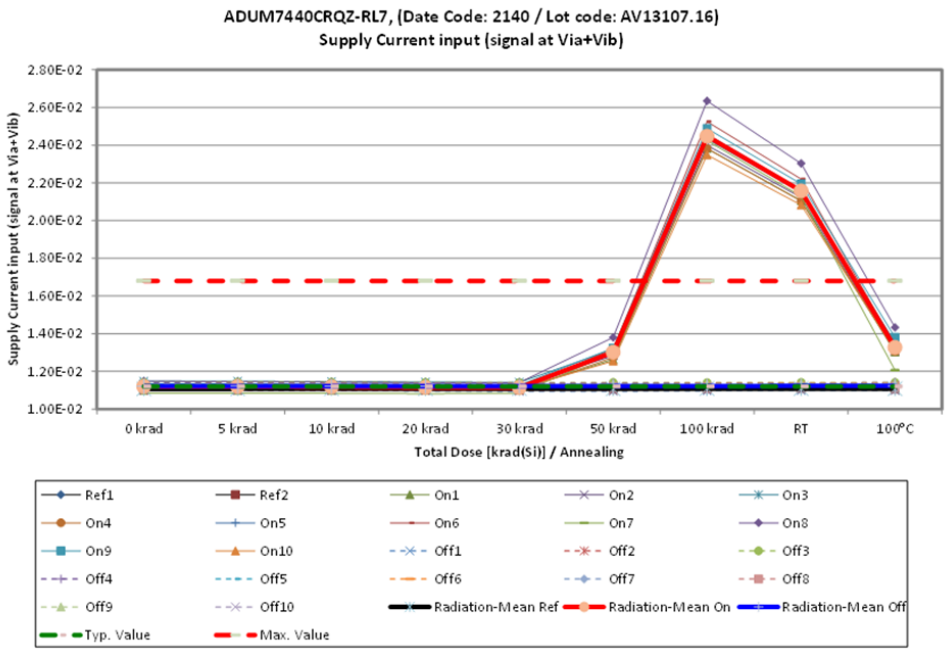

| # | Parameter | Symbol |
|---|---|---|
| 1 | Quiescent Supply Current input (no signal) | IDD_I(Q) |
| 2 | Quiescent Supply Current output (no signal) | IDD_O(Q) |
| 3 | Supply Current input (signal at Via+Vib) | IDD_I(a/b) |
| 4 | Supply Current output (signal at Via+Vib) | IDD_O(a/b) |
| 5 | Output High Level Voa | Voh(a) |
| 6 | Output Low Level Voa | Vol(a) |
| 7 | Output Rise Time Voa | tr(a) |
| 8 | Output Fall Time Voa | Tf(a) |
| 9 | Propagation Delay Via to Voa LOW-> HIGH | tplh(a) |
| 10 | Propagation Delay Via to Voa HIGH-> LOW | tphl(a) |
| 11 | Pos Pulse Width Voa | pPW(a) |
| 12 | Output High Level Vob | Voh(b) |
| 13 | Output Low Level Vob | Vol(b) |
| 14 | Output Rise Time Vob | tr(b) |
| 15 | Output Fall Time Vob | Tf(b) |
| 16 | Propagation Delay Vib to Vob LOW-> HIGH | tplh(b) |
| 17 | Propagation Delay Vib to Vob HIGH-> LOW | tphl(b) |
| 18 | Pos Pulse Width Vob | pPW(b) |
| 19 | Supply Current input (signal at Vic+Vid) | IDD_I(c/d) |
| 20 | Supply Current output (signal at Vic+Vid) | IDD_O(c/d) |
| 21 | Output High Level Voc | Voh(c) |
| 22 | Output Low Level Voc | Vol(c) |
| 23 | Output Rise Time Voc | tr(c) |
| 24 | Output Fall Time Voc | Tf(c) |
| 25 | Propagation Delay Vic to Voc LOW-> HIGH | tplh(c) |
| 26 | Propagation Delay Vic to Voc HIGH-> LOW | tphl(c) |
| 27 | Pos Pulse Width Voc | pPW(c) |
| 28 | Output High Level Vod | Voh(d) |
| 29 | Output Low Level Vod | Vol(d) |
| 30 | Output Rise Time Vod | tr(d) |
| 31 | Output Fall Time Vod | Tf(d) |
| 32 | Propagation Delay Vid to Vod LOW-> HIGH | tplh(d) |
| 33 | Propagation Delay Vid to Vod HIGH-> LOW | tphl(d) |
| 34 | Pos Pulse Width Vod | pPW(d) |

# ADUM7440CRQZ-RL7 Test Results

## 4 Channel Digital Isolator, 1kV

No significant changes in parameters except Supply currents

| Pass/Fail | | Total Dose [krad (Si)] | | | | | | | Annealing | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 krad | 5 krad | 10 krad | 20 krad | 30 krad | 50 krad | 100 krad | RT | 100C |
| Functional | On | | | | | | | | | |
| | Off | | | | | | | | | |
| IDD_I(Q) | On | | | | | | 8 | 10 | 10 | 9 |
| | Off | | | | | | | | | |
| IDD_O(Q) | On | | | | | | 10 | 10 | 10 | |
| | Off | | | | | | | | | |
| IDD_I(a/b + c/d) | On | | | | | | | 10 | 10 | |
| | Off | | | | | | | | | |
| IDD_O(a/b + c/d) | On | | | | | | | 10 | 10 | |
| | Off | | | | | | | | | |
| Voh(a/b/c/d) | On | | | | | | | | | |
| | Off | | | | | | | | | |
| Vol(a/b/c/d) | On | | | | | | | | | |
| | Off | | | | | | | | | |
| tr(a/b/c/d) | On | | | | | | | | | |
| | Off | | | | | | | | | |
| tf(a/b/c/d) | On | | | | | | | | | |
| | Off | | | | | | | | | |
| pPW(a/b/c/d) | On | | | | | | | | | |
| | Off | | | | | | | | | |
| tplh(a/b/c/d) | On | | | | | | | | | |
| | Off | | | | | | | | | |
| tphl(a/b/c/d) | On | | | | | | | | | |
| | Off | | | | | | | | | |



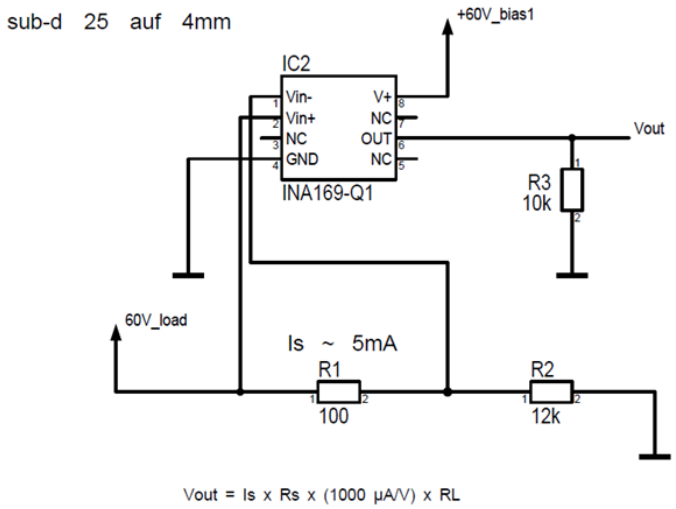
# INA169QPWRQ1 Test Results

## Automotive-Grade, High-Side, Current-Output, current-Shunt Monitor

The INA169-Q1 is an AEC-Q100 qualified automotive-grade unidirectional current shunt monitor with wide input common-mode voltage range.

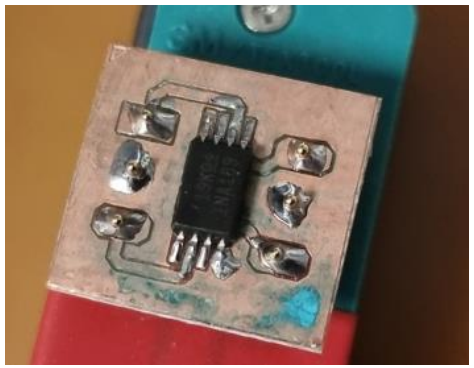
A differential input voltage, i.e. the voltage drop across a defined shunt resistor, and the corresponding current is converted to an output voltage.

$$V_{Out} = (R_S\, I_s)\, g_m\, R_L = (V_{IN+} - V_{IN-})\, g_m\, R_L$$




| Bias Configuration: Static (only @ Standard rate) |
|---|
| V+ = 60 V (worst case bias) |
| $V_{IN+}$ = 60 V (worst case at load) |
| 10 samples |

| Unbiased (Standard and Low rate tests) |
|---|
| All Pins grounded |



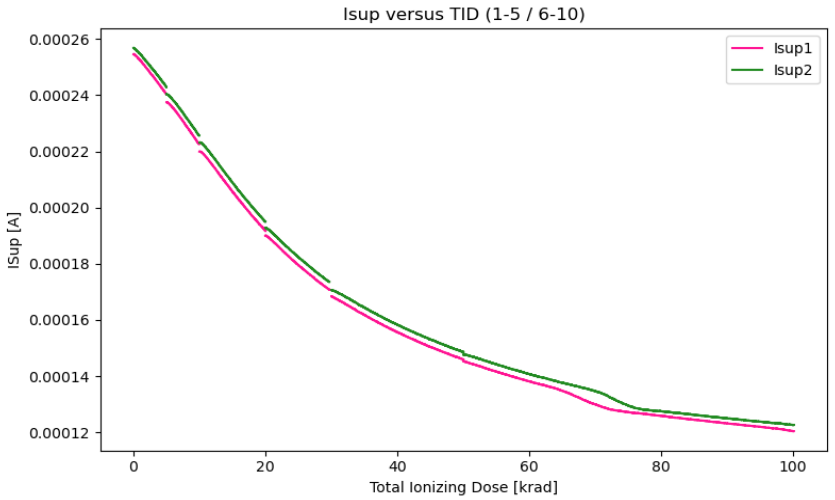
# INA169QPWRQ1 Test Results

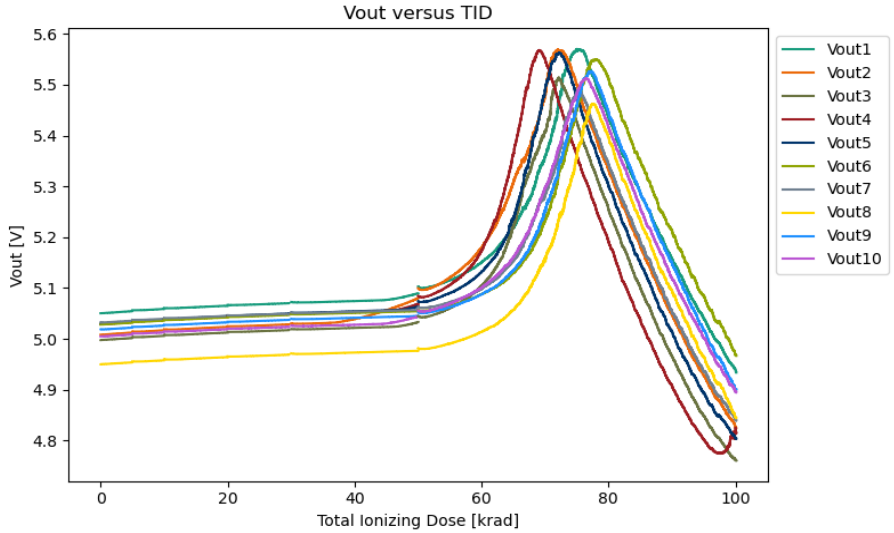
## Automotive-Grade, High-Side, Current-Output, current-Shunt Monitor

Monitoring of supply currents (DUTs on1-on5 & on6-on10)

Monitoring of all 10 Vout during irradiation and room temp. annealing.
Only 1 Vout monitored throughout the 100°C annealing.

From the parameter characterization:
As unbiased samples showed worse degradation, only this mode was included at low dose rate test.

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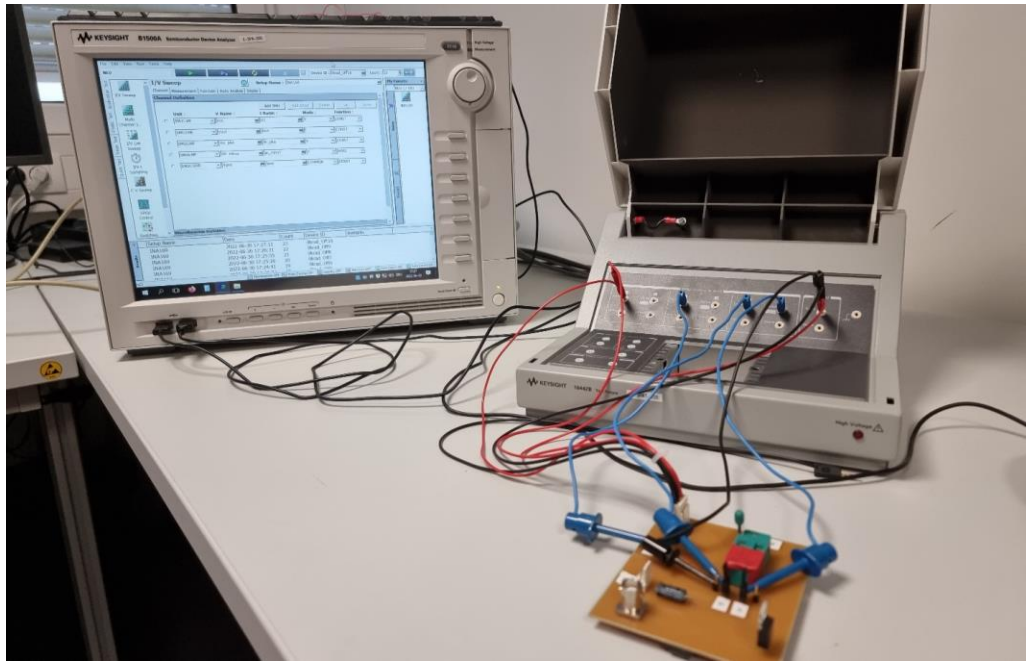
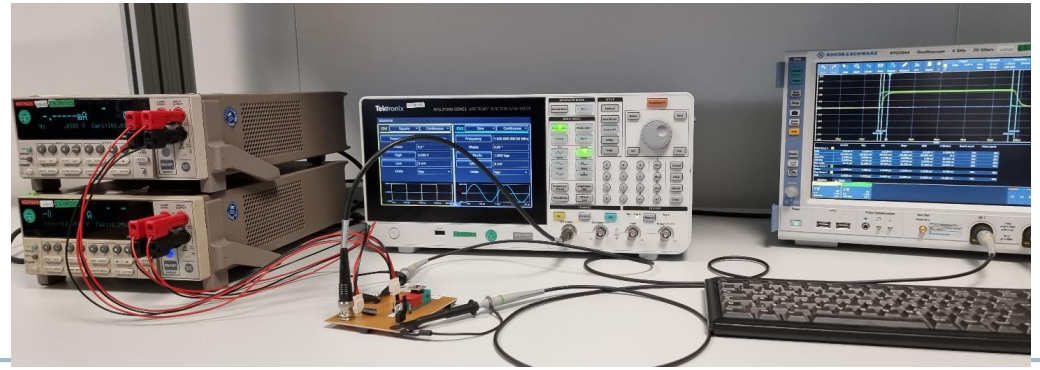
# INA169QPWRQ1 Test Results

## Automotive-Grade, High-Side, Current-Output, current-Shunt Monitor





| # | Parameter | Symbol | |
|---|---|---|---|
| 1 | Quiescent Supply Current input (Vsense=0) | I(Q) | |
| 2 | Input Supply Current (Vsense = 500 mV) | I(sup) | |
| 3 | Output voltage versus Vsense (0-500 mV) | Vout(Sense) | |
| 4 | Output voltage High Level | Vout_H(Step) | |
| 5 | Output voltage Low Level | Vout_L(Step) | |
| 6 | Rise time | tr(Step) | |
| 7 | Fall time | tf (Step) | |
| 8 | Pulse width | pw(Step) | |
| 9 | Propagation delay L→H | propLH | |
| 10 | Propagation delay H→L | propHL | |
| (11) | Transconductance (Vsense = 10 to 150 mV) | g_m | From Data evaluation |
| (12) | Nonlinearity error (Vsense = 10 to 150 mV) | errlin | |
| (12) | Total output error (Vsense = 100 mV) | errout | |

# INA169QPWRQ1 Test Results

## Automotive-Grade, High-Side, Current-Output, current-Shunt Monitor

| Pass/Fail | | Total Dose [krad (Si)] | | | | | | | Annealing | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 krad | 5 krad | 10 krad | 20 krad | 30 krad | 50 krad | 100 krad | RT | 100C |
| Functional | On | | | | | | | | | F:1 / P:9 |
| | Off | | | | | | | | | |
| I(Q) | On | | | | | | | | | F:1 / P:9 |
| | Off | | | | | | | | | |
| I(sup) | On | | | | | | | | | F:1 / P:9 |
| | Off | | | | | | | | | |
| Vout(Sense) | On | | | | | | | 9 | | F:1 / P:9 |
| | Off | | | | | | | 10 | | |
| Vout_H(Step) | On | | | | | | | | | F:1 / P:9 |
| | Off | | | | | | | | | |
| Vout_L(Step) | On | | | | | | | | | F:1 / P:9 |
| | Off | | | | | | | | | |
| tr(Step) | On | | | | | | | | | F:1 / P:9 |
| | Off | | | | | | | 10 | 10 | |
| tf (Step) | On | | | | | | | 10 | | F:1 / P:9 |
| | Off | | | | | | | 10 | 10 | |
| pw(Step) | On | | | | | | | | | F:1 / P:9 |
| | Off | | | | | | | | | |
| propLH (Step) | On | | | | | | | 10 | | F:1 / P:9 |
| | Off | | | | | | 10 | 10 | 10 | |
| propHL (Step) | On | | | | | | | | | F:1 / P:9 |
| | Off | | | | | | | | | |
| g_m | On | | | | | | | | | F:1 / P:9 |
| | Off | | | | | | | 9 | 10 | |
| errlin | On | | | | | | | | | F:1 / P:9 |
| | Off | | | | | | | | | |
| errout | On | | | | | | | 1 | | F:1 / P:9 |
| | Off | | | | | | | | | |

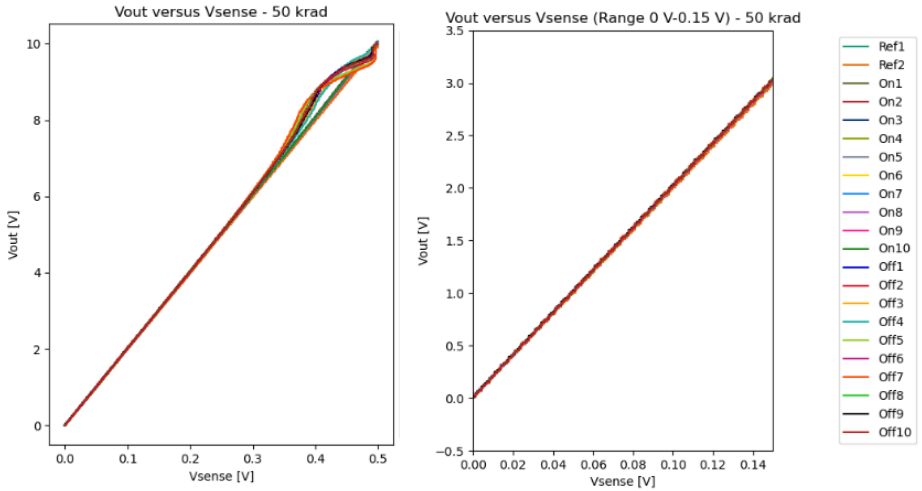
| Pass/Fail | | Total Dose [krad (Si)] | | | | | Annealing | |
|---|---|---|---|---|---|---|---|---|
| | | 0 krad | 18.8 krad | 33.2 krad | 67 krad | 99.6 krad | RT | 100C |
| Functional | Off | | | | | | | |
| I(Q) | Off | | | | | | | |
| I(sup) | Off | | | | | | | |
| Vout(Sense) | Off | | | | 10 | 10 | 10 | |
| Vout_H(Step) | Off | | | | | 10 | 10 | |
| Vout_L(Step) | Off | | | | | | | |
| tr(Step) | Off | | | | 10 | 10 | 10 | |
| tf (Step) | Off | | | | 10 | 10 | 10 | |
| pw(Step) | Off | | | | | | | |
| propLH (Step) | Off | | | 10 | 10 | 10 | 10 | 9 |
| propHL (Step) | Off | | | | | 10 | 10 | |
| g_m | Off | | | | 7 | 10 | 10 | |
| errlin | Off | | | | | 10 | 10 | |
| errout | Off | | | | 5 | 10 | 10 | |

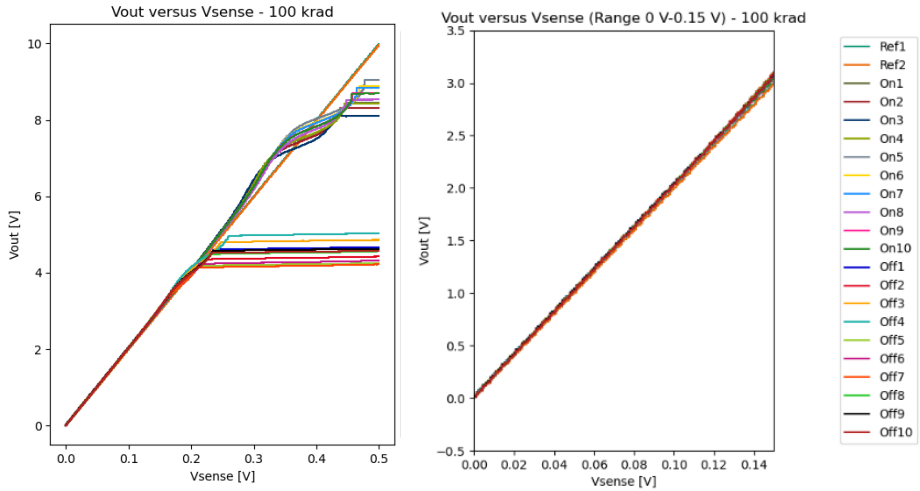
- LDR test with different  dose levels for intermediate tests
- At HDR 100°C annealing showed a severe negative impact (incl. 1 functional failure)

# INA169QPWRQ1 Test Results

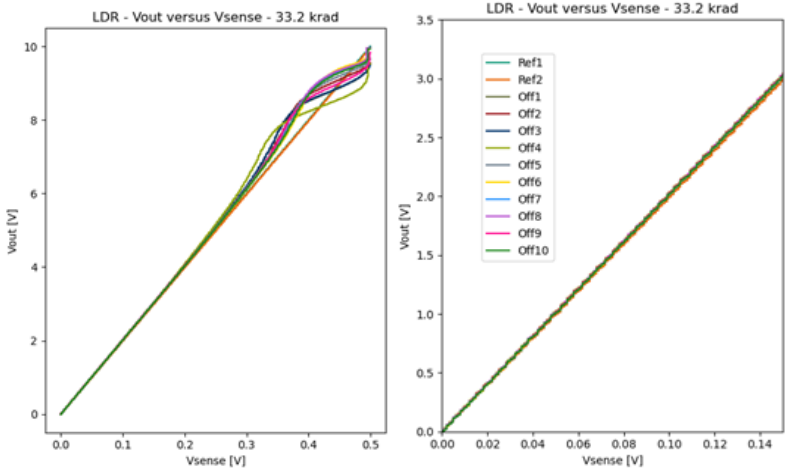
## Automotive-Grade, High-Side, Current-Output, current-Shunt Monitor

- Standard Rate

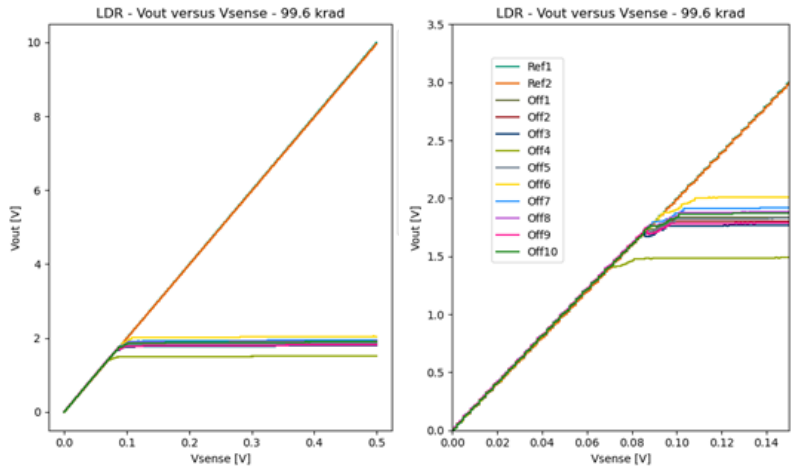



- Low Rate



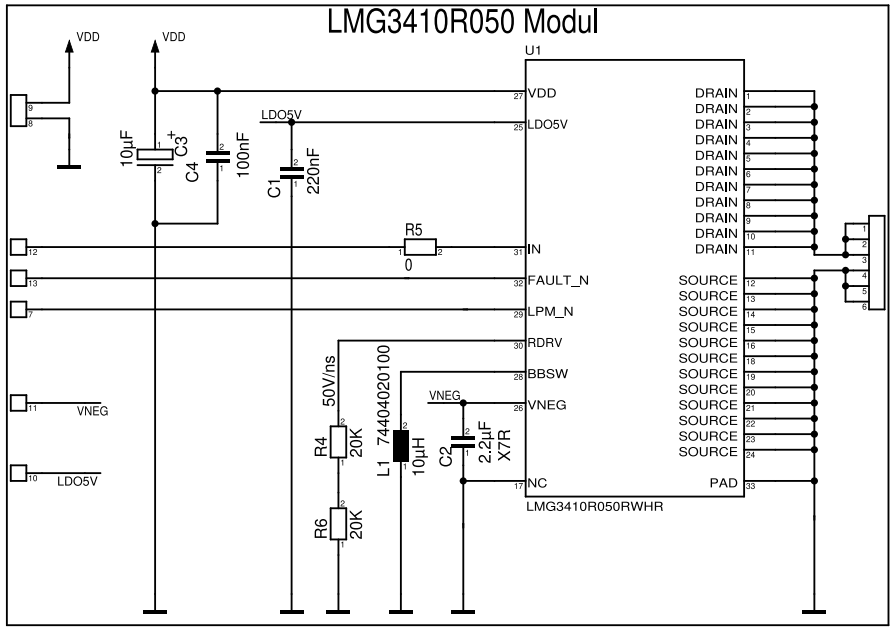

- *The INA169 can be used over the range Vsense 0 →0.5V*
- *However the manufacturer recommends staying within 0→0.15 V*



# LMG3410R050RWHT Test Results

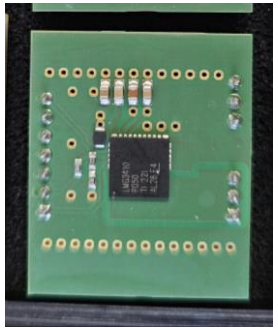
## Gate Drivers 600 V GaN with integrated driver and protection

- Control the internal GaN FET once it is powered up.
- Includes overcurrent and overtemperature protection and undervoltage protection.
- a series silicon FET turns the GaN module off if VDD is not supplied
- When off, the series FET blocks the drain voltage or, in case it is switched off during operation, enforces the VGS of the GaN to move below the threshold voltage.
- When the device is powered up, VNEG (generated by a buck-boost converter) turns on the GaN. The silicon FET then switches the gate between VNEG and its SOURCE pin voltage.
- An internal LDO can deliver up to 5 mA to an external load.
- The device has a low power mode which, when LPM pin is pulled low, disables the internal buck-boost converter



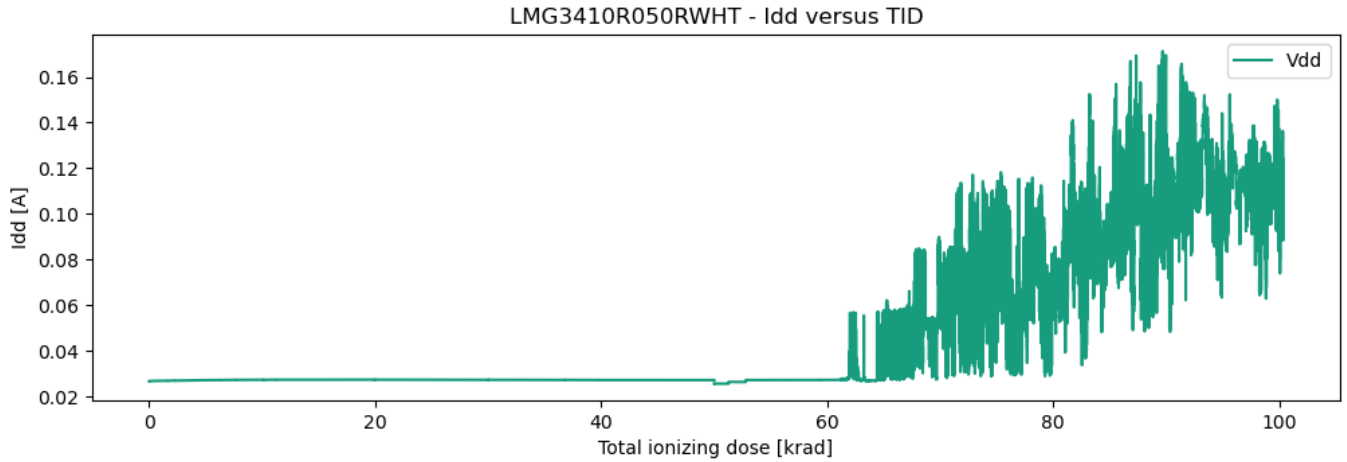

| Bias Configuration: Static |
|---|
| Vdd = 12 V,<br>Vdrain = 600 V |

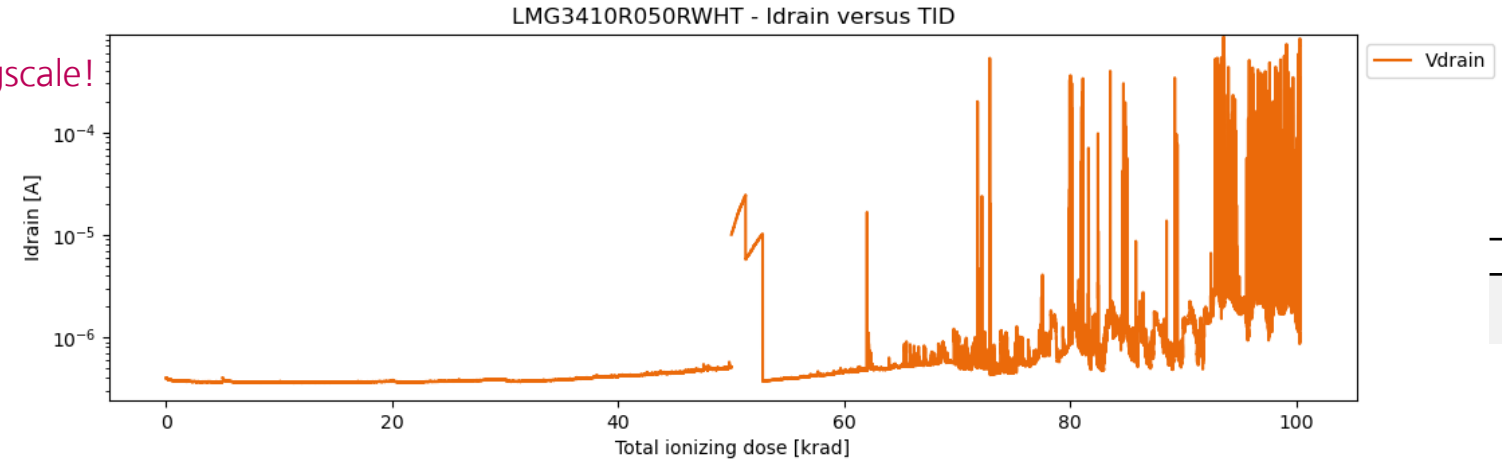
| Unbiased |
|---|
| 5 samples, All Pins grounded |



# LMG3410R050RWHT

## Gate Drivers 600 V GaN with integrated driver and protection




- Logscale!

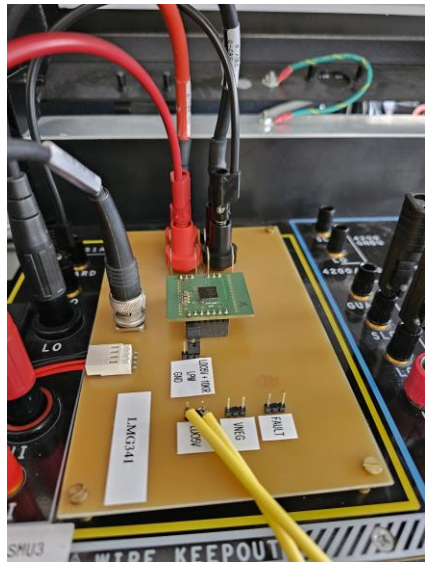
- Idd and Idrain show high volatility >60 krad
- High current state was triggered upon power up at 50 krad intermediate step

| # | Parameter | Symbol | Conditions |
|---|---|---|---|
| 01 | Supply current | Idd | Vdd = 12V, Sum of supply currents DUTs ON 1-5 |
| 02 | Drain current | Idrain | Vdrain = 600V, Sum of drain currents DUTs ON 1-5 |

# LMG3410R050RWHT

## Gate Drivers 600 V GaN with integrated driver and protection

- Set of test parameters cover electrical characteristics
  - (switching would require equipment applying ~100 V/ns, do-able, but complex)



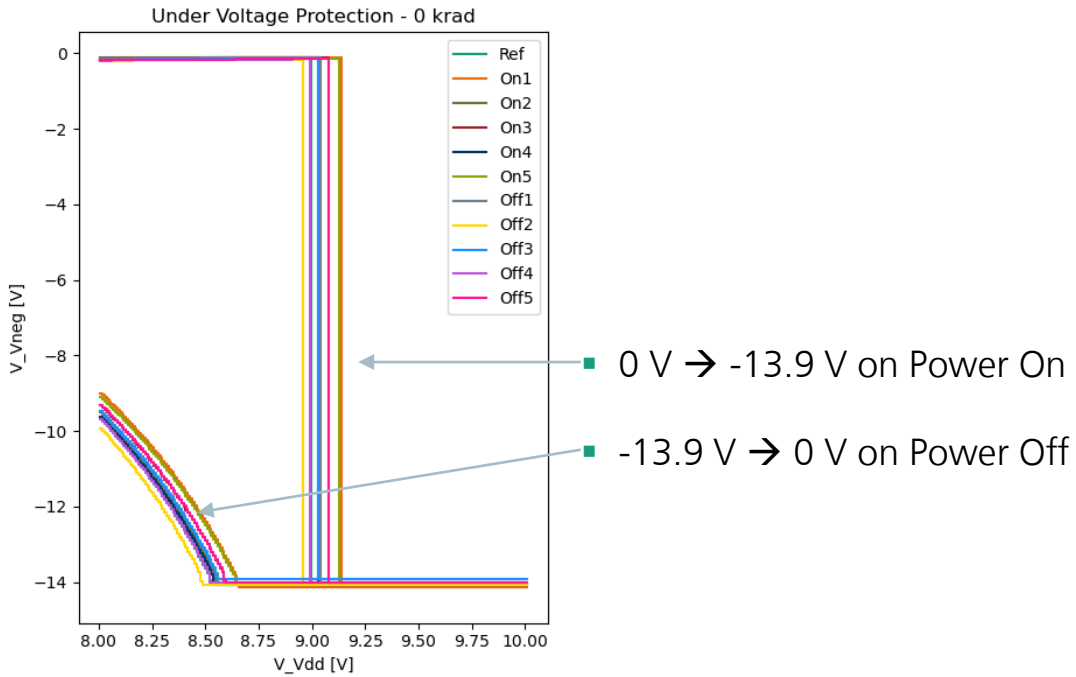
| Pass/Fail LMG3401 | | Total Dose [krad (Si)] | | | | | | | Annealing | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 krad | 5 krad | 10 krad | 20 krad | 30 krad | 50 krad | 100 krad | RT | 100C |
| Functional | On | | | | | | F:3 | F:5 | | |
| | Off | | | | | | | | | |
| Idd_LPM | On | | | | | | 5 | 5 | 4 | |
| | Off | | | | | | | | | |
| Idd_Q_off | On | | | | | | | 4 | | |
| | Off | | | | | | | | | |
| Idd_Q_on | On | | | | | | | 4 | | |
| | Off | | | | | | | | | |
| Idd_op | On | | | | | | | | | |
| | Off | | | | | | | | | |
| V_LDO5V | On | | | | | | | | | |
| | Off | | | | | | | | | |
| Vneg | On | | | | | | 3 | 5 | 5 | 5 |
| | Off | | | | | | | 5 | 5 | 5 |
| VDD,(on) | On | | | | | | F:3 | F:5 | | |
| | Off | | | | | | | | | |
| VDD,(off) | On | | | | | | F:3 | F:5 | | |
| | Off | | | | | | | | | |
| Idss | On | | | | | | 2 | 2 | | |
| | Off | | | | | | | | | |
| RDS_on | On | | | | | | 2 | 3 | | |
| | Off | | | | | | | | | |

| # | Parameter | Symbol |
|---|---|---|
| 1 | Quiescent current, ultra-low-power mode | Idd_LPM |
| 2 | Quiescent current (Transistor off) | Idd_Q_off |
| 3 | Quiescent current (Transistor on) | Idd_Q_on |
| 4 | Operating current (fsw = 500 KHz) | Idd_op |
| 5 | 5V LDO output voltage | V_LDO5V |
| 6 | Negative Supply voltage (20 mA load current) | Vneg |
| 7 | VDD turnon threshold | VDD,(on) |
| 8 | VDD turnoff threshold | VDD,(off) |
| 9 | Drain leakage current (Vds = 600V, Tj = 25°C) | Idss |
| 10 | On-state Resistance (no condition on IDS set in datasheet, IDS = 10A chosen) | RDS_on |

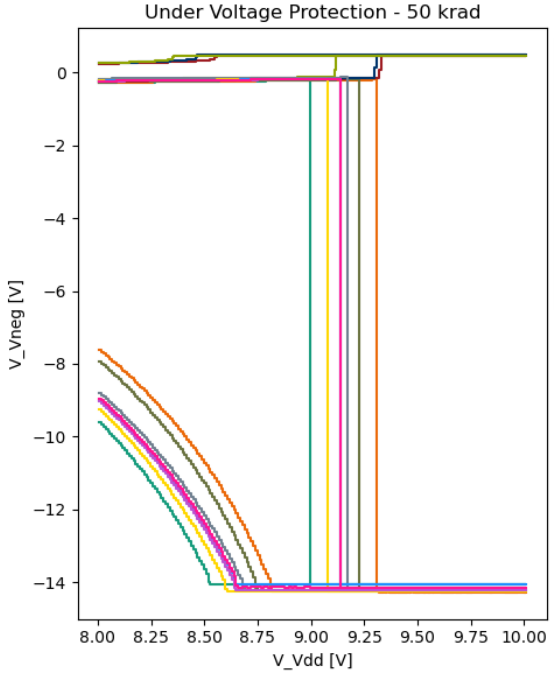
# LMG3410R050RWHT

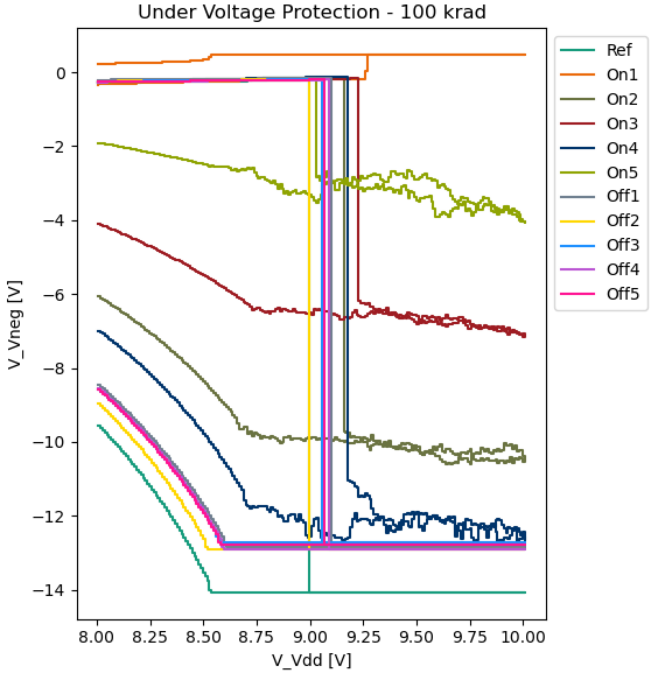
## Gate Drivers 600 V GaN with integrated driver and protection

- Loss of functionality best visible when looking at the undervoltage tests
- Unbiased samples show a shift in voltage level
- Some biased samples do not turn the GaN on or not to the specified range




- 0 V → -13.9 V on Power On
- -13.9 V → 0 V on Power Off



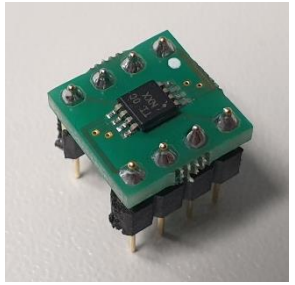
# Operational Amplifiers Test Results

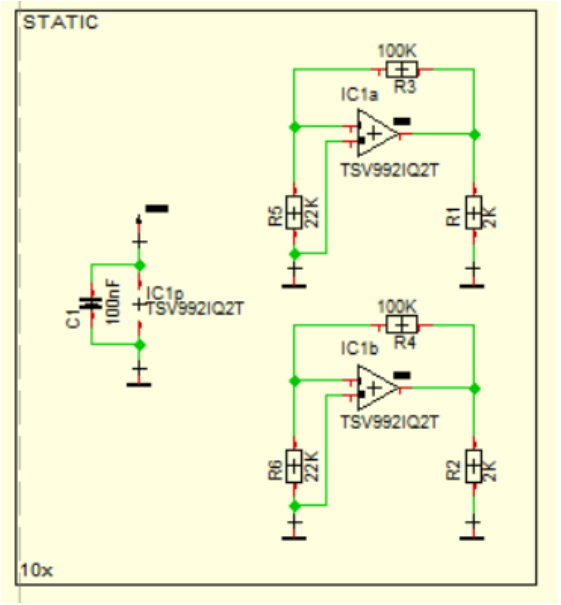
## THS4032MDGNREP / TSV992IQ2T / TSZ182HYDT

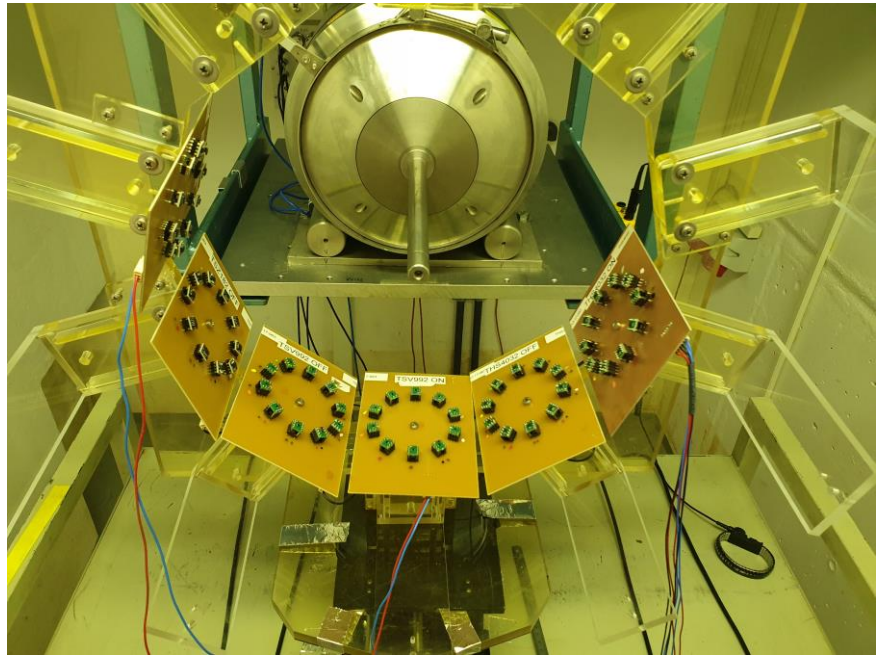
| Device under test | Manufacturer |
|---|---|
| **THS4032MDGNREP** | Texas Instruments |
| **TSV992IQ2T** | STMicroelectronics |
| **TSZ182HYDT** | STMicroelectronics |

| # | Device | Parameter | Symbol | Conditions |
|---|---|---|---|---|
| 01 | TSV992 | Supply current | $I_{CC}$ | $V_{CC}$ = 5 V |
| 02 | TSZ182H | Supply current | $I_{CC}$ | $V_{CC}$ = 5 V |
| 03 | THS4032 | Output voltage | $I_{CC}$ | $V_{CC}$ = ± 15 V |

Dual OpAmps with identical package / pin layout





# Operational Amplifiers Test Results

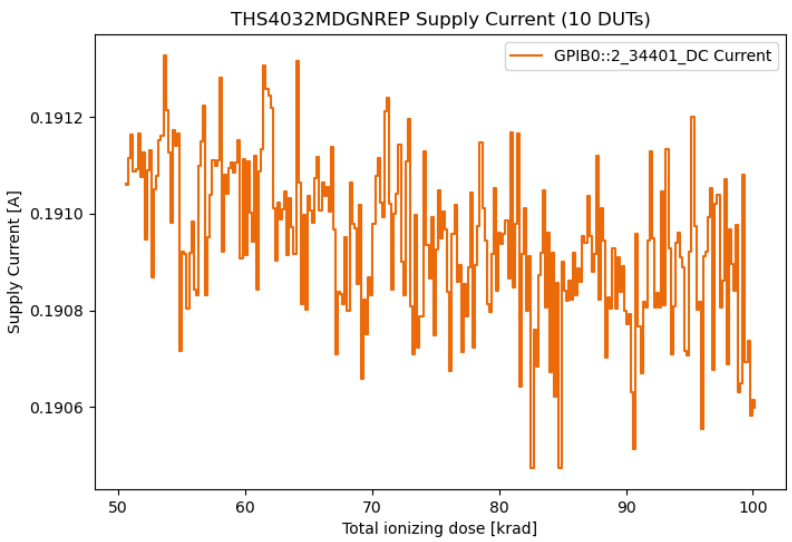
## THS4032MDGNREP / TSV992IQ2T / TSZ182HYDT

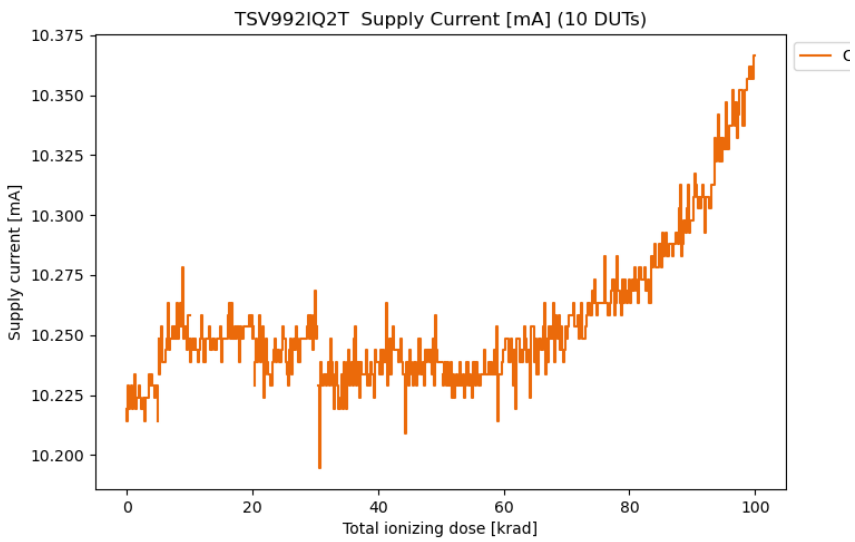
TSV992IQ2T / THS4032MDGNREP: minor or no degradation

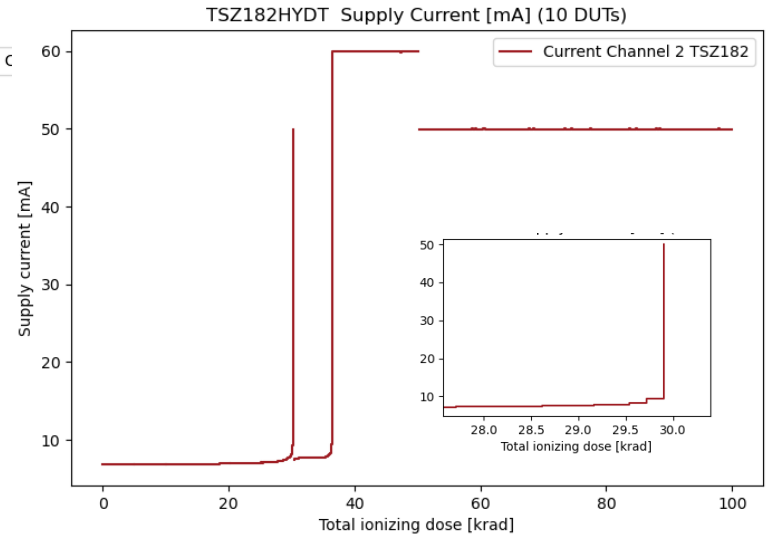
TSZ182HYDT:

triggers into high current state at 30 krad, resets during intermediate test, triggers again at 36 krad, doesn't reset

| # | Device | Parameter | Symbol | Conditions |
|---|---|---|---|---|
| 01 | TSV992 | Supply current | $I_{CC}$ | $V_{CC}$ = 5 V |
| 02 | TSZ182H | Supply current | $I_{CC}$ | $V_{CC}$ = 5 V |
| 03 | THS4032 | Output voltage | $I_{CC}$ | $V_{CC}$ = ± 15 V |




  **Public information**

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# Operational Amplifiers Test Results

## THS4032MDGNREP / TSV992IQ2T / TSZ182HYDT

| THS4031-EP | biased | | unbiased | |
|---|---|---|---|---|
| Parameter | $V_{CC}$ = ± 15 V | $V_{CC}$ = ± 5 V | $V_{CC}$ = ± 15 V | $V_{CC}$ = ± 5 V |
| Supply Current | 100 krad | 100 krad | 100 krad | 100 krad |
| Input Bias Current | 100 krad | 100 krad | 100 krad | 100 krad |
| Input Offset Voltage | 100 krad | 100 krad | 100 krad | 100 krad |
| Input Offset Current | 100 krad | 100 krad | 100 krad | 100 krad |
| Short-Circuit Current | 100 krad | | 100 krad | |
| Output Voltage 1 | 100 krad | 100 krad | 100 krad | 100 krad |
| Output Voltage 2 | 100 krad | 100 krad | 100 krad | 100 krad |
| Common Mode Rejection Ratio | 100 krad | 100 krad | 100 krad | 100 krad |
| Power Supply Rejection Ratio | 100 krad | 100 krad | 100 krad | 100 krad |
| Large Signal Voltage Gain | 100 krad | 100 krad | 100 krad | 100 krad |
| Small Signal Bandwidth | 100 krad | 100 krad | 100 krad | 100 krad |
| Slew Rate | 100 krad | (100 krad)* | 100 krad | 100 krad |
| | | *single parametric failure during RT annealing | | |


| TSV991 | biased | | | unbiased | | |
|---|---|---|---|---|---|---|
| Parameter | $V_{CC+}$ = 5 V | $V_{CC+}$ = 3.3 V | $V_{CC+}$ = 2.5 V | $V_{CC+}$ = 5 V | $V_{CC+}$ = 3.3 V | $V_{CC+}$ = 2.5 V |
| Supply Current | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad |
| Input Bias Current | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad |
| Input Offset Voltage | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad |
| Input Offset Current | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad |
| High Level Output Voltage 1 | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad |
| High Level Output Voltage 2 | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad |
| Low Level Output Voltage 1 | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad |
| Low Level Output Voltage 2 | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad |
| Common Mode Rejection Ratio | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad | 100 krad |
| Power Supply Rejection Ratio | 100 krad | | | 100 krad | | |
| Large Signal Voltage Gain | 100 krad | x | 100 krad | 100 krad | 100 krad | 100 krad |
| Gain Bandwith Product | 100 krad | x | 100 krad | 100 krad | 100 krad | 100 krad |
| Slew Rate | 30 krad | 30 krad | 100 krad | 50 krad | 50 krad | 100 krad |

| TSZ181H | biased | | | unbiased | | |
|---|---|---|---|---|---|---|
| Parameter | $V_{CC+}$ = 5 V | $V_{CC+}$ = 3.3 V | $V_{CC+}$ = 2.2 V | $V_{CC+}$ = 5 V | $V_{CC+}$ = 3.3 V | $V_{CC+}$ = 2.2 V |
| Supply Current | 30 krad | 30 krad | 30 krad | 100 krad | 100 krad | 100 krad |
| Input Bias Current | 30 krad | 30 krad | 30 krad | 100 krad | 100 krad | 100 krad |
| Input Offset Voltage | 30 krad | 30 krad | 30 krad | 100 krad | 100 krad | 100 krad |
| Input Offset Current | 30 krad | 50 krad | 30 krad | 100 krad | 100 krad | 100 krad |
| High Level Output Voltage | 30 krad | 30 krad | 30 krad | 100 krad | 100 krad | 100 krad |
| Low Level Output Voltage | 30 krad | 100 krad | 30 krad | 100 krad | 100 krad | 100 krad |
| Common Mode Rejection Ratio 1 | 30 krad | 30 krad | 30 krad | 100 krad | 100 krad | 100 krad |
| Common Mode Rejection Ratio 2 | 30 krad | 30 krad | 30 krad | 100 krad | 100 krad | 100 krad |
| Power Supply Rejection Ratio | 30 krad | | | 100 krad | | |
| Large Signal Voltage Gain | 30 krad | 30 krad | 30 krad | 100 krad | 100 krad | 100 krad |
| Gain Bandwith Product | 30 krad | 30 krad | 30 krad | 100 krad | 100 krad | 100 krad |
| Slew Rate | 30 krad | 30 krad | 30 krad | 100 krad | 100 krad | 100 krad |

- Indicated is the last „good“ intermediate test

| Equipment | Manufacturer | Model |
|---|---|---|
| Mixed Signal Test Platform | UNITES Systems | UNIMET2020 |
| Frontadapter “TA39” | UNITES Systems | TA39 |

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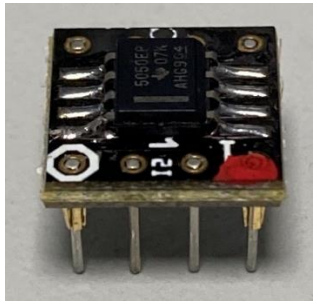
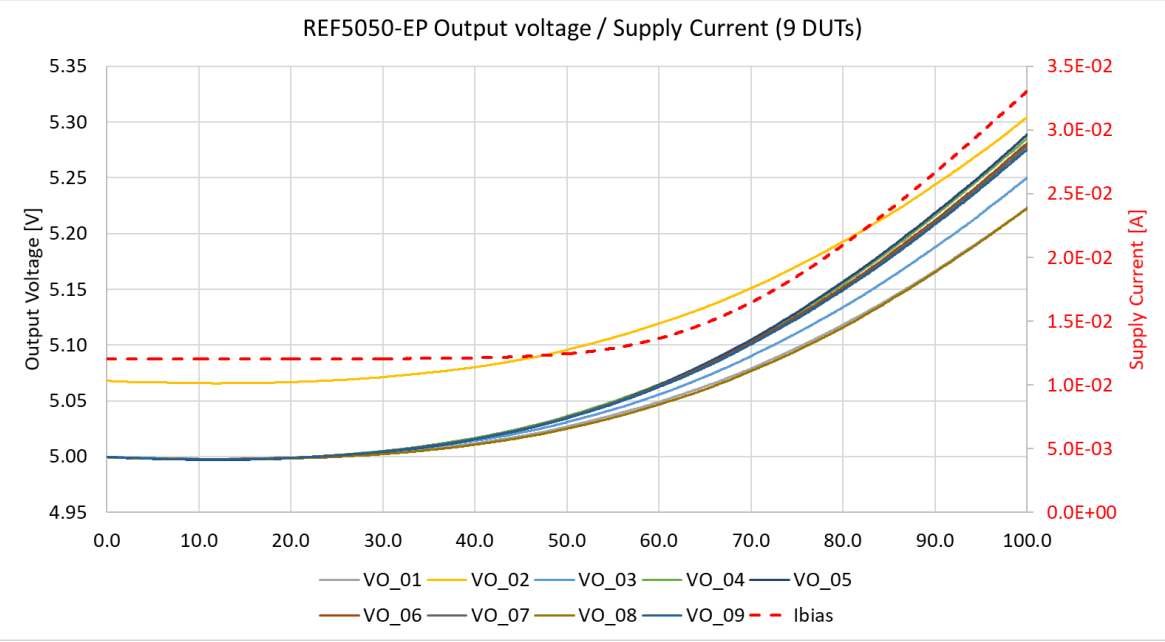
# REF5050MDREP TID-Test Results

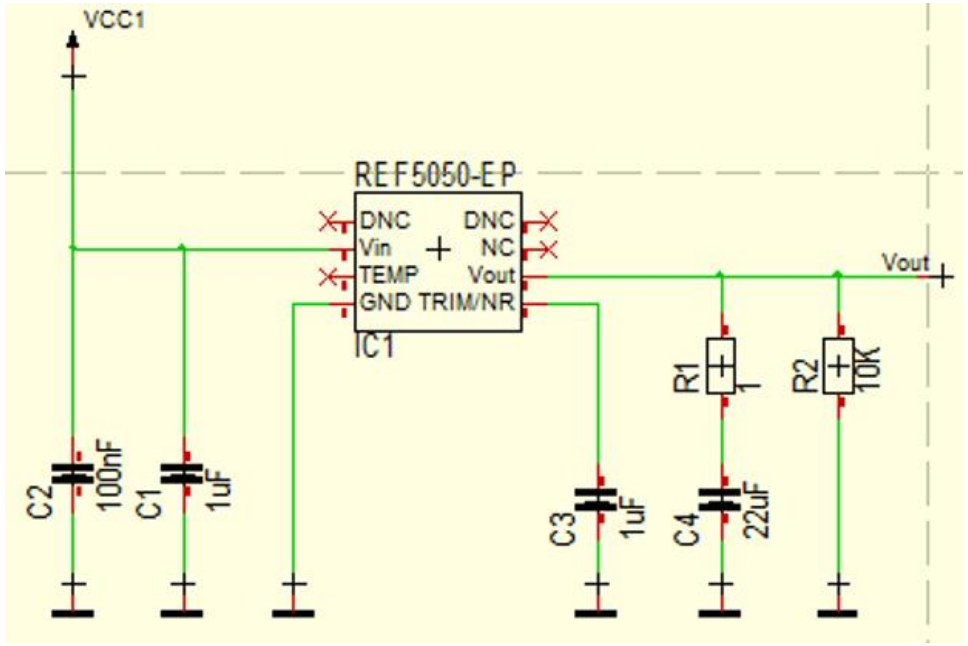
## Voltage Reference

| Bias Configuration: Static (10 samples) | Unbiased (10 samples) |
|---|---|
| $V_{IN}$ = 15V | All Pins grounded |



The REF5050-EP is a high precision voltage reference with a low-noise and a very low-drift. These references are capable of both sinking and sourcing and are supposedly robust with regard to line and load changes.



# REF5050MDREP TID-Test Results

## Voltage Reference

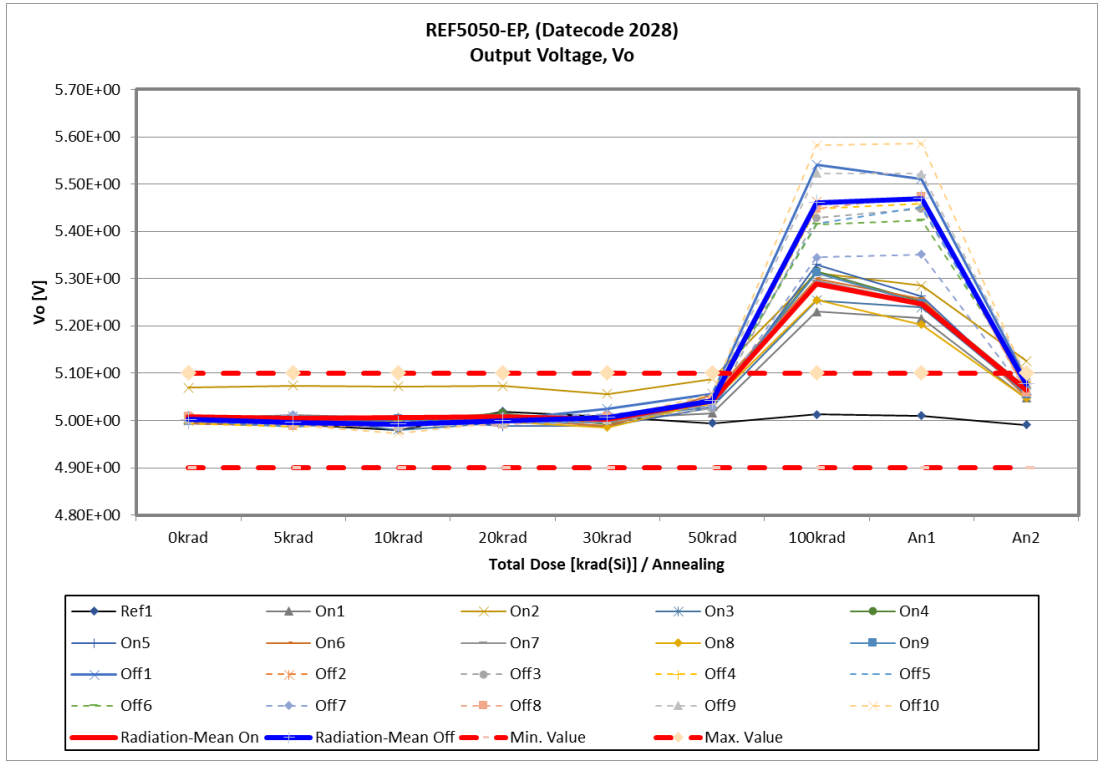
| REF5050-EP | $V_{IN}$ = ($V_{OUT}$ + 0.2 V) = 5.2 V, $I_{LOAD}$ = 0 |
|---|---|
| **Parameter** | **Test Conditions** |
| Output voltage | |
| Line regulation | $V_{IN}$ = 5.2 to 18 V, $I_{LOAD}$ = 10 mA |
| Load regulation | $I_{LOAD}$ = 2 to 10 mA |
| Short circuit current | |
| Quiescent current | |

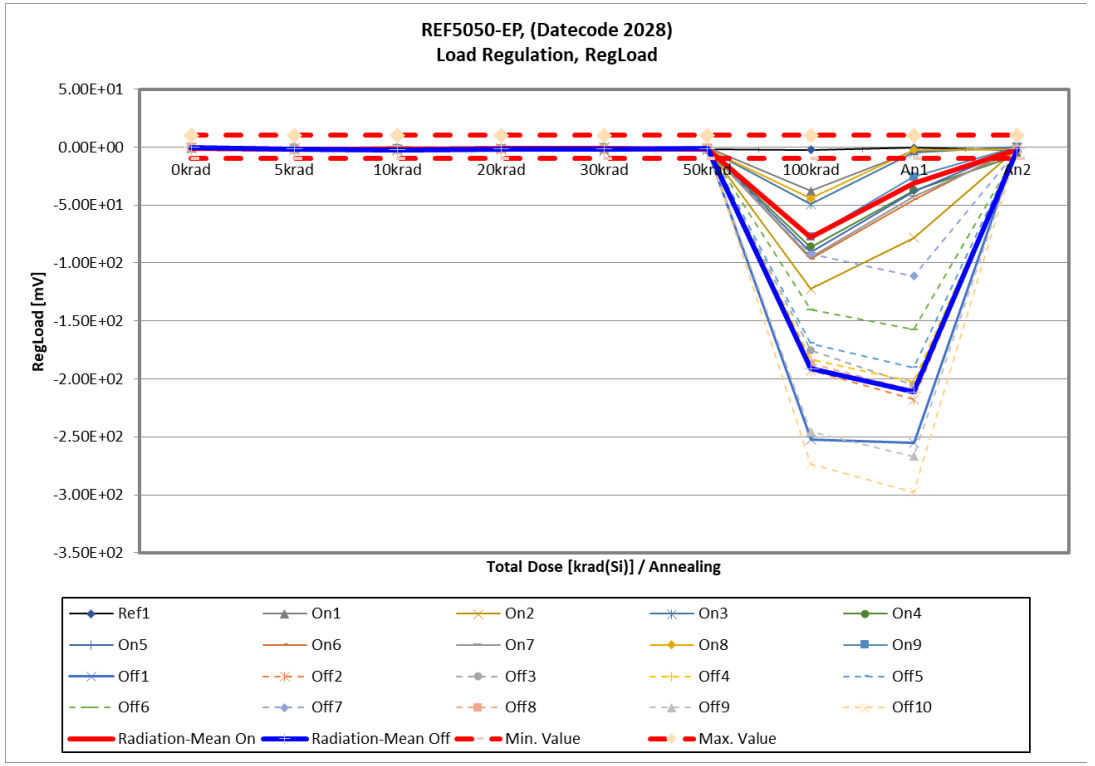

| Pass/Fail REF5050-EP | | Total Dose [krad (Si)] | | | | | | | Annealing | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | 0 krad | 5 krad | 10 krad | 20 krad | 30 krad | 50 krad | 100 krad | RT | 100C |
| Functional | On | | | | | | | | | |
| | Off | | | | | | | | | |
| Vo | On | | | | | | | 9 | 9 | 1 |
| | Off | | | | | | | 10 | 10 | |
| Line Regulation | On | | | | | | | | | |
| | Off | | | | | | | | | |
| Load Regulation | On | | | | | | | 9 | 6 | |
| | Off | | | | | | | 9 | 10 | |
| ISC | On | | | | | | | 9 | 9 | |
| | Off | | | | | | | | | |

# REF5050MDREP TID-Test Results

## Voltage Reference

- Caveat: BiCMOS tested at 10 krad(Si)/h



# IRF9540NPBF TID-Test Results

## MOSFET P-Channel 100V


Infineon/International Rectifier IRF9540NPbF
100 V power p channel MOSFET
$I_D$ = 23 A current
$R_{DS(on)}$ = 0.117 Ohm.

3 date codes

Per Date Code:

- 10 biased
- 10 unbiased
- 1 control / reference sample

- → 60 DUTs irradiated and tested simultaneously

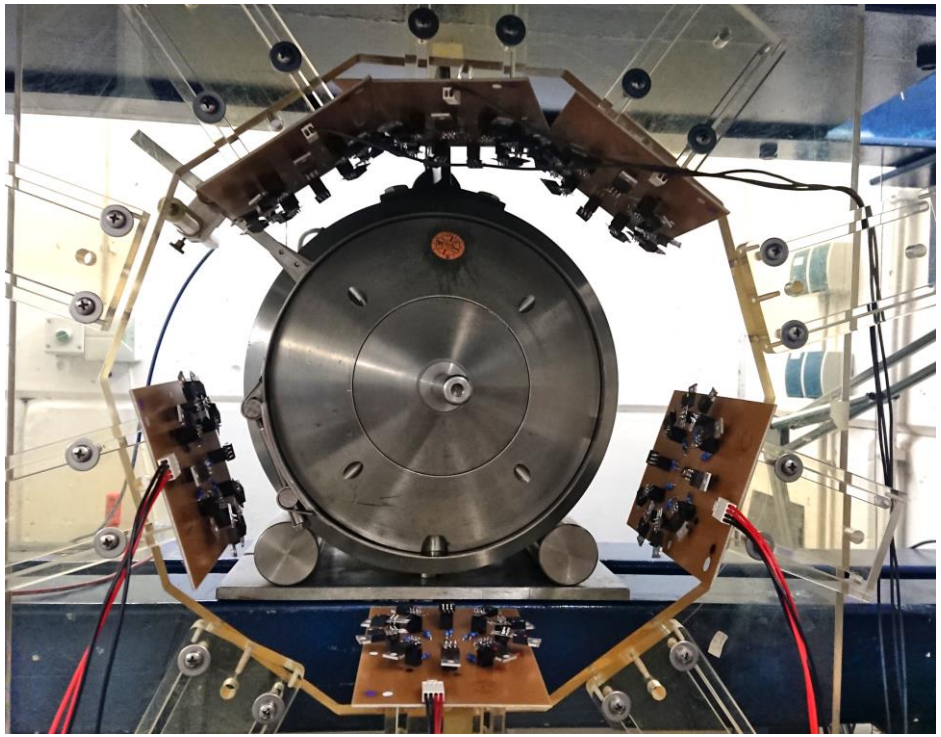
| Color code | Imprint | Translates to date code | … and … |
|---|---|---|---|
| | P021J / 40RV | Year 2020<br>Week 21 | Assembly line „J“<br>Assembly lot code 40RV |
| | P124D / LW43 | Year 2021<br>Week 24 | Assembly line „D“<br>Assembly lot code LW43 |
| | P145J / AH99 | Year 2021<br>Week 45 | Assembly line „J“<br>Assembly lot code AH99 |

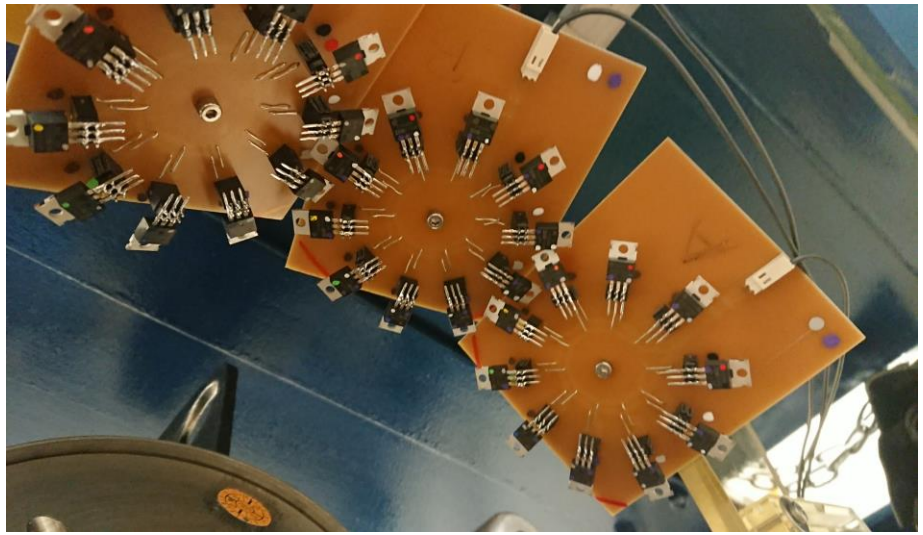
# IRF9540NPBF TID-Test Results

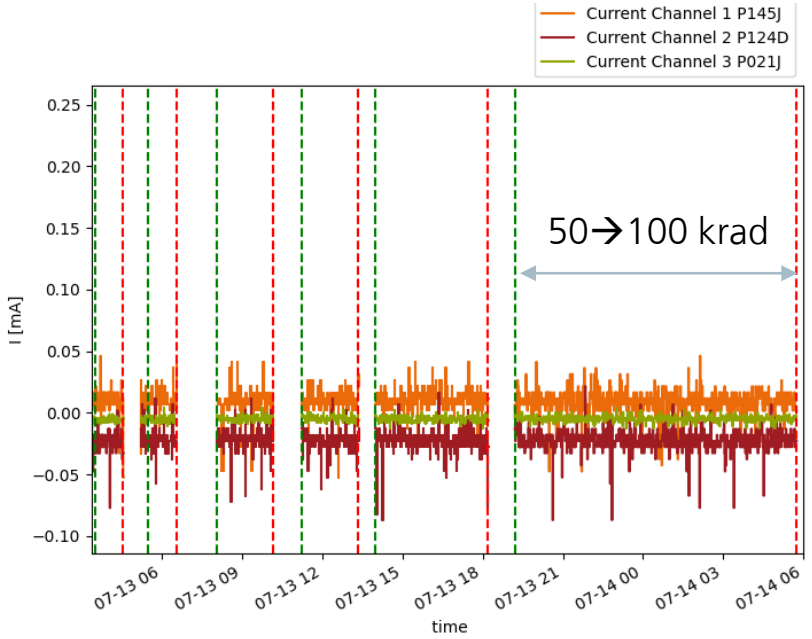
## MOSFET P-Channel 100V

| Bias Configuration: Static |
| --- |
| VDS = -100 V<br>VGS = 0 V<br>10 samples per lot |

| Unbiased |
| --- |
| 10 samples per lot, All Pins grounded |







# IRF9540NPBF TID-Test Results

## MOSFET P-Channel 100V

| Parameter | Symbol |
|---|---|
| Zero Gate Voltage Drain Current | $I_{DSS}$ |
| Drain-Source On-State Resistance 1 | $R_{DS(on)1}$ |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ |
| Reverse Gate-Source Leakage Current | $I_{GSS}$ |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ |

| Equipment | Manufacturer | Model |
|---|---|---|
| Mixed Signal Test Platform | UNITES Systems | UNIMET2020 |
| Front adapter "TA37F" | UNITES Systems | TA37F |

1 DUT failed functionally during 100°C annealing

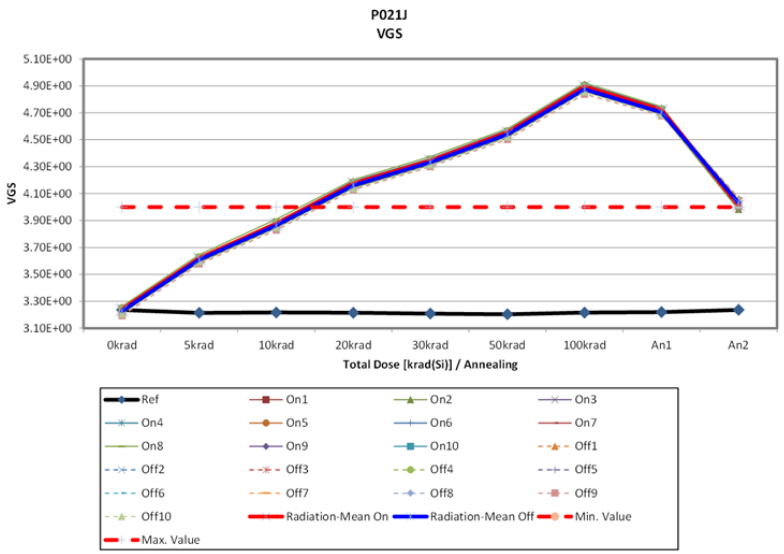
Parametric failures as low as 10 krad in VGS_th

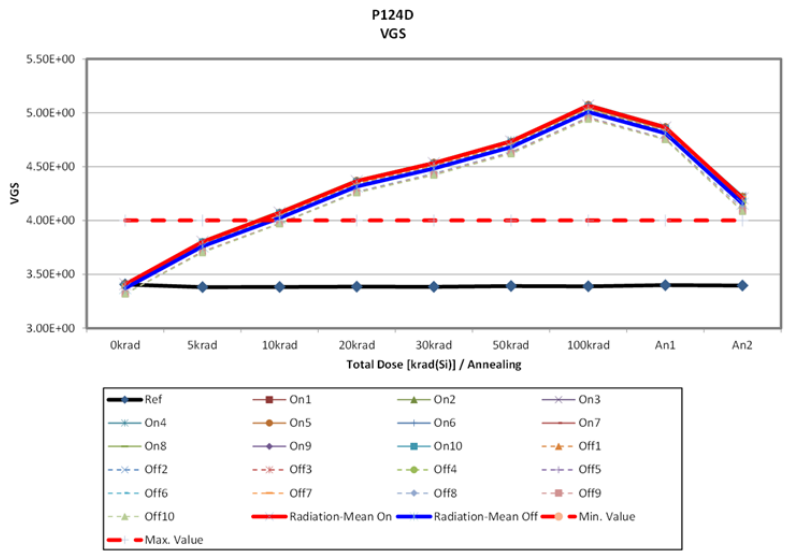
| Parameter | Mode/ Bias | | Co-60 Gammadose [krad(Si)] | | | | | | | Annealing | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 0 | 5 | 10 | 20 | 30 | 50 | 100 | 24 h RT | 168 h 100°C |
| $I_{DS}$ | On | P021J | | | | | | | | | |
| | | P124D | | | | | | | | | |
| | | P145J | | | | | | | | | |
| | Off | P021J | | | | | | | | | |
| | | P124D | | | | | | | | | |
| | | P145J | | | | | | | | | |
| $R_{DS\_on}$ | On | P021J | | | | | | | | | |
| | | P124D | | | | | | | | | |
| | | P145J | | | | | | | | | |
| | Off | P021J | | | | | | | | | |
| | | P124D | | | | | | | | | |
| | | P145J | | | | | | | | | |
| $I_{GS}$ | On | P021J | | | | | | | | | |
| | | P124D | | | | | | | | | |
| | | P145J | | | | | | | | | |
| | Off | P021J | | | | | | | | | |
| | | P124D | | | | | | | | | |
| | | P145J | | | | | | | | | |
| $V_{GS\_th}$ | On | P021J | | | | | | | | | |
| | | P124D | | | | | | | | | |
| | | P145J | | | | | | | | | |
| | Off | P021J | | | | | | | | | |
| | | P124D | | | | | | | | | |
| | | P145J | | | | | | | | | |
| $V_{BR}$ | On | P021J | | | | | | | | | |
| | | P124D | | | | | | | | | |
| | | P145J | | | | | | | | | |
| | Off | P021J | | | | | | | | | |
| | | P124D | | | | | | | | | |
| | | P145J | | | | | | | | | |

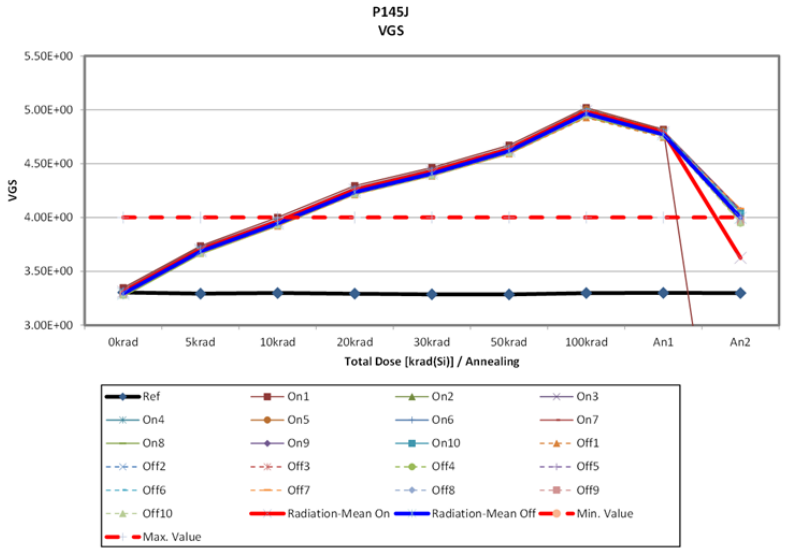
| | |
|---|---|
| | Pass |
| | Check comments in Section 1.1.1. |
| | Parametric Failure |
| | Funktional Failure |

# IRF9540NPBF TID-Test Results

## MOSFET P-Channel 100V



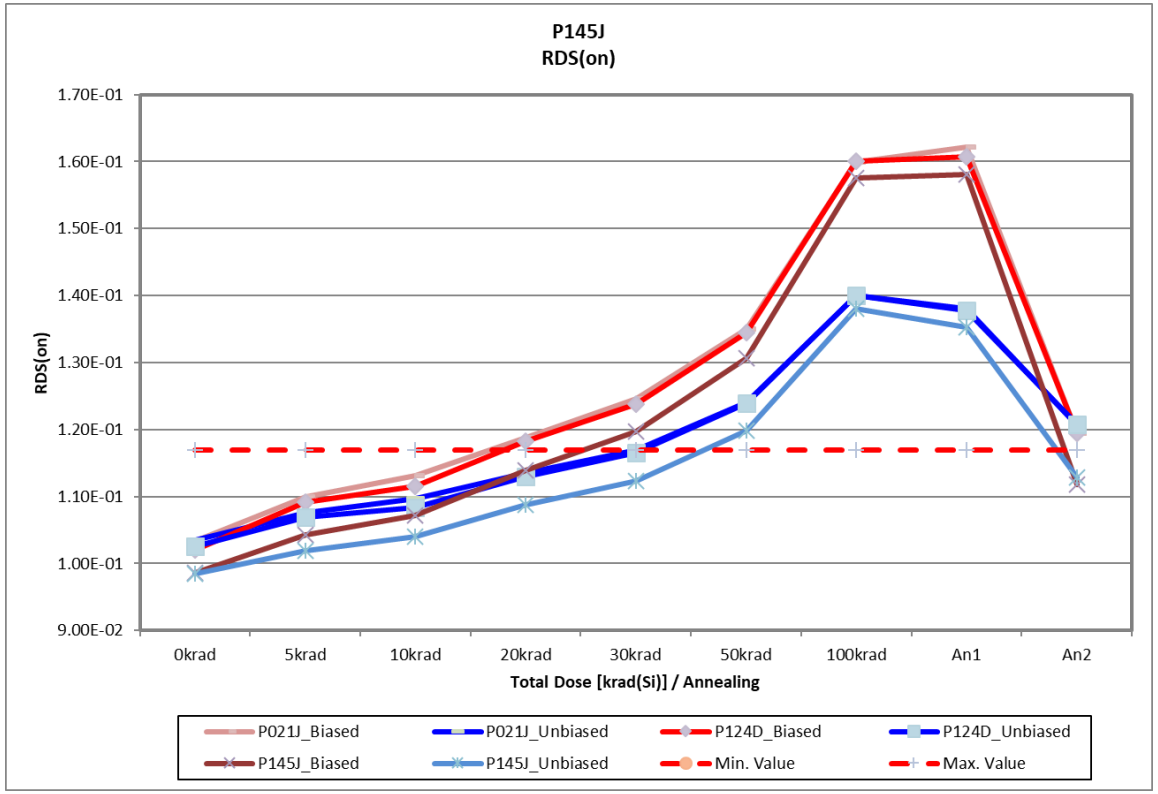




Parametric failures in gate threshold voltage as low as 10 krad

- 1 DUT functional failure after 100°C

# IRF9540NPBF TID-Test Results

## MOSFET P-Channel 100V




P021J and P124D indistinguishable in this plot

P145J has lower RDSon, thus crosses parameter limit at higher TID cannot be linked to assembly line or date code

| Color code | Imprint | Translates to date code | … and … |
|---|---|---|---|
| | P021J / 40RV | Year 2020<br>Week 21 | Assembly line „J“<br>Assembly lot code 40RV |
| | P124D / LW43 | Year 2021<br>Week 24 | Assembly line „D“<br>Assembly lot code LW43 |
| | P145J / AH99 | Year 2021<br>Week 45 | Assembly line „J“<br>Assembly lot code AH99 |

# Summary

## Overview

| Item | Manufacturer | Part Description | |
|---|---|---|---|
| ADUM7440CRQZ-RL7 | Analog Devices | Digital Isolators 4 Channel Digital Isolator, 1kV | Parameter violation > 30 krad(Si), limited to supply currents<br>No loss of functionality at 100 krad |
| INA169QPWRQ1 | Texas Instruments | Current & Power Monitors & Regulators Auto Cat Hi-Side Measurement Mon | Low dose rate sensitive, parameter violation > 20 krad, loss of functionality depending on range of Vsense |
| LMG3410R050RWHT | Texas Instruments | Gate Drivers 600-V 50-m GaN with integrated driver and protection | Loss of functionality > 30 krad(Si), internal GaN does not switch on |
| TSV992IQ2T | STM | Op-Amp | Depending on operation condition: issues with slew rate > 30 krad(Si)<br>Otherwise no parameter violation or functional failure at 100 krad(Si) |
| TSZ182HYDT | STM | Op Amp | Biased: >30 krad loss of functionality, high current state<br>Unbiased: No parameter violation or functional failure at 100 krad(Si) |
| THS4032MDGNREP | Texas Instruments | Op Amp | No parameter violation or functional failure at 100 krad(Si) |
| REF5050MDREP | Texas Instruments | Voltage Reference | Parameter degradation >50 krad espc. Vo / Load Regulation |
| IRF9540NPBF | Infineon | MOSFET P-Channel 100V 23A TO220AB | Parameter degradation of VGSth observed at 10 krad, no functional failure<br>Lot dependence observed esp. Rds_on |

# Thank you for your attention!

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