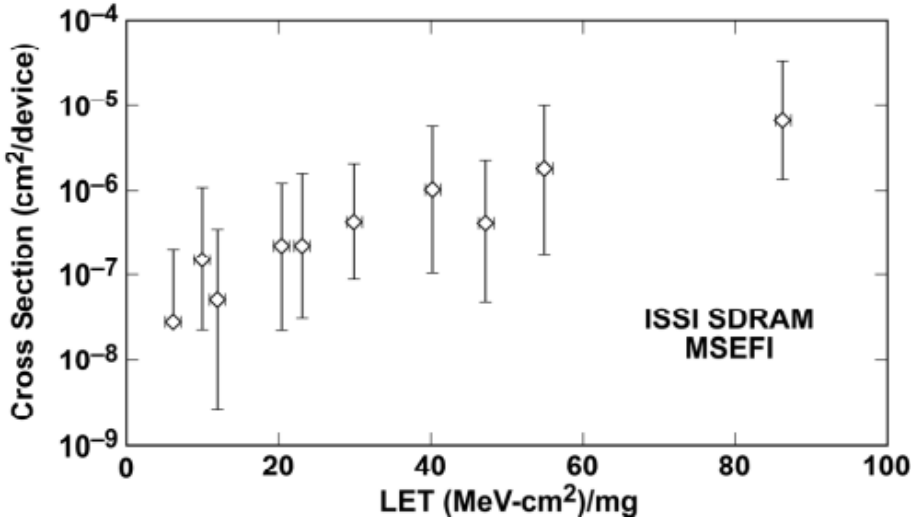
Test Results on SDRAM IS42S86400B-7TLI

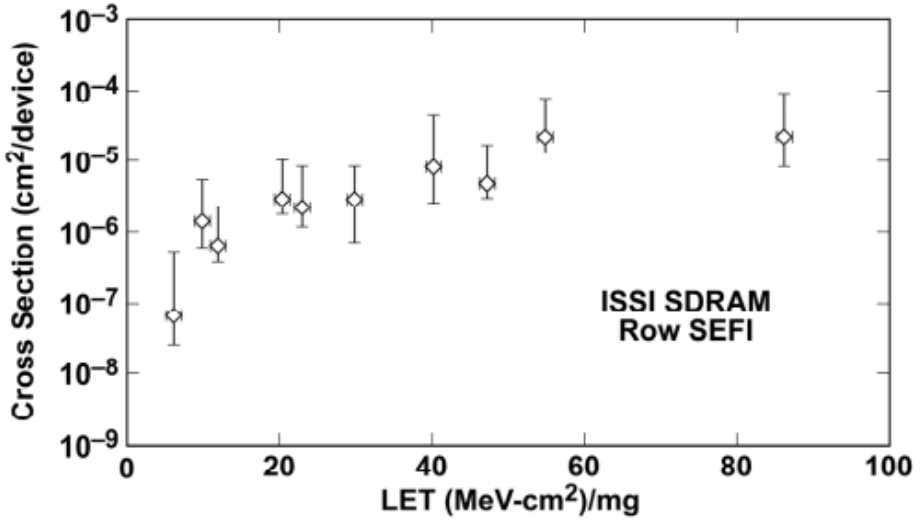
Thierry BONNOIT
Maximilien GLORIEUX
Cesar BOATELLA POLO

29 June 2023

Context and Objectives

- [1][2] reported important SEFI mechanism on ISSI IS42S86400B-7TL SDRAM
  - Million SEFI: Million errors induced by one ionizing particle impact
  - Row/Column SEFI: Set of row/Column with a large number of errors
- Objectives:
  - Reproduce SEFI with LASER attack:
    - Identify sensitive area and event signature
    - Explore mitigation options
  - Measure HI sensitivity
  - Evaluate LEON4 EDAC capability to detect and correct SEFI induced errors





[1]: F. Irom and M. Amrbar, "Heavy Ion Single Event Effects Measurements of 512Mb ISSI SDRAM," *2015 IEEE Radiation Effects Data Workshop (REDW)*, Boston, MA
[2]: G. R. Allen *et al.*, "2015 Compendium of Recent Test Results of Single Event Effects Conducted by the Jet Propulsion Laboratory's Radiation Effects Group," *2015 IEEE Radiation Effects Data Workshop (REDW)*, Boston, MA

LASER Test Approach Overview

- CNES Laser Facility characteristics:
  - Single photon absorption
  - Wavelength: 1064nm
  - Pulse energy: up to 2.5nJ per pulse
  - Pulse picket to reduce pulse frequency
  - Pulse duration: 7.5ps
  - 1X to 50X lens
    - Range: 13x13 mm to 250x250 µm
    - Resolution: 22µm to 0.9µm
- Dynamic test algorithm with flexible options:
    - Operation order
    - Data pattern
    - Address sequence

LASER Experiment Sizing

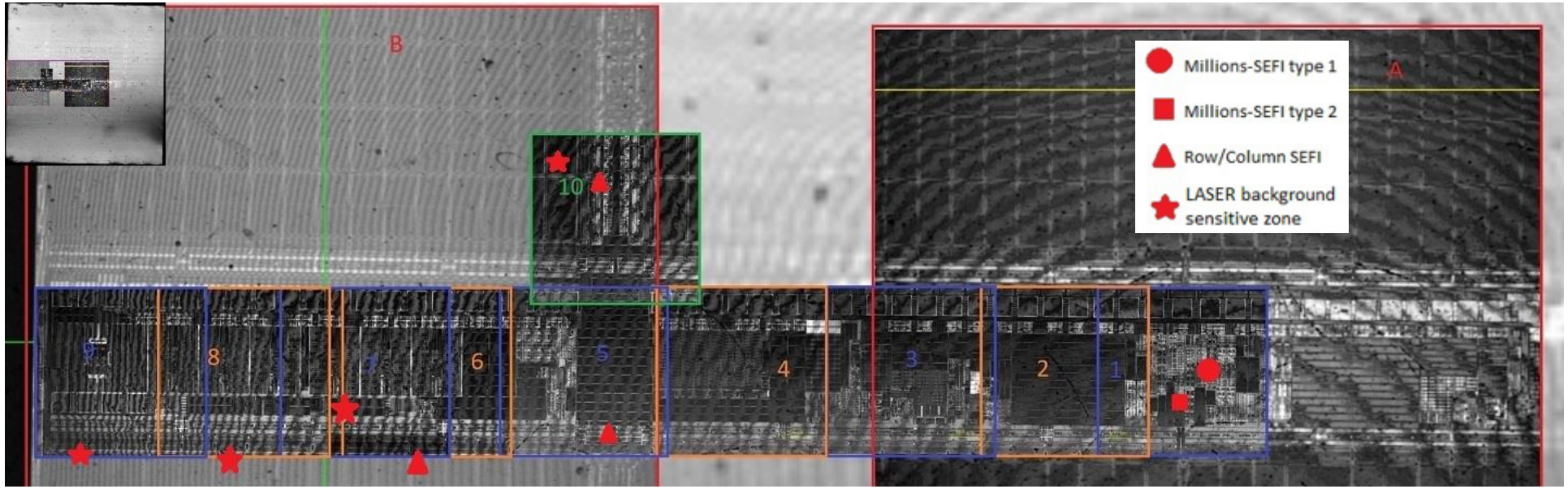
- 50 MHz operation: complete R/W operation duration is 1.4s
- Die area is 9.1x9.1 mm
- Overall scan duration (512x512 pixel per zone):

Lens	Scannable area	Number of zone	Duration
1X	13×13 mm	1	4 days/scan
5X	2.5×2.5 mm	16	68 days/scan
20X	650×650 µm	196	2 years/scan
50X	250×250 µm	1369	16 years/scan

- Possible options:
  - Increase number of laser hit per memory operation
  - Reduce the address range of memory operation
  - Select scanned area

LASER Test Results

- 2 Million SEFI Mechanisms identified
- Row and Column SEFI were observed
- Some regions sensitive to LASER charge accumulation
- Other events (SEU, MBU, MCU, Transients)



Million SEFI Type 1

- Not related to a specific address range and data pattern
- For most of observed events:
  - Similar erroneous data was read at each address (independently of the test pattern)
  - Each address has a specific erroneous data pattern
- Most of the errors are corrected after a write operation but:
  - Few address are still not operating correctly
  - If the refresh is disabled, much more address are not operating correctly
  - The uncorrectable errors seem weak cells / stuck bits
- Power cycle needed to recover
- Possible explanation:
  - Upsets in the memory physical mapping tables that are usually loaded at power on and are not accessible by the user

Million SEFI Type 2

- Upsets in the memory configuration register
  - Modification of the burst sequence
    - New burst configuration is either “000” or “111”
  - Upset of the “Single location address” and “Sequential/Interleaving” bits
  - CAS bit was not upset
- Using a burst of size 1 allows to mask this SEFI
- Re-writing the configuration register correct the SEFI
  - Stored data is not lost and can be read afterward
  - If some write operations were performed, they may not be performed correctly

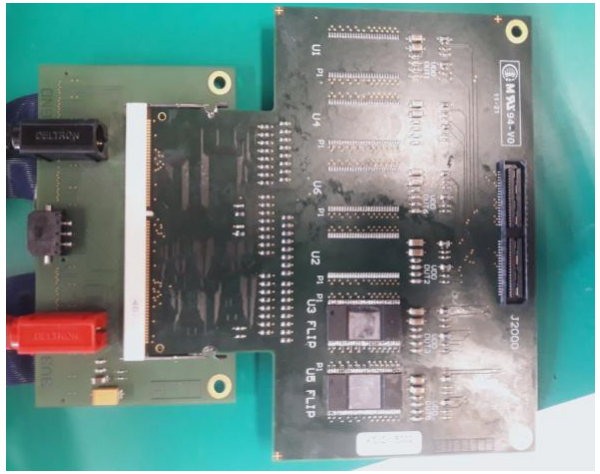
LASER Charge Accumulation

- When LASER energy is increased, some regions are sensitive to the remaining energy not filtered by the pulse picker
  - All address are erroneous
  - Output is tied to 0xFF

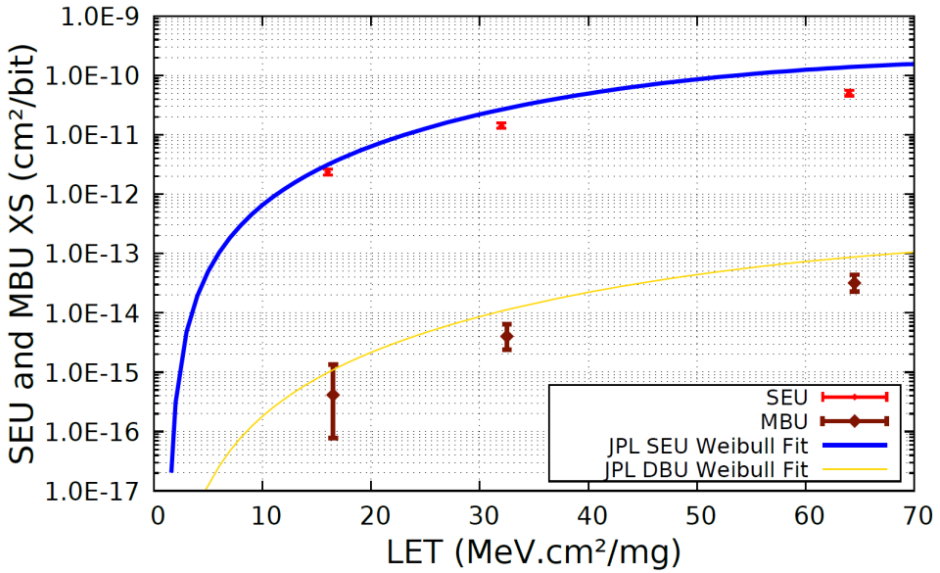
- This is a test artifact!

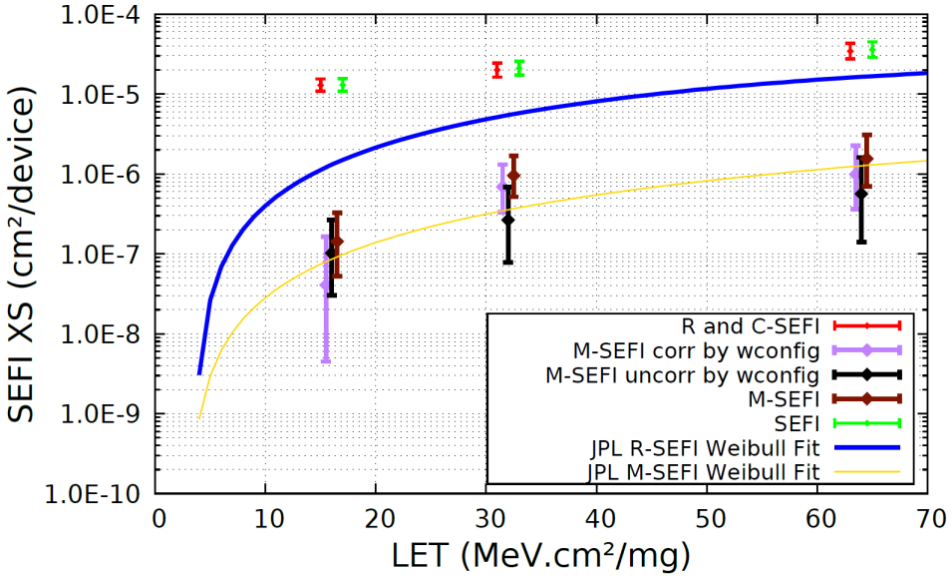
- Observed at several location on the die

Stand-alone HI Tests



- Objective
  - Reproduce SEFI events and measure XS
- SEU – MBU
  - Consistent with JPL results
- SEFIs
  - M-SEFI 1 and 2 observe as in LASER
  - Other SEFI mechanisms identified





System HI Tests with GR740 LEON4

- ISSI as main memory of GR740 LEON4
  - Assess EDAC capability to detect/correct SEFIs
  - 2 devices irradiated simultaneously
- GR740 EDACs are based on 4 bits nibbles
  - 1 nibble error can be corrected
  - Bus data width: 64 or 32 bits (data wrote on 2 consecutive address)
  - 2 interleaving scheme:
    - Mode A: 4 group of 16 bits
    - Mode B: 2 group of 32 bits
  - Test performed in mode A – 32 bits

Table 89. Mode Ax4 interleaving pattern (64-bit data width)

63:60	59:56	55:52	51:48	47:44	43:40	39:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
C	D	A	B	A	B	C	D	B	A	D	C	D	C	B	A
								C_{cb}	D_{cb}	A_{cb}	B_{cb}	C_{cb}	D_{cb}	A_{cb}	B_{cb}

Table 90. Mode Bx2 interleaving pattern (64-bit data width)

63:60	59:56	55:52	51:48	47:44	43:40	39:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
A	B	A	B	A	B	A	B	B	A	B	A	B	A	B	A
												A_{cb}	B_{cb}	A_{cb}	B_{cb}

Table 91. Mode Ax4 interleaving pattern (32-bit data width)

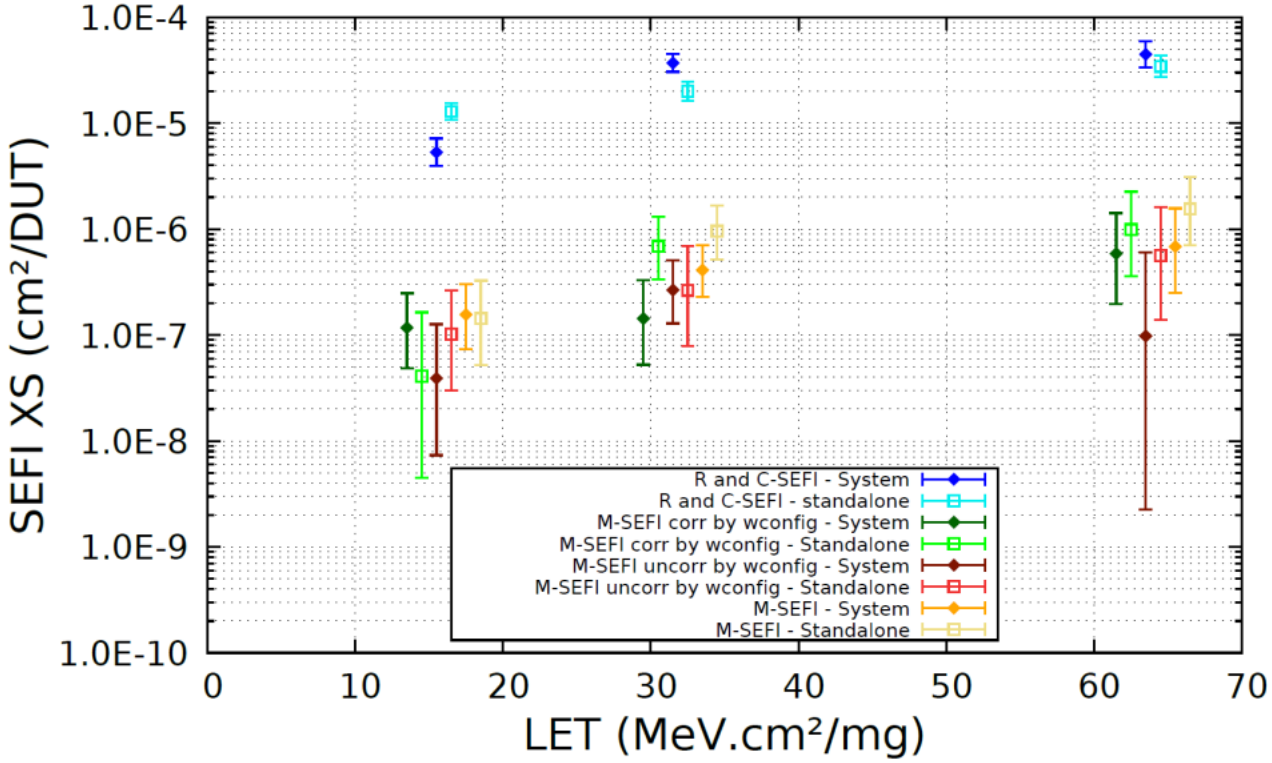
95:80	79:76	75:72	71:68	67:64	63:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
-	C_{cb}	D_{cb}	A_{cb}	B_{cb}	-	C	D	A	B	A	B	C	D
-	B_{cb}	A_{cb}	D_{cb}	C_{cb}	-	B	A	D	C	D	C	B	A

Table 92. Mode Bx2 interleaving pattern (32-bit data width)

95:80	79:76	75:72	71:68	67:64	63:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
-	-	-	A_{cb}	B_{cb}	-	A	B	A	B	A	B	A	B
-	-	-	B_{cb}	A_{cb}	-	B	A	B	A	B	A	B	A

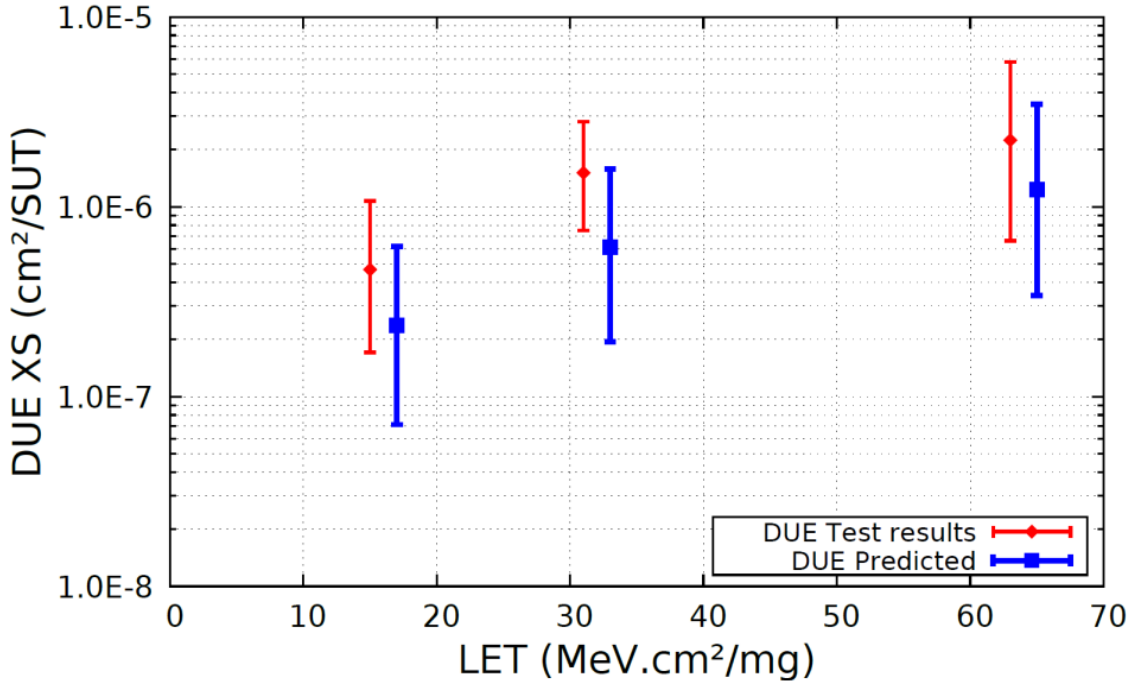
System Test Results

- Test algorithm implemented in software, in the LEON4 CPU
- EDAC error counters used to identify SEFIs
- Similar cross-section as stand-alone test



Detectable Uncorrectable Errors

- GR740 SDRAM are protected with Reed-Solomon ECC
  - EDAC is able to correct data even if one SDRAM device is not functional
  - DUE occurs if two nibbles are erroneous
    - SEFI + SEFI
    - SEFI + SEU
  - DUE are detected by LEON4 interruption when the corresponding address is read
    - DUE XS depends on software execution flow
    - XS is reported for the system



Impact of EDAC Configuration

- The impact of EDAC mode was assessed analytically
  - EDAC can correct one nibble error per group
  - In mode A 64/32 bit or B 64 bits:
    - a M-SEFI impact one nibble / group
    - $P(DUE) = P(Ev_1 \cap Ev_2)$
    - Ev_1/Ev_2 is M-SEFI, R/C-SEFI or SEU
    - $P(A\ -64) = 2 \times P(A\ -32)$ but system memory is 2 times larger in 64 bit mode
  - In mode B 32 bits:
    - SEFI impact two nibble / group
    - Any SEFI will lead to DUE
    - $P(DUE) = N_{DUT} \times P(SEFI)$

Table 89. Mode Ax4 interleaving pattern (64-bit data width)

63:60	59:56	55:52	51:48	47:44	43:40	39:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
C	D	A	B	A	B	C	D	B	A	D	C	D	C	B	A
								127:120	119:112	111:104	103:96	95:88	87:80	79:72	71:64
								C_{cb}	D_{cb}	A_{cb}	B_{cb}	C_{cb}	D_{cb}	A_{cb}	B_{cb}

Table 90. Mode Bx2 interleaving pattern (64-bit data width)

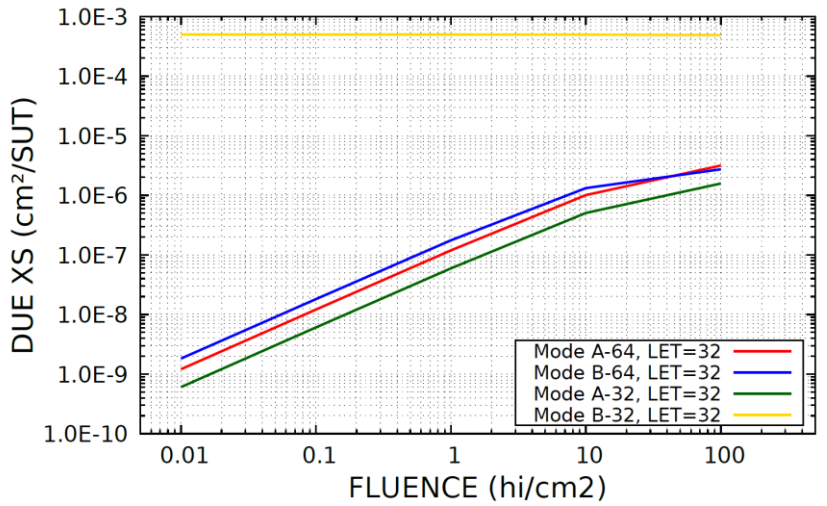
63:60	59:56	55:52	51:48	47:44	43:40	39:36	35:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
A	B	A	B	A	B	A	B	B	A	B	A	B	A	B	A
												95:88	87:80	79:72	71:64
												A_{cb}	B_{cb}	A_{cb}	B_{cb}

Table 91. Mode Ax4 interleaving pattern (32-bit data width)

95:80	79:76	75:72	71:68	67:64	63:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
-	C_{cb}	D_{cb}	A_{cb}	B_{cb}	-	C	D	A	B	A	B	C	D
-	B_{cb}	A_{cb}	D_{cb}	C_{cb}	-	B	A	D	C	D	C	B	A

Table 92. Mode Bx2 interleaving pattern (32-bit data width)

95:80	79:76	75:72	71:68	67:64	63:32	31:28	27:24	23:20	19:16	15:12	11:8	7:4	3:0
-	-	-	A_{cb}	B_{cb}	-	A	B	A	B	A	B	A	B
-	-	-	B_{cb}	A_{cb}	-	B	A	B	A	B	A	B	A



GEO Error Rate Estimations

- GEO DUE probability was estimated considering a memory restore cycle each hour
  - Memory restore cycle is write config register + memory scrubbing
- 15 year GEO mission, with 3.7 mm of Al spherical shielding
- As only 3 LET are available, simple error calculation is performed
- In mode B - 32 bit, it corresponds to the probability to get a SEFI during the mission

ECC Mode	P(DUE) in 1h	P(DUE) in 15y
A – 64 bit	2.16E-9	0.028%
B – 64 bit	3.23E-9	0.042%
A – 32 bit	1.08E-9	0.014%
B – 32 bit	1.74E-4	100%

Conclusions

- Several SEFI mechanism were identified and observed with LASER
  - Some cannot be corrected with write config register (power cycle needed)
- LASER experiment is a good preparation for complex HI test but
  - Experiment sizing can be difficult
  - LASER experiment is not exhaustive
- LASER results helpful to prepare post-processing scripts
- Stand-alone HI test provided similar results as JPL
- System test shown that GR740 EDACs can correct SEFIs
  - DUE still possible in case of SEFI+SEU or SEFI+SEFI on several memory components
  - GEO mission DUE very unlikely in mode A or B-64 bits
  - EDACs mode B-32 bits not well hardened against SEFI/permanent faults