CORHA Project: Radiation screening of COTS components and verification of COTS RHA approach - Part 2

S. Gerardin[1], M. Bagatin[1], A. Paccagnella[1],
P. Beck[2], C. Tscherne[2], M. Wind[2], M. Poizat[3]

[1] DEI - University of Padova, Italy
[2] Seibersdorf Labor GmbH, Austria
[3] ESA - ESTEC, The Netherlands

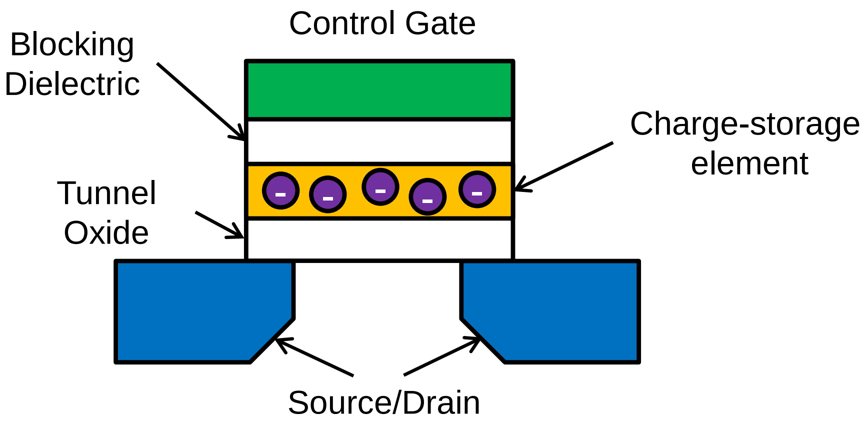
Outline

- Non-volatile Memories for Small Satellites
- Experimental Results
  - Total Ionizing Dose
    - Lot-to-lot Variability Study
  - Single Event Effects:
    - Heavy Ions
    - Protons
- Radiation Hardness Assurance for COTS used on low-cost missions
  - Proposed flow and guidelines

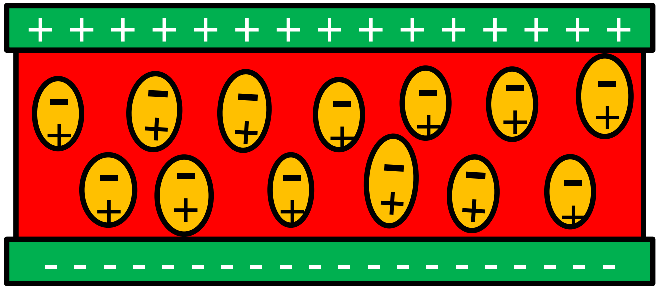
Devices

- Microcontrollers and FPGAs used in small satellites require low-footprint non-volatile memories (NVM) for configuration, code, and data storage purposes
- SPI and NOR interfaces

	MB85RS256TY	CY15B102QN	CY14V101PS	MT28EW128ABA
Part Type	SPI **Ferroelectric** RAM	SPI **Ferroelectric** RAM	SPI Non-volatile SRAM (**SONOS**)	Parallel NOR Flash Memory (**Floating Gate**)
Manufacturer	Fujitsu Semiconductor	Cypress	Cypress	Micron Technology
Size	256 kbit	2 Mbit	1 Mbit	128 Mbit
Operating Voltage	1.8 to 3.6 V	1.8 to 3.6 V	Core 2.7 to 3.6 V; I/O 1.71 to 2.0 V	Core 2.7 to 3.6 V; I/O 1.65 to 3.6 V
Operating Temperature	-40°C to 125°C	-40°C to 125°C	-40°C to 85°C	-40°C to 85°C
Package	SOP8	SOIC8	SOIC16	TSOP56



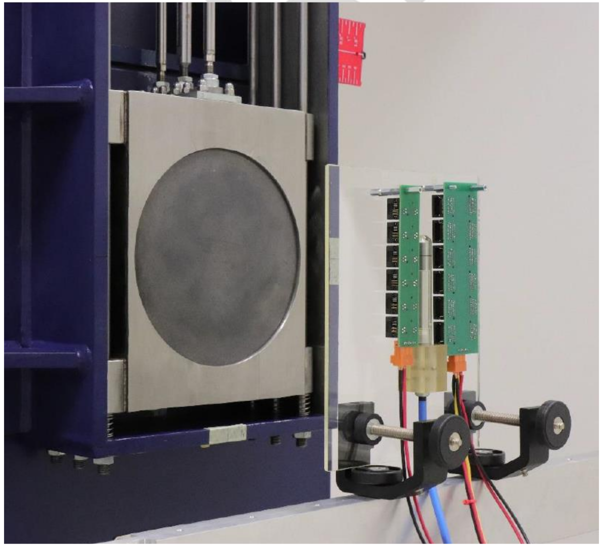
- Storage concept: Inject or remove **charge** between the control gate and the channel
- Charge storage element: **floating polysilicon gate (FG)**, **charge-trap layer** (e.g. Semiconductor Oxide Nitride Oxide Semiconductor - SONOS)
- Radiation can remove stored charge



- Storage concept: **Ferroelectric materials** are able to retain the **polarization** of the dipoles which occurs when an electric field is applied after the field has been removed
- Cells are not very sensitive to **radiation**, peripheral circuitry can be, but voltages are low

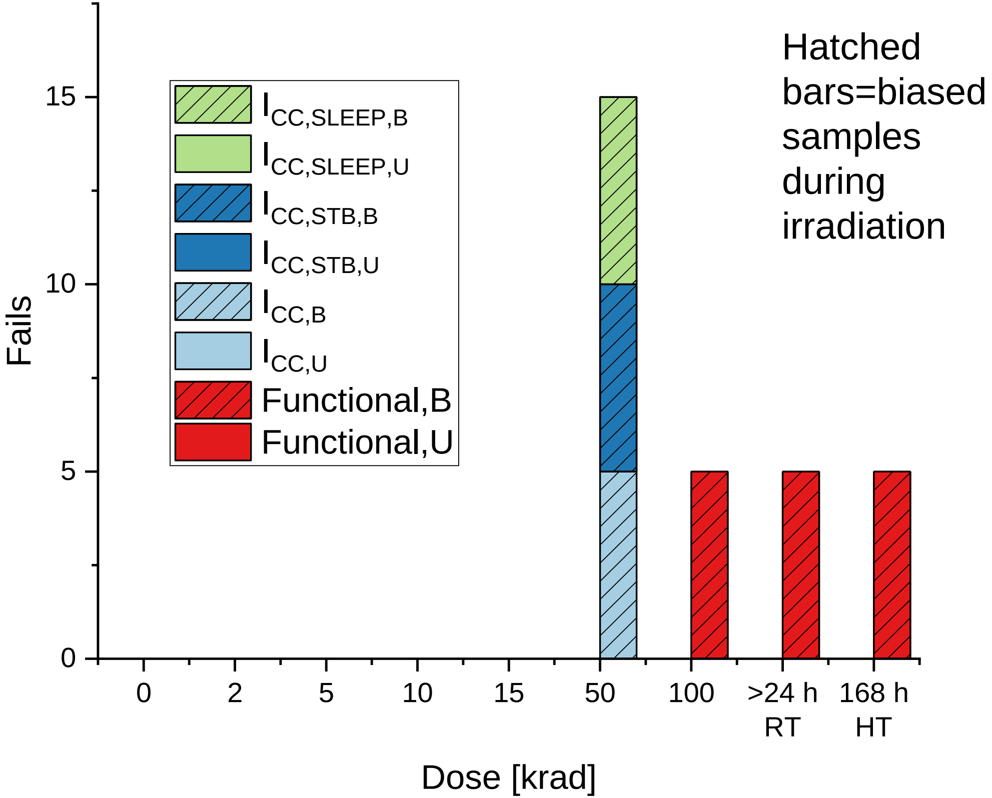
TID Facility and Experiments

- Co^{60} source at Seibersdorf Laboratories
- Dose rate: 2.4 krad(Si)/hour
- Steps: 2, 5, 10, 15, 50, 100 krad(Si)
- 24+ hours annealing at room temperature + 1 week at 100°C
- Devices
  - 5 samples under static bias (memories were idle, but selected, ready to operate)
  - 5 unbiased samples (grounded pins)
  - References for each experimental conditions
- Parametric degradation measured and failure modes identified up to 100 krad(Si)
- Three different lots were tested for CY15, one for the others

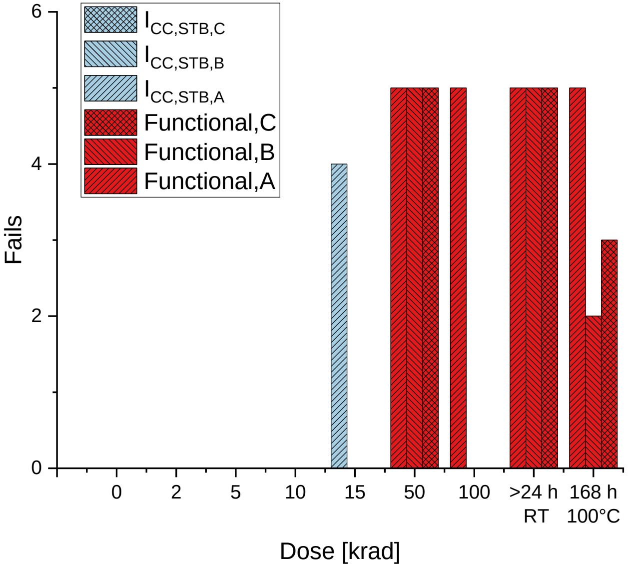


Ferroelectric memory: MB85RS256TY

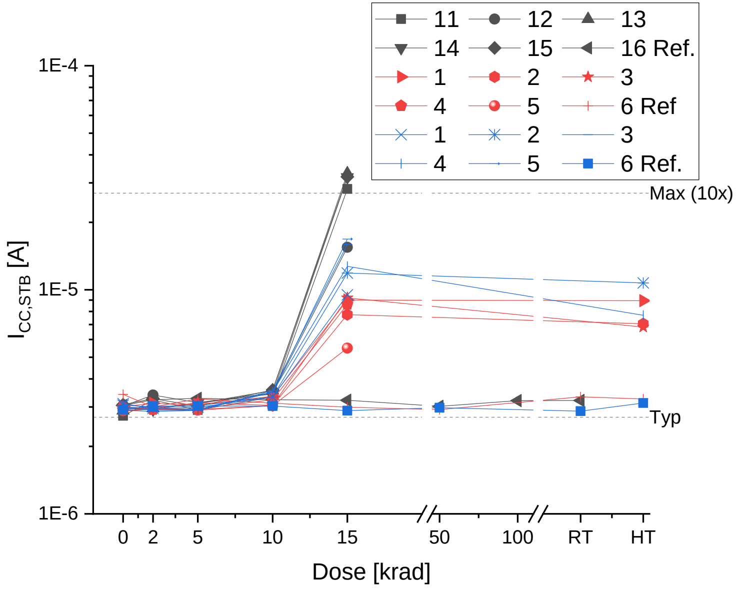
- No issues with cells (FRAM)
- Minor parametric (power consumption) between 15 and 50 krad(Si) in all the biased samples
- Functional failures between 50 and 100 krad(Si) in all the biased samples



Ferroelectric memory: CY15B102QN

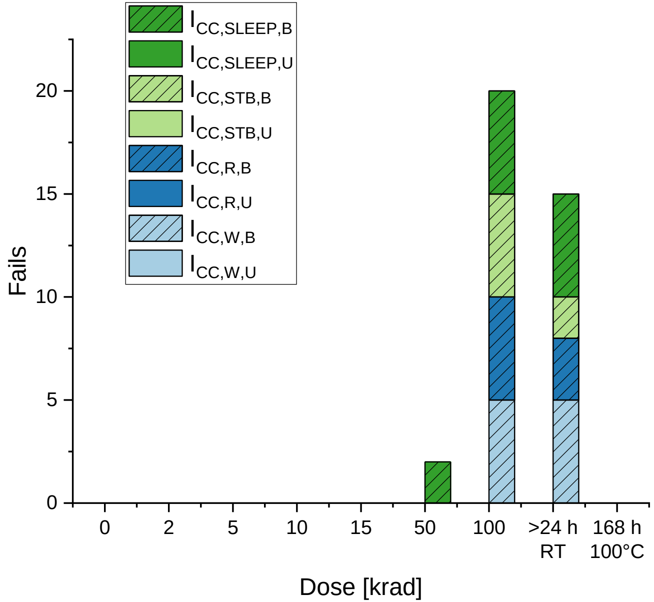


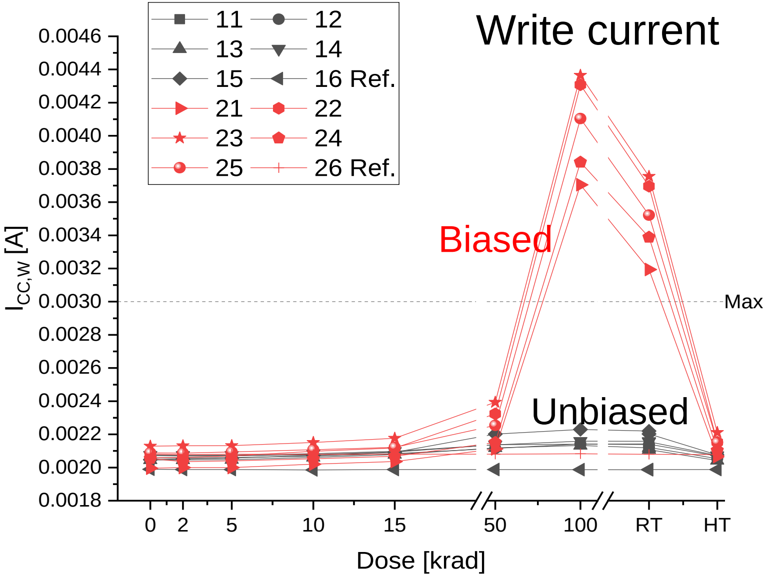
N.B. Lot A (black) irradiated to 100 krad(Si), lot B and lot C (red and blue) to 50 krad(Si)



- No issues with cells (FRAM)
- Minor parametric (standby power) between 15 and 50 krad(Si). Lot-to-lot Variability.
- Functional failures between 50 and 100 krad(Si) in biased samples in all three lots
- Recovery of some samples after 100°C annealing.
- All other parameters do not show significant variations across lots

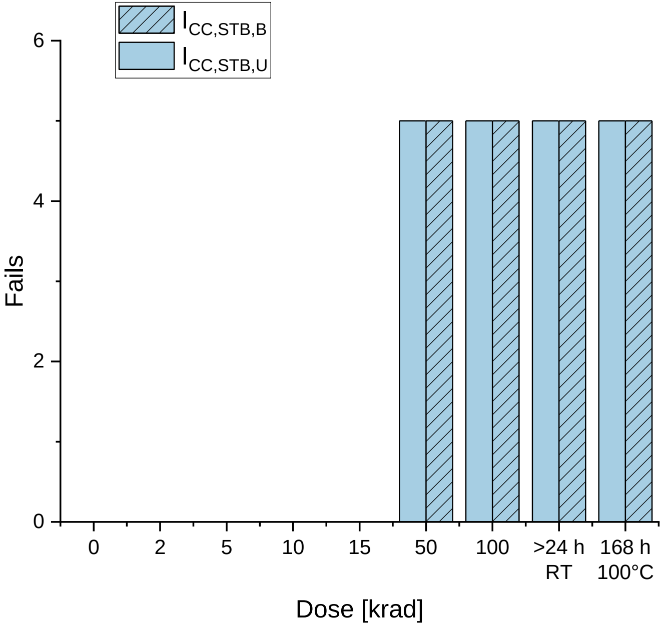
Non-volatile SRAM memory: CY14V101PS

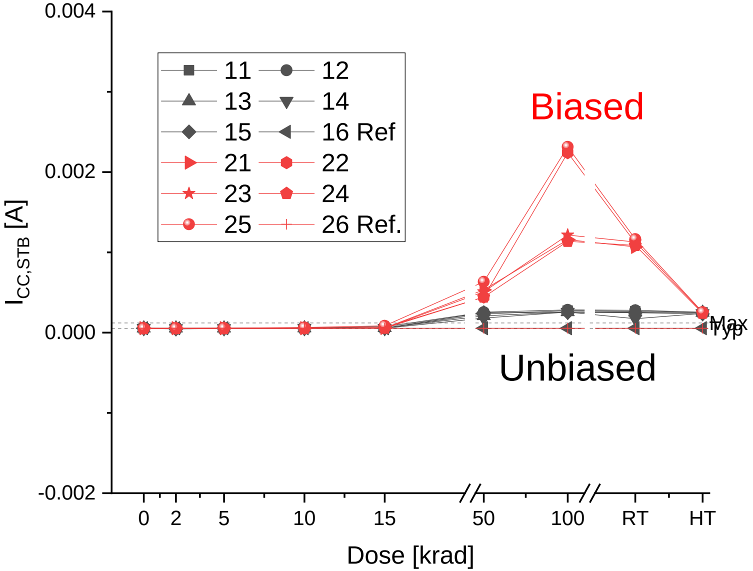




- No issues with functionality of volatile (SRAM) or non-volatile (SONOS) storage
- Tolerable power consumption degradation in the peripheral circuitry above 50 krad(Si)
- Some sample-to-sample variability
- Current marginally increases also in unbiased devices, but stays well below max spec

NOR Flash memory: MT28EW128ABA



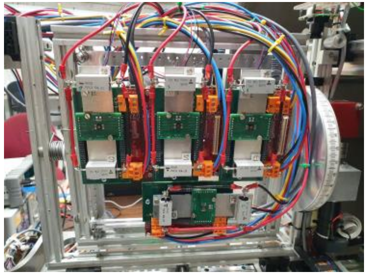


- No issues with functionality of cells (Floating Gate)
- Increase in standby current, both in biased and unbiased components
- Some sample-to-sample variability
- Current increases also in unbiased devices over Max limit, but < than in biased devices

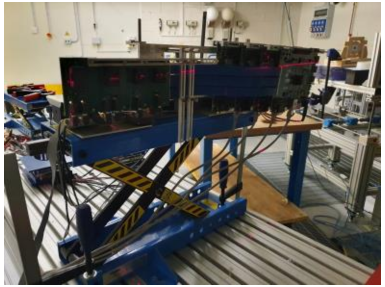
Test setup: custom motherboard + daughterboard with a power analyzer

- SEU: powered off for non-volatile cells, standby for volatile
- SEFI: a loop of (erase)/program/read (SEFI full) or read (SEFI read)
- SEL: biased and heated in idle ready-to-operate conditions

- All memories were tested with heavy ions at HIF, Louvain-la-Neuve



- The two most sensitive devices have been tested with protons: CY14 nvSRAM, CY15 FeRAM at TIFPA Trento

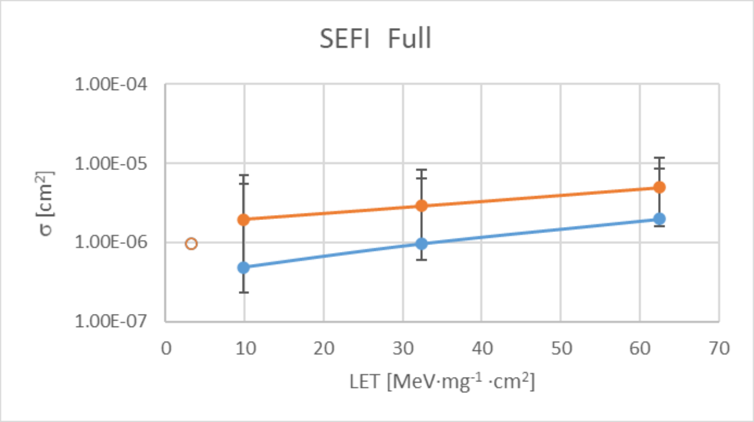


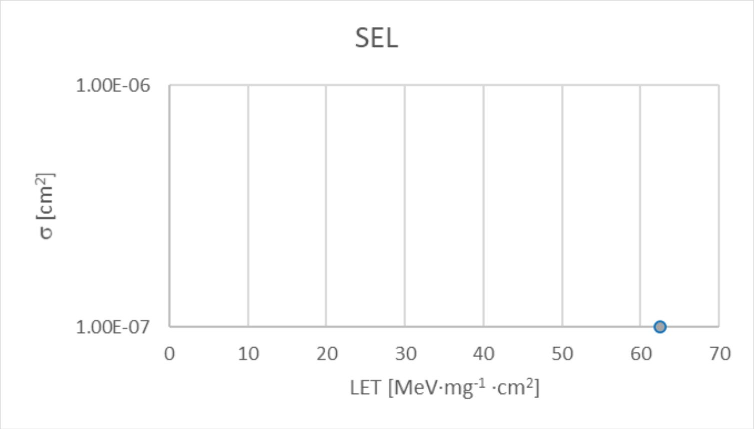
Heavy-ion	Range [µm Si]	LET [MeV/(mg/cm²)]
Ne	3.3	202
Ar	9.9	114
Kr	32.4	94.2
Xe	73.1	62.5

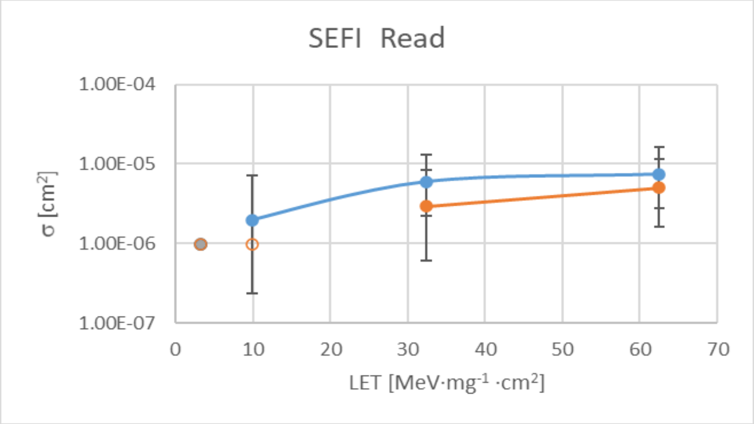
p energy [MeV]	Range [mm Si]	LET [MeV/(mg/cm²)]
70	22	$8.016\cdot10^{-3}$
119	56	$5.370\cdot10^{-3}$
169	104	$4.220\cdot10^{-3}$
202	141	$3.617\cdot10^{-3}$

MB85: SEE with Heavy Ions

- FRAM technology
- Cells are immune up to > 60 MeV·mg^{-1}·cm^2
- SEFI σ considerably lower than in the Cypress devices
- No SEL @ 85°C

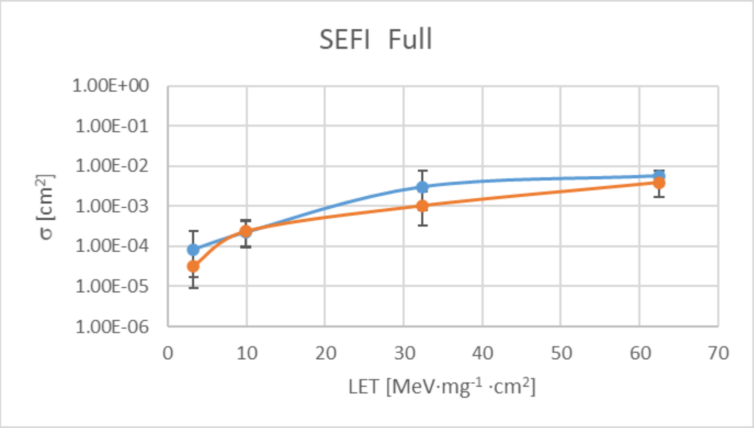


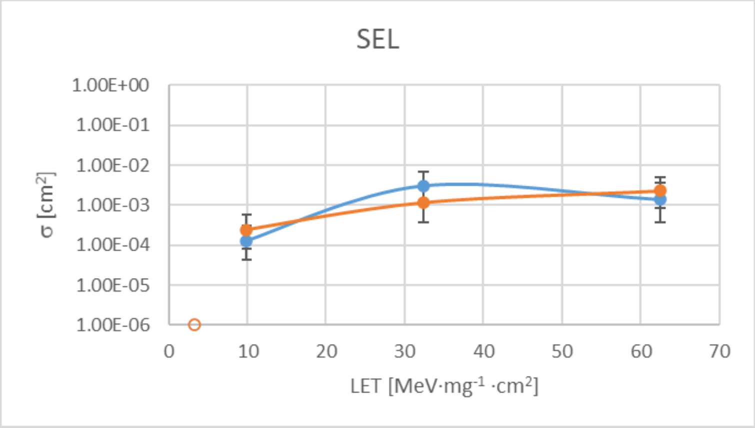


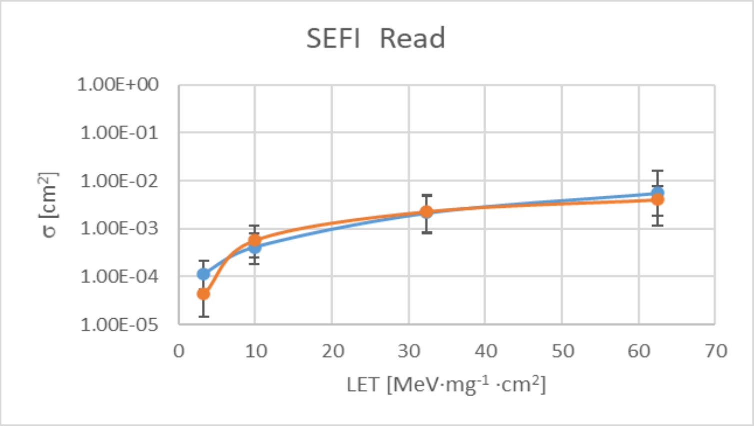


CY15: SEE with Heavy Ions and Protons

- FRAM technology
- Cells are immune up to > 60 MeV·mg^{-1}·cm^2
- Cross sections for SEFIs and SEL (at room temperature) are very close
- Hard to tell if there is a spike in the current, when the device is operating and dynamic current dominates, but it is likely
- Events (SEFI and SEL, no SEU) with protons qualitatively consistent with heavy-ion sensitivity

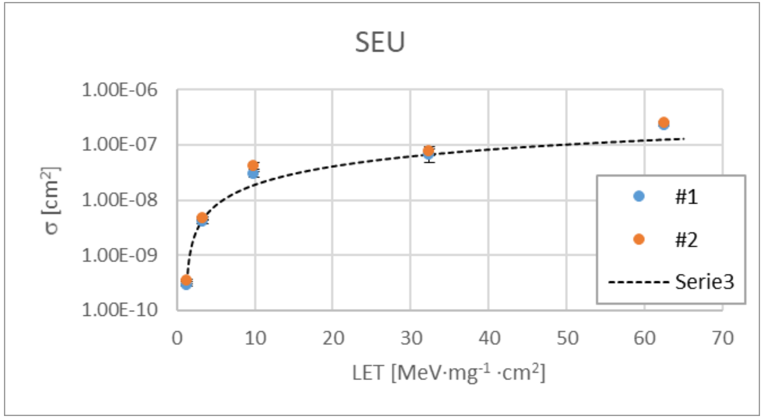


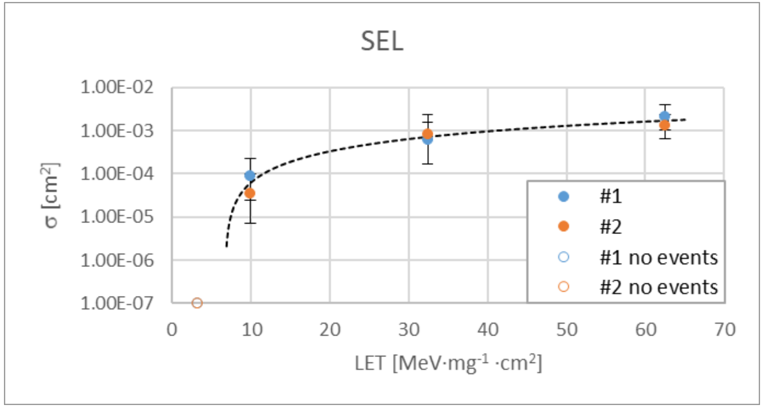


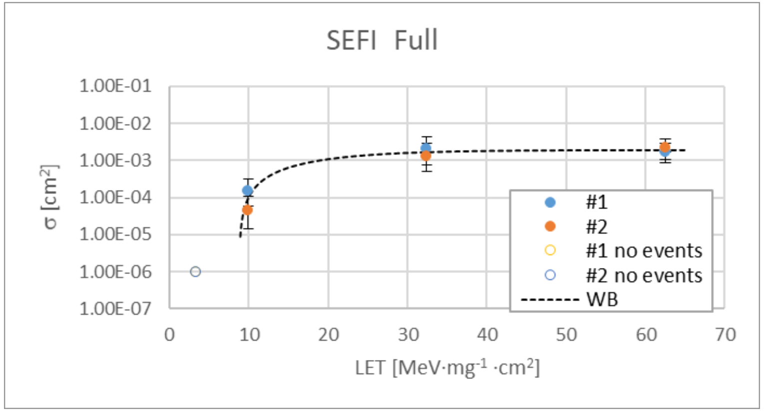


CY14: SEE with Heavy Ions and Protons

- nvSRAM (SRAM+SONOS)
- NV cells are immune up to 62.5 $MeV \cdot mg^{-1} \cdot cm^2$ (higher LET will be tested)
- SRAM cells are sensitive
- SEL (RT), SEFI σ are similar (again, hard to tell if there is a spike in SEFI events, but it is likely)
- Events (SEU, SEFI and SEL) with protons consistent with heavy-ion sensitivity (large error bars and significant dose for SEFIs)

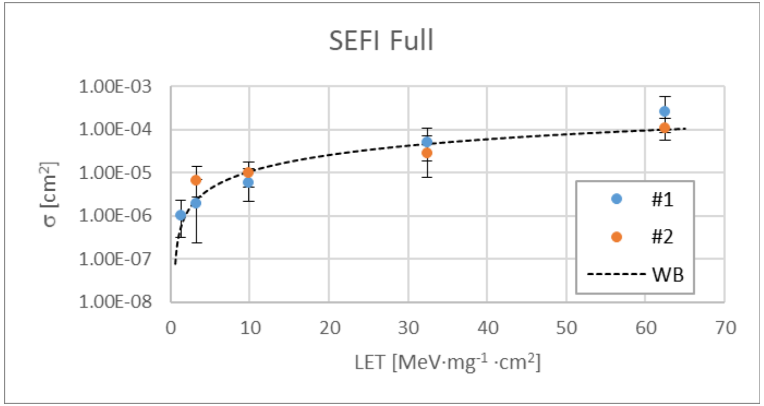


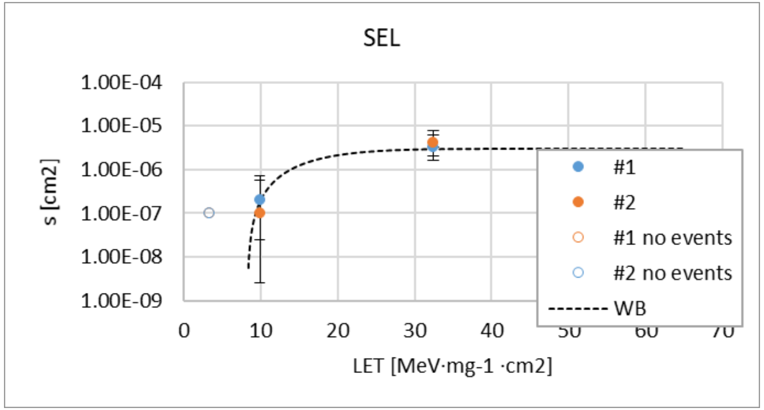


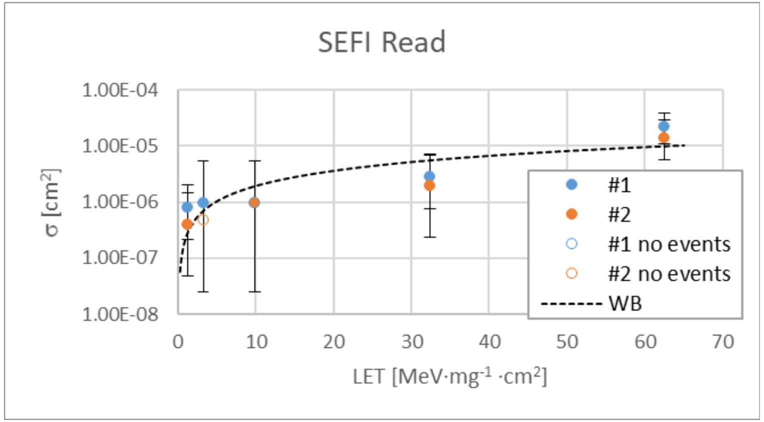


MT28: SEE with Heavy Ions

- NOR Flash
- Cells sensitive at 62.50 MeV·mg-1·cm^2, $\sigma < 10^{-10}$ cm^2
- Destructive events with Xe (inability to program and erase). Likely charge pump failure, not related to TID







NVM Summary

- Total Ionizing Dose
  - All memory cells, regardless of the storage technology, behave well
  - Increase in the supply current in various conditions and to various extents is the most common issue at doses below 50 krad(Si)
  - Functional failures can appear above 15 krad(Si)
  - In general, the samples show a consistent behavior even between lots in the case of the CY15
  - Small differences are visible in stand-by current for the biased components
- Single Event Effects
  - All tested NV cells are pretty hard with respect to SEU
    - data loss only with Micron NOR Flash with Heavy Ions (HI) at an LET of 62.5 (small σ)
  - CY14 nvSRAM has expected SEU sensitivity in the SRAM cells (both HI and p)
  - Significant and consistent SEL/SEFI σ in Cypress devices (both HI and p)
  - Destructive events in the Micron NOR Flash with HI at an LET of 62.5 $MeV \cdot mg^{-1} \cdot cm^2$

- Non-volatile Memories for Small Satellites
- Experimental Results
  - Total Ionizing Dose
    - Lot-to-lot Variability Study
  - Single Event Effects:
    - Heavy Ions
    - Protons
- Radiation Hardness Assurance for COTS used on low-cost missions
  - Proposed flow and guidelines

Introduction

- The goal of this work package was to define a **radiation hardness assurance (RHA)** methodology compatible with the requirements of **small missions**
  - Use of COTS components
  - Restricted budget
- We incorporated ideas from the literature and lessons learned during the project and proposed a **simplified flow**
- Use of **available information** to the maximum extent
- Only some highlights will be presented

Proposed Flow

1. Radiation Environment
2. Criticality Analysis
3. Evaluation of radiation performance of selected parts
   a) Use of Existing Radiation Data
   b) Use of Information on Manufacturing Technology
   c) Radiation Testing
      i. Board-level Testing
4. Part Suitability Assessment

2. Criticality Analysis

- Mission-ending failures should be addressed first
- The following radiation effects should be always considered
  - **Destructive SEE**
    - Single Event Latchup, Single Event Gate Rupture or Single Event Burnout
  - Less likely to induce mission-ending critical failures, but still important to consider are TID and DD-induced failures
- Considerations should also be given to the effects causing **single event functional interrupts (SEFIs)**
  - no physical damage to the devices, but loss of information which may seriously put a mission at risk
- **SEUs can usually be mitigated** (and should)

3.b Use of Information on Manufacturing Technology

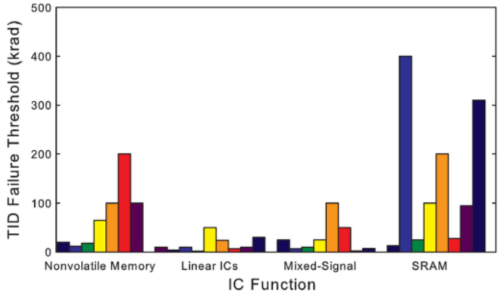
- When no test data are available and testing is not a possibility, an **analysis of the manufacturing technology** should be performed
- Concerning **Total Ionizing Dose**
  - **Scaling** (gate oxide thickness reduction, replacement of LOCOS with STI), has led to an **increase in the tolerance of devices with small feature size operating at low voltage**
  - In general, **the larger the supply voltage, the more likely the device is to suffer from total ionizing dose effects**
    - Digital devices are more aggressively scaled than their analog counterparts, but variability is large especially among COTS
    - Devices with a low supply voltage may have internal circuitry working at higher voltages (e.g. non-volatile devices)

Technology and TID Sensitivity

- Results obtained by the CORHA project
  - **Functional failures** tend to occur at relatively **high doses** in all tested components,
  - **Parametric failures** may occur at doses as low as 2 krad in some analog components
- Failure doses as low as 1 krad can be found; below 1 krad, the probability of failure due to total dose is very very small
- Moderate parametric failures can be tolerated, to be addressed on a case-by-case basis
- Based on results collected during the project and the scientific literature, **guidelines relating technologies to expected TID tolerance** have been proposed

Category	Device	Parametric Failure Level (krad)		Functional Failure Level (krad)		TID Pass Level (krad)		Comment
		biased	unbiased	biased	unbiased	biased	unbiased	
NVM	MT28EW128ABA	50	50			15	15	Standby current increases over spec.
NVM	CY14V101PS	50	100			15	50	Supply current increases overs spec.
NVM	MB85RS256TY	50		**100**		15	100	
NVM	CY15B102QN	15		**50**		10	100	Standby current increases over spec, then functional failure.
µC	STM32F103RGT6			54.1	100.1	25.1	54.1	
µC	STM32L152RET6			100.1	168h, 100°C	25.1	24h, RT	
OpAmp	LT1499HS#PBF-ND	10.0	10.0	> 100	> 100	2.0	2.0	
OpAmp	LTC6240HVCS#PBF-ND	10.3	10.3	> 100	> 100	2.0	2.0	
OpAmp	MAX44248ASA+T	> 100	> 100	> 100	> 100	100	100	
Analog Mux	CD74HC4051M96	11.0	54.0	> 100	> 100	2.0	25.0	Truth Table Test fails after 24h, RT anneal and recovers after 168h, elevated temperature annealing
Analog Mux	ADG5408TCPZ-EP	2.0	11.0	> 100	> 100	0.0	2.0	Truth Table Test fails at 2 krad for the biased and at 100 krad for the unbiased device
ADC	ADC128S102CIMTX	11.0	11.0	> 100	> 100	2.0	2.0	

Summary of CORHA TID Results



From Dodd et al. IEEE TNS 2008

Technology and SEE Sensitivity

- The evolution of SEE with scaling is much less straightforward
  - Latchup increases with T and V (strong dependence on doping levels and geometry)
  - LET_{th} for SEU decreases and MBU increases
  - SEFIs become more and more complex and difficult to diagnose
- CORHA results
  - Wide variety of observed behaviors
  - SEL is a common threat
  - SEUs are common in volatile storage
- Based on the results collected during the project and the scientific literature, **guidelines relating SEE to technologies** have been proposed

Category	Device	SEL	Comments
Non-volatile Memory	MT28EW128ABA	Yes	Small probability
Non-volatile SRAM	CY14V101PS	Yes	@ room temperature and also with protons
Non-volatile Memory	MB85RS256TY	No	
Non-volatile Memory	CY15B102QN	Yes	@ room temperature and also with protons
Microcontroller	STM32F103RGT6	No	
Microcontroller	STM32L152RET6	Yes	Intense latching @ Room temperature and also with protons
OpAmp	LT1499HS#PBF-ND	No	
OpAmp	LTC6240HVCS#PBF-ND	No	
Analog Mux	CD74HC4051M96	No	
Analog Mux	ADG5408TCPZ-EP	No	A single latch up was observed @ room temperature
ADC	ADC128S102CIMTX	Yes	

Category	Device	SEU
Non-volatile Memory	MT28EW128ABA	Sensitive only at high LET (large feature size)
Non-volatile SRAM	CY14V101PS	Non-volatile storage is immune, volatile one is sensitive
Non-volatile Memory	MB85RS256TY	Immune
Non-volatile Memory	CY15B102QN	Immune

Summary of CORHA SEE Results

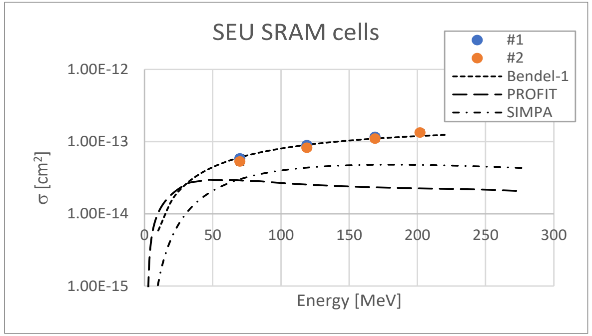
3.c TID Testing Guidelines

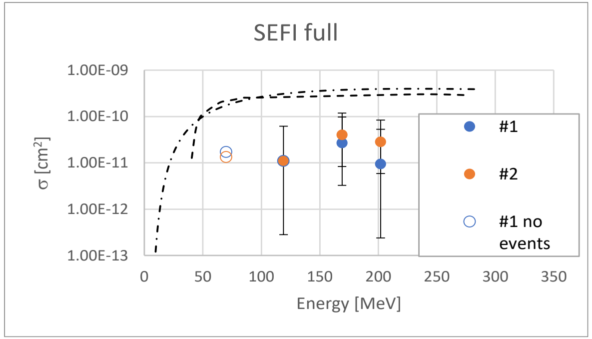
Expected Dose	Recommendation
$< 1krad_{(Si)}$	No testing
$1 – 5\ krad_{(Si)}$	Decision for testing at component, board or equipment level shall be made by the mission engineers.
$> 5krad_{(Si)}$	Perform testing at component, board or equipment level.

- These recommendations are valid for low-cost missions only
  - There are always risks associated with no testing

3.c SEE Testing Guidelines

- **SEE testing** should be focused on **destructive events**
  - **a single high-LET heavy ion** may be used to save beam time
  - **Implement mitigation for soft events**, but… unexpected SEFIs can always show up, especially in complex COTS (a simple ECC or CRC might be ineffective against them)
- **Proton sensitivity** can be derived **from heavy-ion sensitivity** for electronics with a threshold LET_{th} smaller than 15 $MeV \cdot cm^2 \cdot mg^{-1}$
  - Analytically (PROFIT, SIMPA, FOM) or by means of simulation, thus reducing the amount of testing required.
  - CORHA data show that the predictions can be underestimated or overestimated by a **more than one order of magnitude**.
  - Models developed many years ago for SEU:
    - Fewer materials in the semiconductor industry
    - Larger feature size





Examples of overestimation and underestimation of proton effects by PROFIT and SIMPA collected during CORHA

3.c SEE Testing Guidelines

Scenario	Criticality Level	Recommendation
LEO, low altitude and small inclination	Low	No testing
	High	Perform at least **board-level testing with protons**
LEO, MEO, GEO	Low	Perform at least **heavy-ion testing for destructive events** (single high LET) in critical components
	High	Full component level testing with heavy ions and optionally protons. If proton testing is waived, consider sufficient margin on modeling results.

- General SEE testing recommendations

Conclusions

- A **radiation hardness assurance** methodology suitable for low-budget missions, focused on COTS, has been proposed, leveraging the scientific literature and the experimental data collected in the frame of the CORHA project
- The proposed methodology is based on a standard flow, with suggestions and guidelines to reduce cost with the least possible increase in risk:
  - **Guidelines for exploiting** in the best possible way **existing data or technological information** about the EEE reduction of tested parts with increased design margin;
  - **Simplified SEE testing** targeting only destructive events, assuming mitigation for soft events is implemented;
  - Board-level testing
- It must be noted, however, that the **complexity of modern devices** which can feature hundreds or even thousands of operating modes, demands for more extensive testing rather than less