

# Advanced Data Handling Architecture (ADHA)

## Backplane Definition and Design

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# BACKPLANE DESCRIPTION 1/2

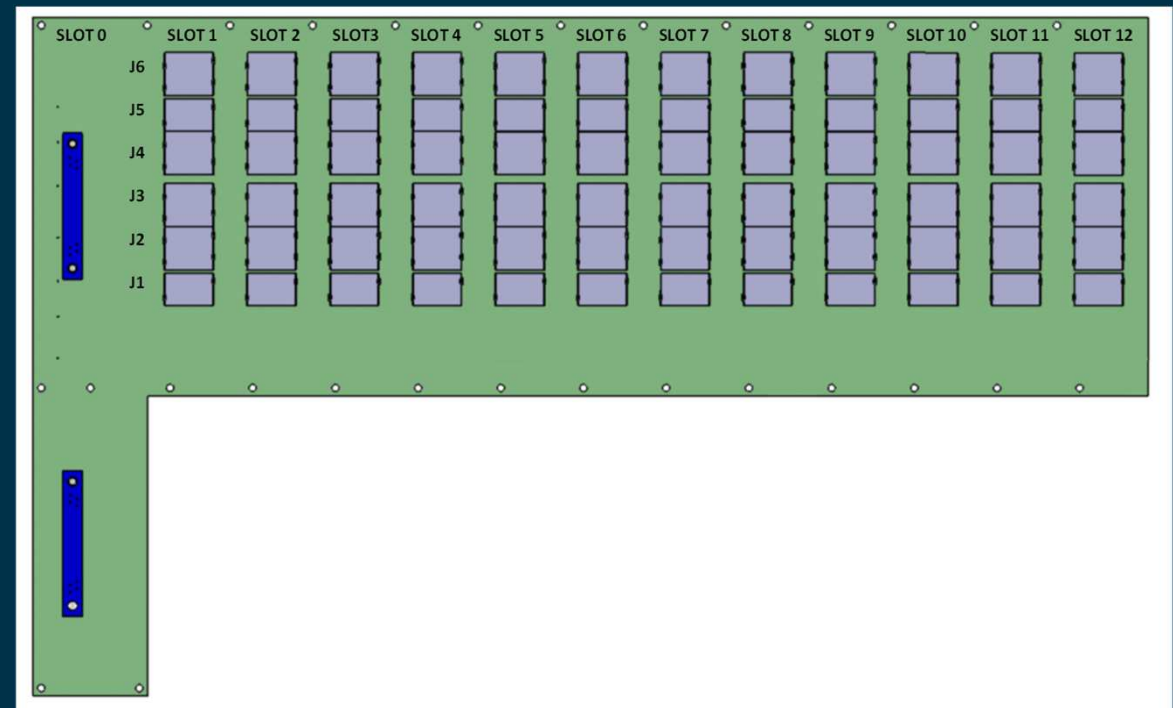
One of the standard ADHA element is the units' backplane, a crucial element for the standardization being the interconnection means between the modules.

It provides:

- Data communication links
- Monitoring links
- Control links
- Power distribution

ADHA standard 6U backplane hosts:

- Up to 12 modules with 6HP pitch
- 1 dual DC/DC module with 8HP pitch providing +12V (main), +5V (AUX) and +28V (for HPC)

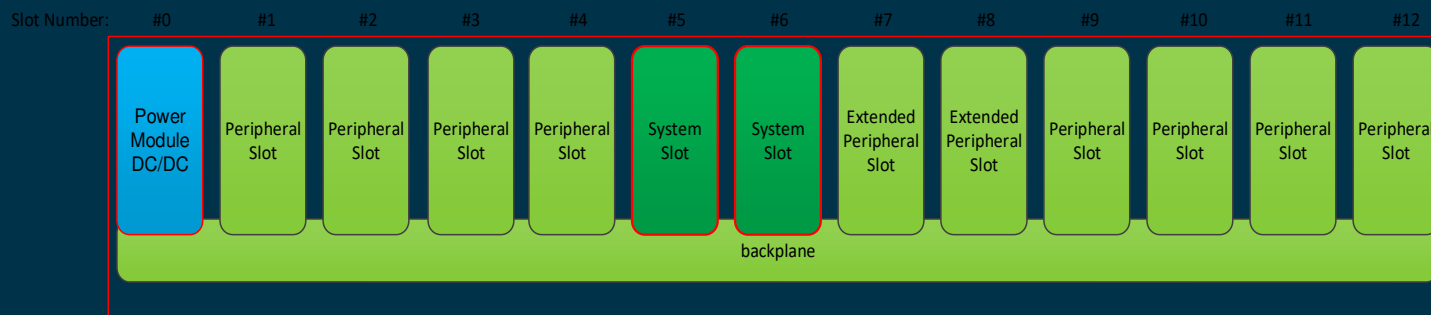


# BACKPLANE DESCRIPTION 2/2

ADHA backplane slots profile are subsets of each other:

- **system slots** provide the full functionality on the backplane implementing the Star Point for data links from/to the peripheral modules on **J6** and **J3** connectors, and the command and control of the unit on **J2** connector.
- **extended Peripheral slots** provide the Star Point for SpaceFibre from/to the peripheral modules on **J6** connector and receive the commands from **J1** connector.
- modules host in the **peripheral slots** can only receive commands from **J1** and exchange data with the central hubs from **J4** connector

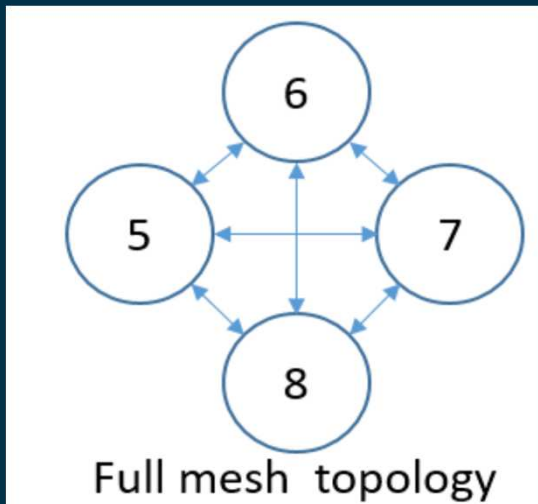
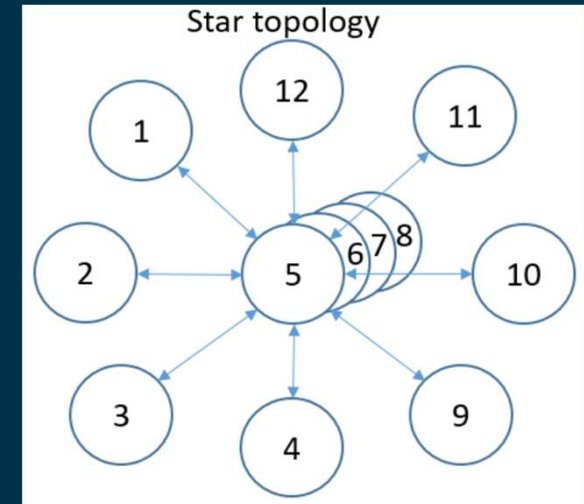
cPCI Standard	System Slot	Extended Peripheral Slot	Peripheral Slot
P6	Optional: Star Point of SpaceFibre	Optional: Star Point of SpaceFibre	Unused: General Purpose
P5	Unused: General Purpose	Unused: General Purpose	Unused: General Purpose
P4	Optional: SpaceWire / SpaceFibre	Optional: SpaceWire / SpaceFibre	Optional: SpaceWire / SpaceFibre
P3	Optional: Star Point of SpaceWire	Optional: Star Point of SpaceWire	Unused: General Purpose
P2	Source for Control Signal Pins (PSON, RST, Monitoring)	Unused: General Purpose	Unused: General Purpose
P1	Control Signal Pins Power Pins (12V, 5V, 28V)	Control Signal Pins Power Pins (12V, 5V, 28V)	Control Signal Pins Power Pins (12V, 5V, 28V)
P0	Optional, unused -> removed		



# DATA COMMUNICATION LINKS 1/2

Data communication links are based on Space Fiber (SpFi) and Space Wire (SpW).

- Space Fiber (SpFi) and space Wire (SpW) links are implemented in **star topology** from slot 5,6,7,8 to slots 1,2,3,4 and 9,10,11,12

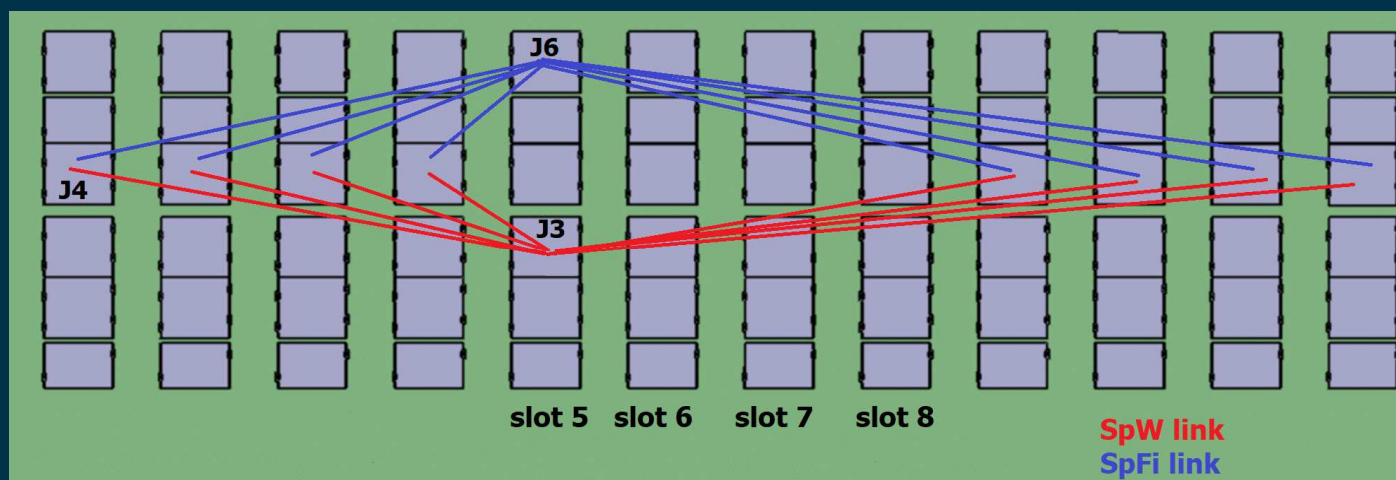


- Space Fiber (SpFi) and space Wire (SpW) links are implemented in **full mesh** topology between slots 5,6,7,8

# DATA COMMUNICATION LINKS 2/2

**SpW** single “star” links are routed from **J3** of slots 5, 6, 7, 8 to **J4** of the peripherals slots 1 to 4 and 9 to 12 supporting a data rate up to **200Mbps**.

**SpFi** links are implemented with 2x lanes (i.e. 2Tx and 2Rx) supporting a data rate up to **6.25Gbps/lane**. The SpFi links are routed from the **J6** connectors of slots 5, 6, 7, 8 to the **J4** connectors of the peripheral slots 1 to 4 and 9 to 12.



# COMMAND AND CONTROL

System controller in the slot 5 and 6 has in charge the Command and Control (C&C) of ADHA modules (shelf controller functionality). The management is done using:

- Busses (CAN) but SpW and SpFi can be used as well
- Discrete lines (PSON signals and RESET signals, SYNC signals)

Furthermore the geographical addressing is used to identify the physical slot position.  
The source of CTRL signals is **J2** connector of the system slots  
Control Signals (all slots) + Power Lines are received on **J1** connector

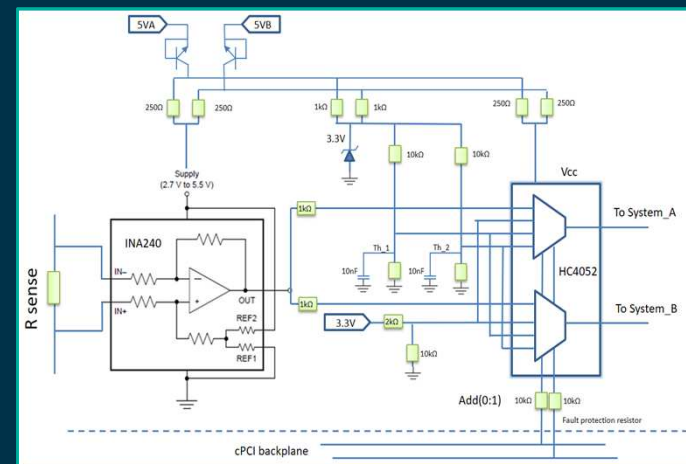


# HEALTH MONITORING SYSTEM 1/2

**HMS** is not specified in the CPCI SS, however an independent monitoring system is needed to monitor the status of the modules.

The **HMS** is able to acquire, from each ADHA module, 4 analogue parameters (4+4 parameters for 2FCG module in slot from 1 to 4) :

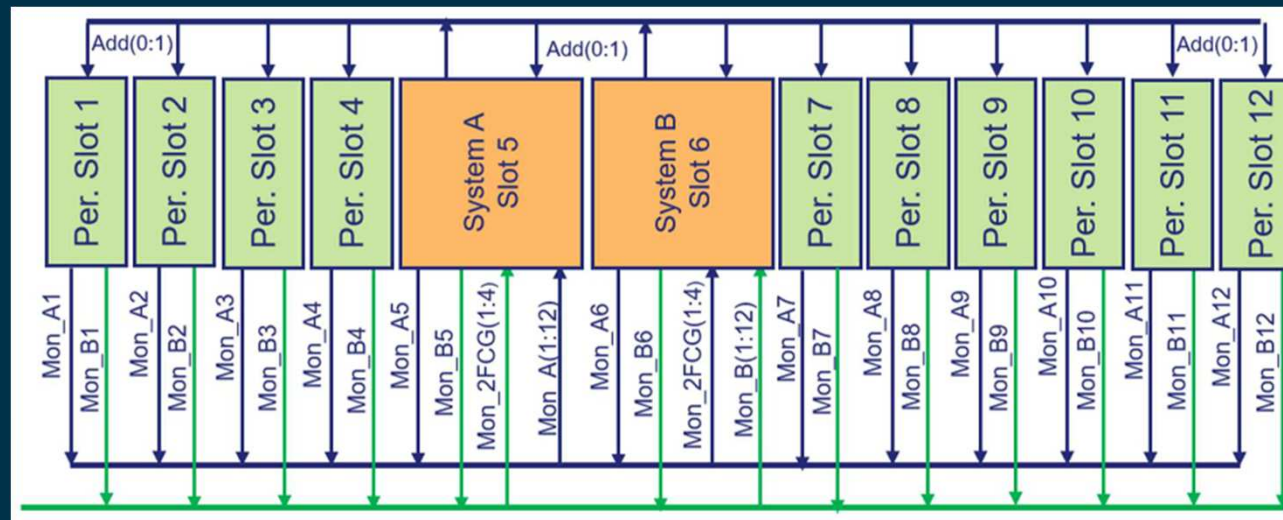
- +12V power line current (this is the main power line used by each module)
- A secondary voltage on the module (for example +3.3V )
- Two module's temperatures (host spot on the module defined by the manufacturer).





# HEALTH MONITORING SYSTEM 2/2

The acquiring system on the system module uses address Add(0:1) to select (cyclically) the monitored parameters, and convert the 16 analogue inputs (including its own parameters) into digital. Address lines are open-collector wired-OR routed through **J1** from System controller A and B to all the modules.



- HMS requires negligible PCB room and power consumption (< 0,5W over the 5V lines).
- It is always active in all the modules, independently if they are switched On or in failure.

The presence of HSSL leads to take care about the signals integrity, being the transmitted signals sensible to: impedance mismatch, crosstalk, stray capacitance that could cause signals degradation.

It is important to use a Printed Circuit Board (PCB) substrate materials with high-speed properties:

- Low dissipation factor  $D_f$  (to reduce losses)
- Low dielectric constant  $D_k$  (to reduce stray capacitance)

**Megtron6** or **EM-528K** are example of good high speed materials suitable for ADHA's PCB.

# MATERIAL, PHYSICAL BUILDUP AND ROUTING RULES 2/5

The feasibility ADHA-U1 study assessed that the ADHA backplane can be developed with minimum of 18 layers build-up. The layers build-up includes:

## 8 layers for signals routing:

- 48x4 SpFi strip-lines, 100Ω controlled impedance;
- 48x4 SpW strip-lines, 100Ω controlled impedance;
- 64x2 Single ended lines;
- 2x2 CAN bus differential lines, 100Ω controlled impedance
- 4x2 Sync differential lines, 100Ω controlled impedance

## 10 plane layers for GND and Power rails

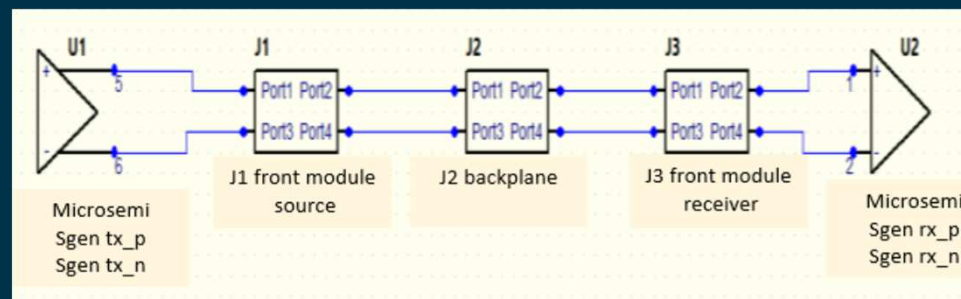
Layer	Stack-up	Description	Cu layer type	Finish thickness	
1		Plane	18,00		
2		MEGTRON6 R5775(K) 1080X2	Signal	150,00	18,00
3		2x Megtron6_R5670(K) 1080	Plane	87,00	87,00
4		MEGTRON6 R5775(K) 1080X2	Signal	150,00	18,00
5		2x Megtron6_R5670(K) 1080	Plane	87,00	87,00
6		MEGTRON6 R5775(K) 1080X2	Signal	150,00	18,00
7		2x Megtron6_R5670(K) 1080	Plane	87,00	87,00
8		MEGTRON6 R5775(K) 1080X2	Signal	150,00	18,00
9		2x Megtron6_R5670(K) 1080	Plane	87,00	87,00
10		MEGTRON6 R5775(K) 1080X2	Signal	150,00	18,00
11		2x Megtron6_R5670(K) 1080	Plane	87,00	87,00
12		MEGTRON6 R5775(K) 1080X2	Signal	150,00	18,00
13		2x Megtron6_R5670(K) 1080	Plane	87,00	87,00
14		MEGTRON6 R5775(K) 1080X2	Signal	150,00	18,00
15		2x Megtron6_R5670(K) 1080	Plane	87,00	87,00
16		MEGTRON6 R5775(K) 1080X2	Signal	150,00	18,00
17		2x Megtron6_R5670(K) 1080	Plane	87,00	87,00
18		MEGTRON6 R5775(K) 1080X2	Signal	150,00	18,00
		Plane	18,00	18,00	

Cu thickness=324.0 μ; Dielectric =2600.88 μ; Stack Up thickness = 2924,88 μ

The overall performance SpFi links depends on backplane and connectors. Each HSSL link consists of two differential pair: Tx+/Tx-, Rx+/Rx supporting a data rate up to 6.25 Gbps.

## Backplane SpFi routing rules are:

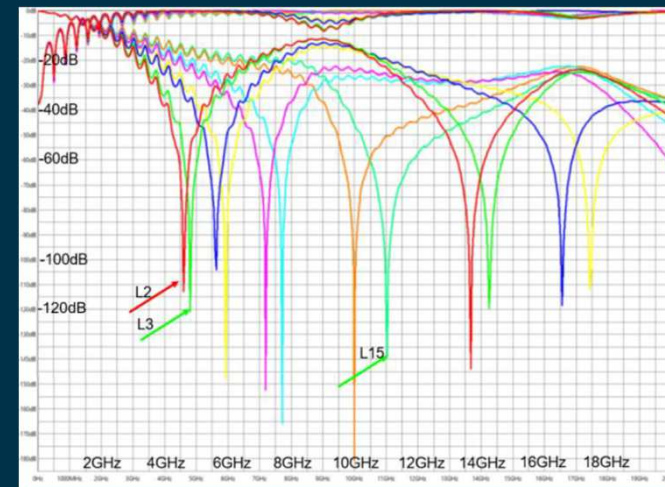
- Lanes have to be routed in dedicated layers from L17 to L11 to avoid stubs' effect and the need to implement the back drilling (layer as close as possible to the tip of the connector's pin)
- Lanes have to be routed end to end in a single layer (PCB feasibility studies assessed that  $\mu$ -vias can be avoided)
- 2Tx (2Rx) differential lines need matched length
- Non functional pads to be removed
- Final Routed lane needs **simulation**. Simulation has to be done from source to the receiver including models of transmitter-receiver (and their package), connectors and PCBs' routing.



**S11** (return loss), **S21** (insertion loss) and **crosstalk** are the most important parameters to evaluate the **HSSL** lane performances.

For lanes with a bit rate > 2Gbps **back drilling** of the via is needed.

In the figure below is reported a simulation with HyperLynx of **S21** in case of a 24 layers backplane with no back drilling. It shows not acceptable insertion loss.



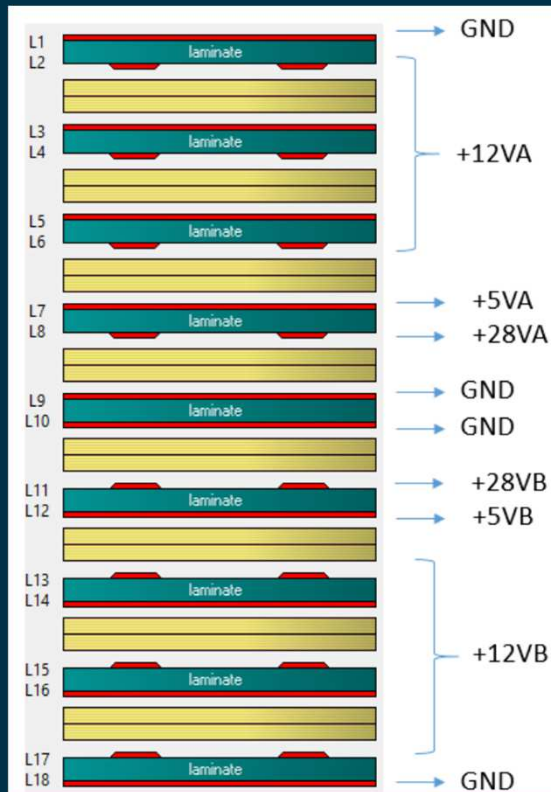
SpW links are implemented with 4 differential lines i.e. 2Rx (Din+/Din- and Sin+/Sin-) and 2Tx (Dout+/Dout- and Sout+/Sout-) supporting a data rate up to 200 Mbps.

## Backplane SpW routing rules are:

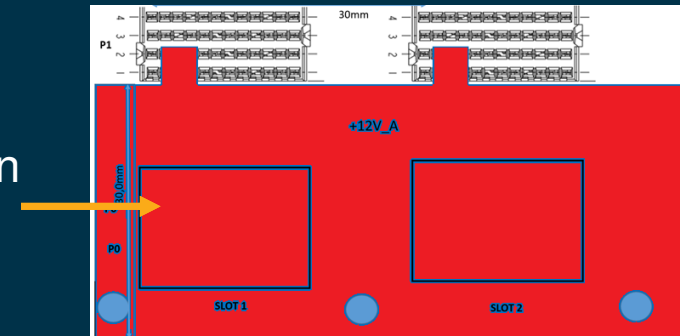
- Lanes have to be routed in dedicated layers from L17 to L11 to avoid stubs' effect and the need to implement the back drilling
- Lanes have to be routed end to end in a single layer (PCB feasibility studies assessed that  $\mu$ -vias can be avoided)
- Din and Sin differential lines need matched length
- Dout and Sout differential lines need matched length
- Final Routed lane needs **simulation** to evaluate signal integrity.
- Data-Strobe **skew** has to be simulated on the final routing of the backplane including the PCBs tracks on the modules.

# BACKPLANE POWER DISTRIBUTION

ADHA power rails are routed in a dedicated area of the backplane where J0 (optional connector of CPCI) is usually allocated.



J0 location



Double insulation requirement is applied to all power lines. Parameters to be analysed for signals at backplane are:

- Voltage drop at maximum rated current
- Voltage insulation between each power & GND lines
- Transients due to switch on of the modules (step load)



# CONCLUSIONS

- A state-of-the-art backplane design is done supporting the modular approach of ADHA.
- Compatibility of 3U- and 6U-Units with the same backplane is given.
- Interoperability and interchangeability of ADHA-modules is guaranteed by standardized slot profiles.
- Flexibility for 6U-module designs of the boards is possible by the available space for a specific backplane and/or additional connectors.
- High speed data links are demonstrated.
- Common command and control busses are implemented.
- Health monitoring system allows a continuous status acquisition.
- Proper power line implementation allows a power distribution along the complete unit.
- A cost efficient design for a wide range of re-use pave the way for a successful demonstration of the ADHA concept.

# About ADHA



This document is one of the series of ADHA documents intended to be applied together for the management, engineering and product assurance for developing and using ADHA products in space projects and applications. It can be publicly distributed by ESA and the ADHA industrial teams (ADS, TAS, and Beyond Gravity).

ADHA is a cooperative effort of the European Space Agency and European industry associations for the purpose of developing and maintaining ADHA products. This Document has been prepared by the ADHA Working Group in the frame of the study “**Advanced Data Handling Architecture (ADHA) Consolidation, Standardisation, and Product Suite Development**” (also called ADHA-2 study).

## PROPRIETARY INFORMATION

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