# Airbus Crisa

## GR740 Payload Controller Module – ADHA Compliant Next Generation Processing Module

CRISA

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# Introduction & Background

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## GR740 PCM development motivation

- There is an increasing market demand for reducing development and time costs of spacecraft avionics.

  Advanced Data Handling Architecture (ADHA) is an ESA initiative with the objective of setting a unified architecture to offer modularity, module reusability and interoperability, so development and integration times are reduced. Avionics for future ESA missions will be based on this standard.

- The market also demands high integration of processing capabilities, including high capacity on-board memory and higher data bandwidths

  Future missions will require the use of high performance processors with multiple-cores and with a significant increase of the on-board memories (for real time on-board processing and temporal storage) and availability of High Speed Serial Links for data transferences

- Flexibility and reuse is a must in order to adapt existing designs to different missions

  The use of high performance reprogrammable FPGAs is a trend in the space industry and provides the required flexibility to the products to foster reusability

# Introduction & Background

- Background
  - Airbus Crisa started the development of the GR740 PCM in 2021 in the frame of an internal R&D and partially supported by CDTI funds.
  - The board was baselined for the processing module (PM) of the PILOT instrument on board lunar lander and it was in charge of performing the functions of visual navigation and hazard avoidance in an autonomous manner on-board the spacecraft.
  - Initial design of the GR740 PCM board was aligned with the preliminary ADHA standard (not fully frozen), therefore it presented some deviations with the latest ADHA requirements.

However:

- PILOT program was cancelled by mid of 2022.
- More mature ADHA specifications were released by ESA and the industry

**Airbus Crisa took the decision to resume the development by migrating the initial concept defined in the frame of PILOT to a fully compliant ADHA System Slot module**

# GR740 Payload Control Module Overview

# What is the GR740 PCM?

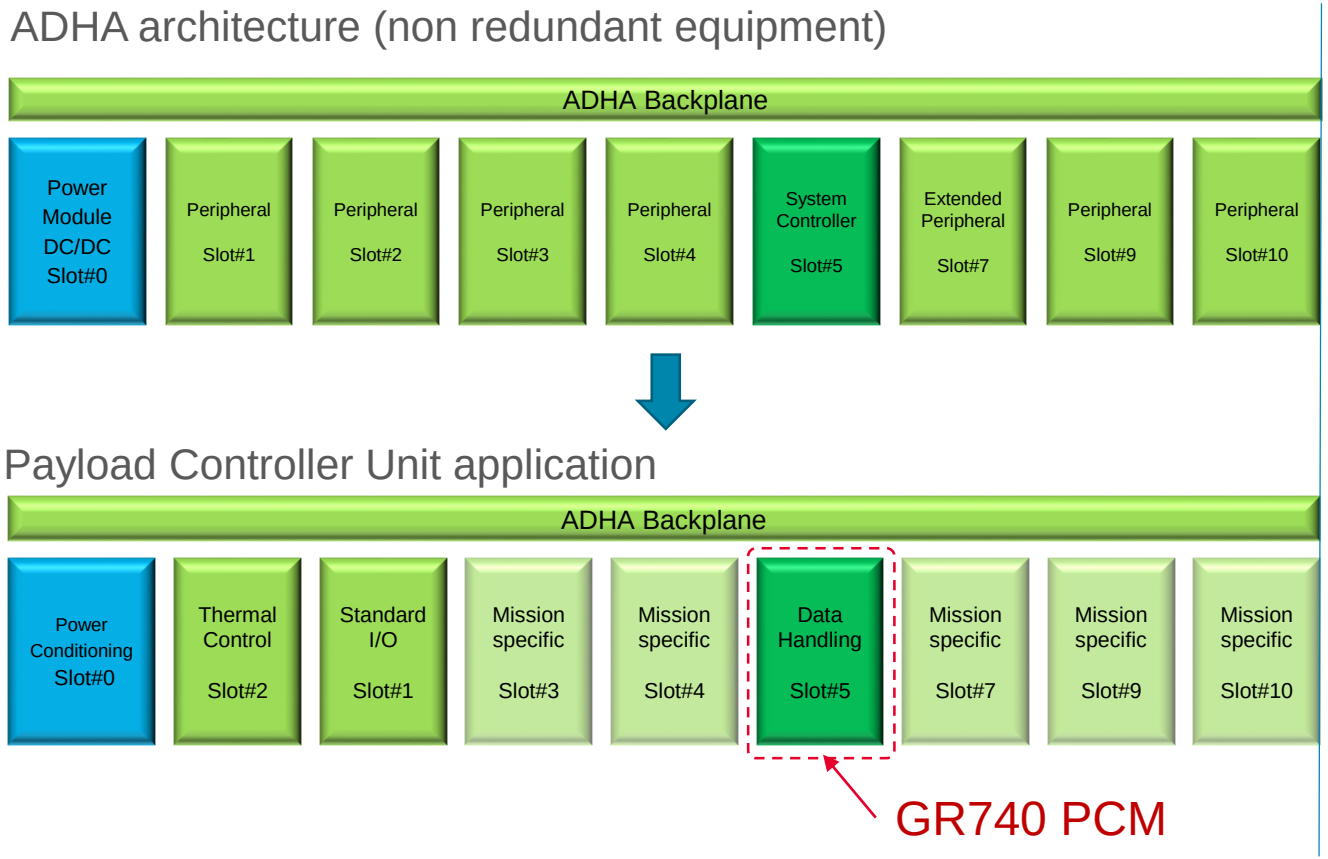
- The GR740 PCM is a high-performance module based on a multi-core LEON4-FT processor and a powerful flash-based reprogrammable FPGA
- It is conceived as a general purpose Payload Controller Board.
- This module fits in a modular architecture based on an ADHA standard unit and performs the System Slot functionality
- Form factor is cPCI Serial for Space 6U with extended depth (220mm) and 6HP pitch.

# GR740 PCM in an ADHA rack

- ADHA standard defines a unit concept with an envelope with up to 13 modules:
  - N & R chains in Slot #0: Power module
  - 1 N & 1 R system controller
  - Up to 5 N & 5 R peripherals

- ADHA concept is very flexible and allows multiple avionic unit configurations according to mission needs.

- The GR740 PCM product is conceived to manage up to 7 peripherals with no internal cross-strapping (typical configuration for Payload Controller Modules: Instrument Control Units, Antenna Control Electronics, etc.)







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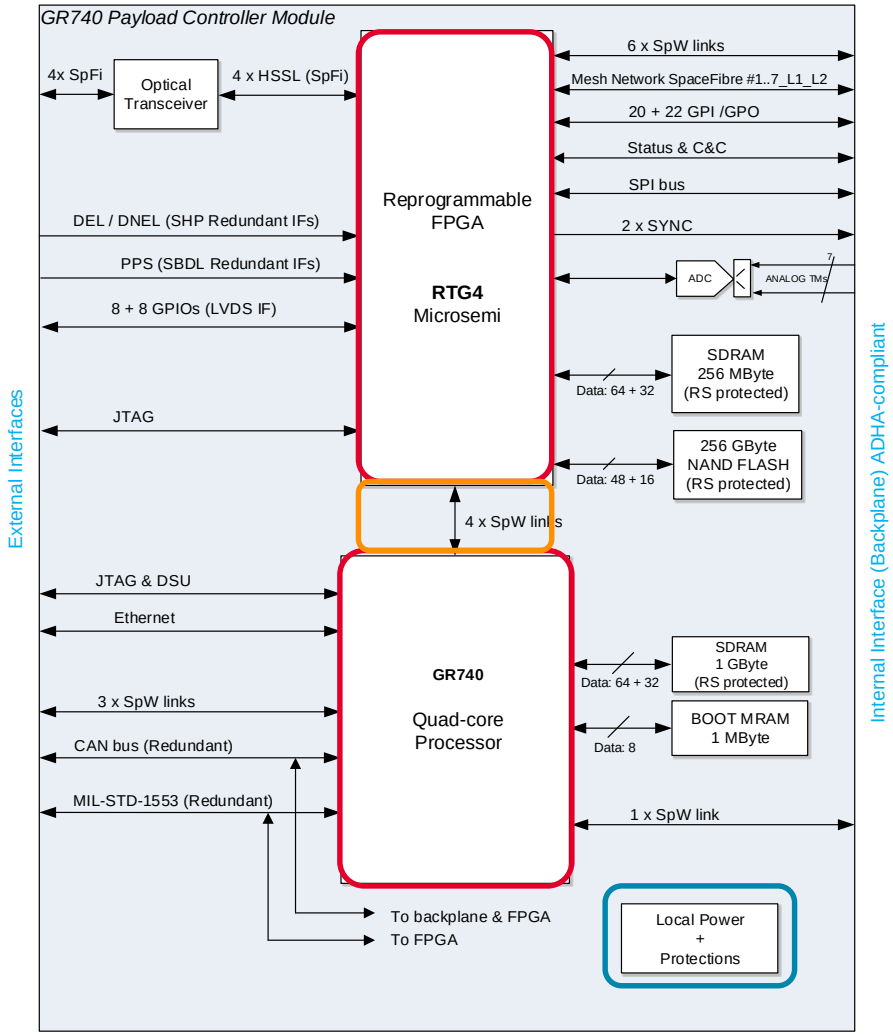
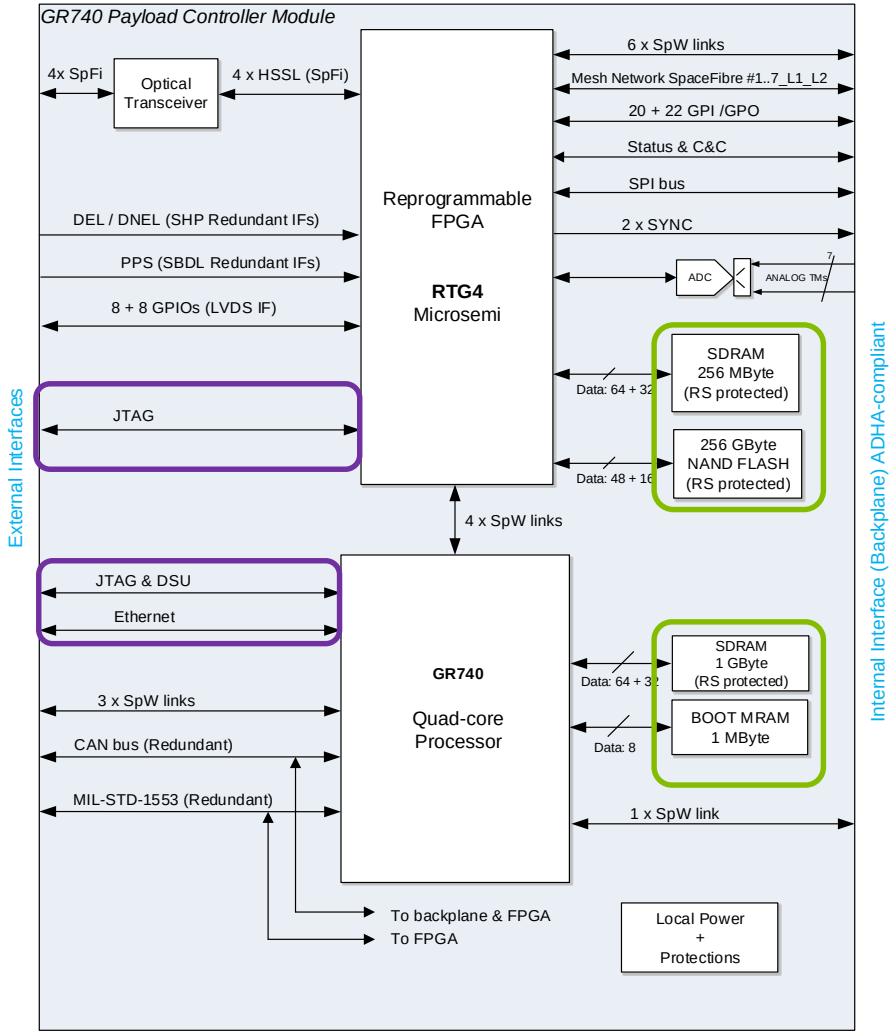
# GR740 PCM Performances




- GR740 Processor (LEON4-FT), processor core running at 250MHz (459 DMIPS single core, 1,744 MIPS aggregated capability for quad cores)
- RTG4 Companion FPGA (Microchip Flash based technology) – Reprogrammable on ground (with unit closed)
- Processor & FPGA connected through 4 x 200Mbps SpW links
- Powered at +12V main secondary power supply
  - Local supply rails generated by POL and LR
  - Overvoltage and LCL/RLCL protection for external failure propagation avoidance
  - Optionally supplied from +3,3V as a main power supply (non-ADHA applications)

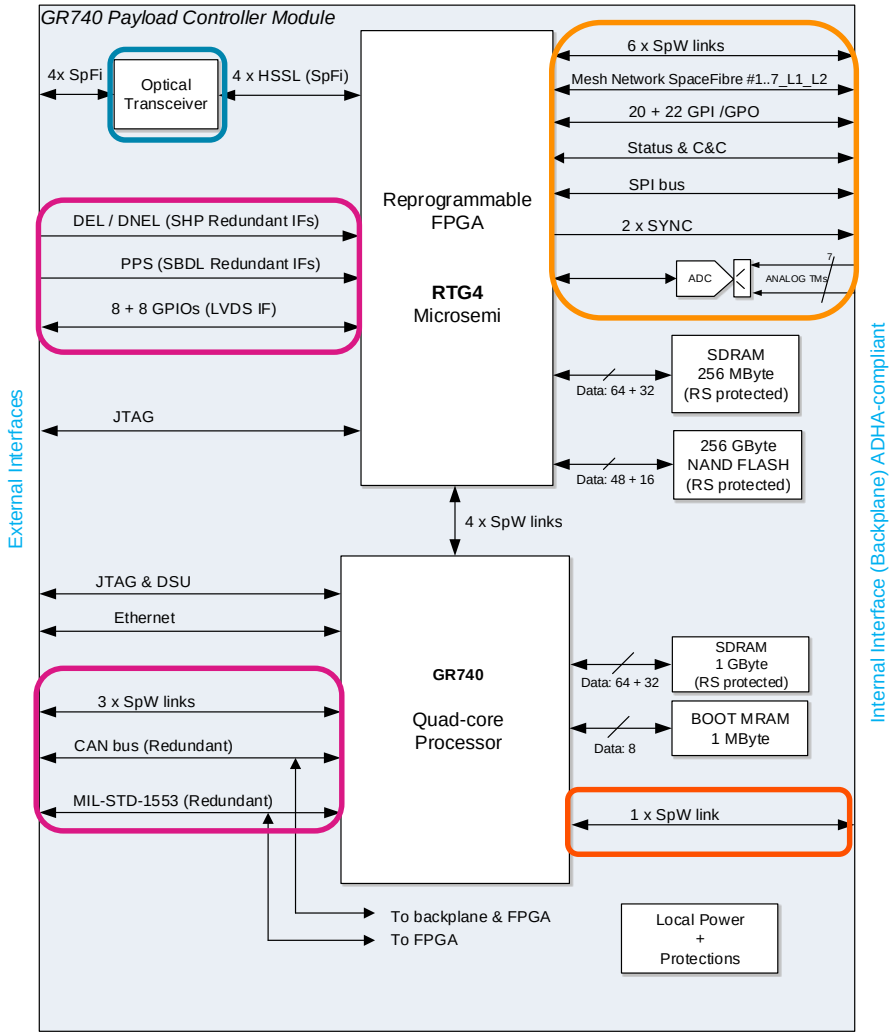
# GR740 PCM Performances




- Memory banks
  - 1 Mbyte BOOT MRAM memory (optional, for long term storage missions)
  - 256 GByte NAND FLASH NVM for Boot, ASW and Scientific data Mass Memory
  - 1GByte processor SDRAM bank (RS protected, 64+32).
  - 256 MByte FPGA external SDRAM bank (RS protected, 64+32) - optional

- Debugging interfaces (available in front panel connectors)
  - SW debug interface via JTAG, DSU and Ethernet
  - FPGA bitstream on ground programming via JTAG

# GR740 PCM Performances




- External interfaces (available in front panel connectors)
  - 3 x SpW interface , 200Mbps, LVDS standard.
  - Dual 1553 bus (BC/RT configurable)
  - Dual CAN bus
  - Ethernet bus (initially for Debug purposes)
  - Redundant DEL / DNEL & PPS interfaces, SBDL PHY.
  - 8+8 LVDS GPI/O connected to FPGA (functionality mission dependent)
- External interfaces (available in rear panel connectors)
  - High Speed Optical Serial Lines (4 lanes x 3,125Gbps) over SpaceFibre
- Internal Interfaces (available in backplane connectors)
  - 7 x SpW interface, 200Mbps, LVDS standard. For high data throughput slots connection
  - 1x SPI interface, up to 10Mbps (for legacy products)
  - Dual CAN bus. For low data throughput slots connection
  - 20 GPIs+22 GPOs connected to FPGA (mission dependent)
  - Analog telemetries acquisition function (HMS)
  - 7 HSSL SpaceFibre mesh network

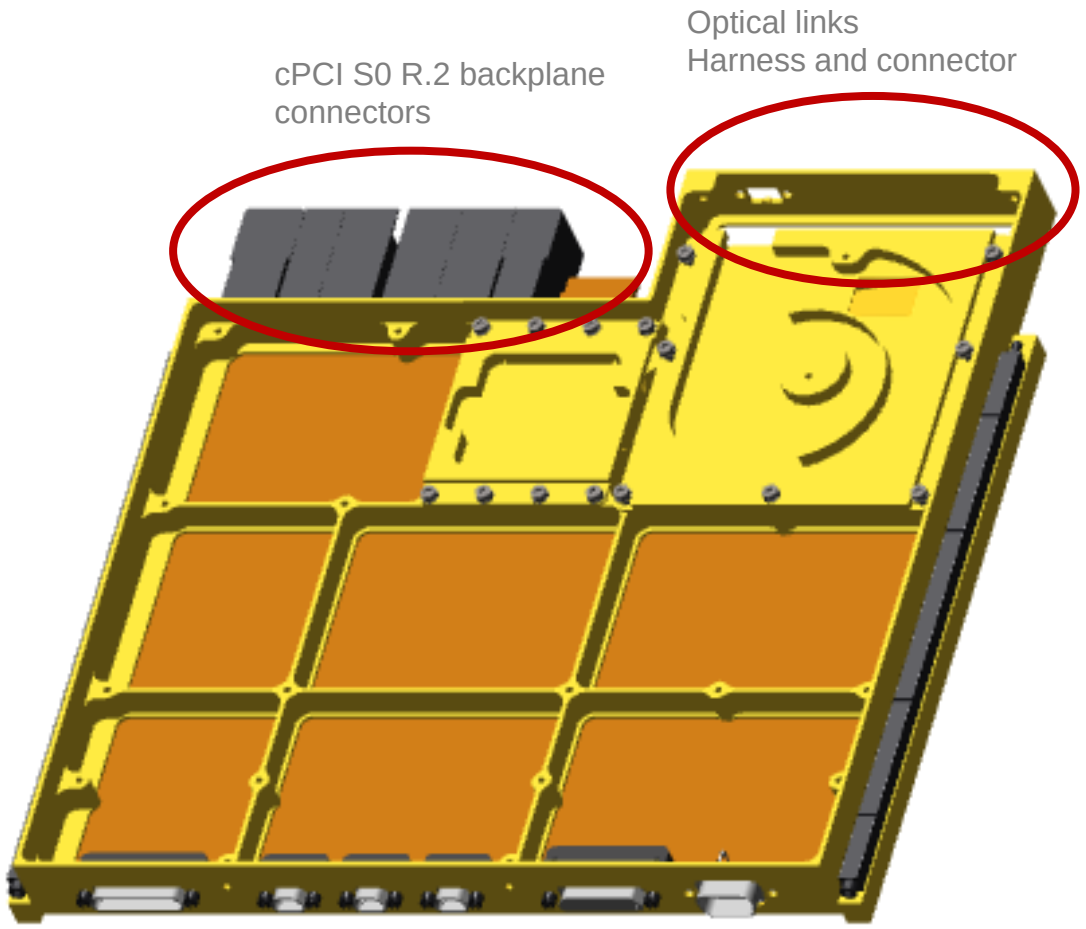
# GR740 PCM Mechanical Design & Interfaces

- cPCI SS 6U with extended depth (220mm) and normalized pitch of 6HP (compatible also with 5HP without optical link).

- Front panel interfaces:
  - 1x MIL-STD-1553
  - 3x SpW links
  - 8+8x GPO/GPI LVDS/SBDL lines
  - Debug & Utility connector
    - Dual CAN bus
    - Redundant PPS/DEL/DNEL
    - Ethernet for debugging
    - JTAG for FPGA bitstream upload

- cPCI S0 R.2 backplane connector (compliant with ADHA standard)

- Rear panel connector for optical links in direct rear I/O backplane zone as per PIGMC cPCI S0 R.2



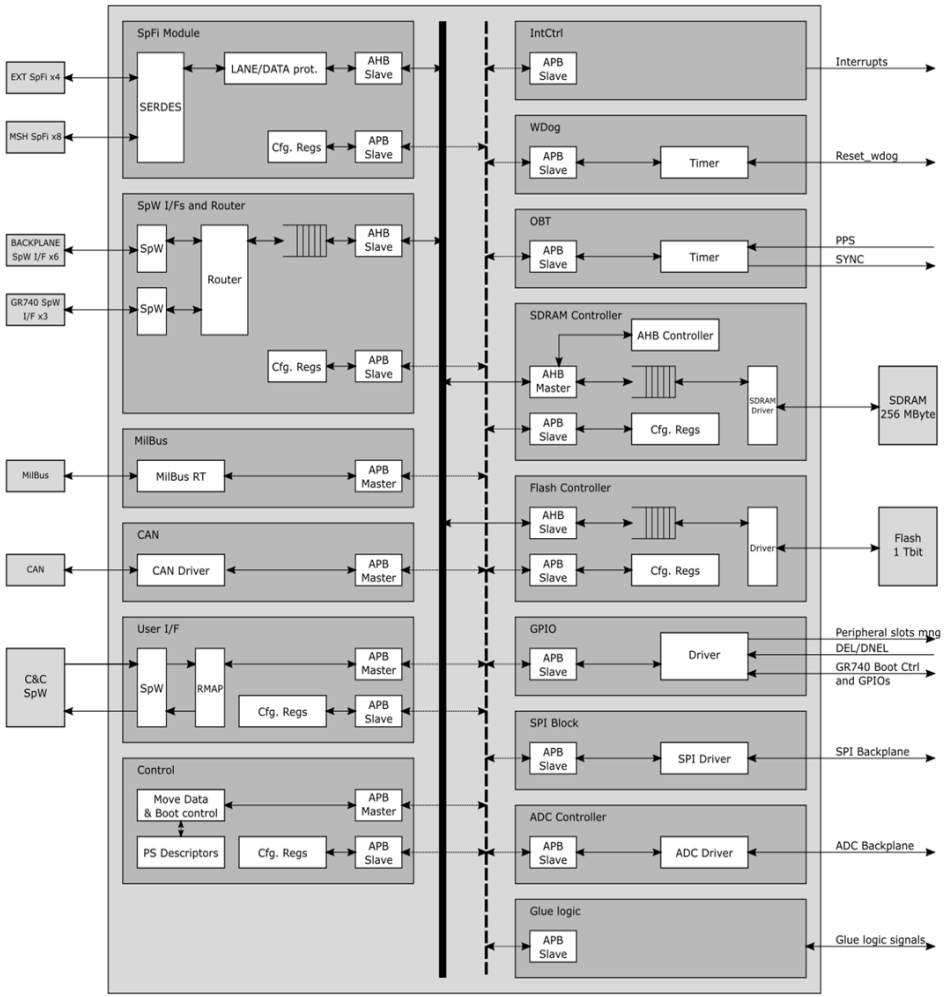
# Software overview

## Two SW products are developed to support the GR740 PCM operation:

- Boot Software (BSW). BSW is intended as a very basic booting SW. Additional functionality could be added as per specific project requirements, such as mode management, multi-product loading or PUS TM/TC capability
  - executed when GR740 PCM is powered up or reset
  - Nominally: stored in the Mass Memory and it will be loaded in RAM upon reset by FPGA, using the Boot by SpW feature of the CPU
    Optional: stored in MRAM for for long term storage missions
  - not patchable in flight but can be patched on ground
  - in charge of the GR740 PCM HW initialization, built-in test (BIT) and copy to RAM and transfer control to Application SW (ASW) which is stored in flash memory

- Hardware Dependent Software (HDSW). The purpose of the HDSW Drivers is to hide the low level HW features from the ASW
  - A passive library of functions, to be linked together with the OS and APSW.
  - Developed in C language
  - Independent from any Operative System used for ASW

# FPGA overview




- The FPGA used in the Processor Module is the RTG4 from Microchip
- Reprogrammable on-ground at closed unit
- Functionality (for the R&D)
  - Boot and ASW download from FLASH through an additional RMAP SpW Link connected to the GR740 processor.
  - User Communications through the previous SpW Link.
  - Routing between 3 SpW Links connected to the GR740 processor and 3 SpW Links connected to the backplane (path addressing and round-robin priority management)
  - Drive the external SDRAM devices
  - Drive the external FLASH devices.
  - Drive the external ADC device.
  - LOBT. Time stamp and LOBT general management.
  - Manage general purpose I/O (GPIO).
  - 4+4 Space fiber nodes (backplane/external) with static routing table capability (switch matrix).
  - Watchdog.
- Design can be customized depending on specific Mission processing needs

# FPGA budgets

| Block | FF | LUT | LRAM | uRAM |
|---|---|---|---|---|
| BP SpFi lanes (x4) | 11272 | 15776 | 16 | |
| External SpFi lanes (x4) | 11272 | 15776 | 16 | |
| SpFi switch matrix | 10000 | 15000 | | |
| 6x SpW nodes + router | 5000 | 7500 | 6 | |
| Control | 1000 | 1700 | | |
| User Interface | 1500 | 1000 | 1 | 4 |
| Interrupt Controller | 50 | 50 | | |
| Watchdog | 75 | 75 | | |
| Local On-Board Time | 300 | 400 | | |
| SDRAM controller | 1000 | 700 | 1 | |
| Flash memory controller | 2000 | 1400 | 1 | |
| GPIO management | 100 | 100 | | |
| HMS management | 500 | 250 | | |
| Glue logic | 50 | 100 | | |
| | | | | |
| Total cells | 44119 | 59827 | 41 | 4 |
| RTG4 max. resources | 151824 | 151824 | 209 | 210 |
| Occupation | 29% | 39% | 20% | 2% |
| Margin | 71% | 61% | 80% | 98% |

Good overall margins!

It allows implementation of specific functions mission dependent





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# Compliance with ADHA standard


 

# Compliance with ADHA standard

- Qualified PoL with Vin compatible with ADHA voltage (and high current) still not available

GR740 PCM baseline uses a PoL ADHA compliant. QML-V version expected to be ready for the first flight mission
As backup, for non-ADHA applications, the GR740 PCM allows supply from +3V3 so maximum flexibility will be guaranteed.

- cPCI S0 R.2 backplane connectors compatible with flight environment still not available.

Not expected impact on GR740 PCM as per cPCI SS specification document.
Minor PCB redesign would be needed depending of the qualification schedule.

- Limited space to allocate external connectors. 6HP pitch for ADHA module seems unavoidable

Baseline for Airbus Crisa ADHA modules is the use of 6HP pitch by default (as defined for the ADHA EM). Rear connector is implemented in the user defined area to implement the optical links. Customization of the ADHA rack could be needed (this area is not standardized yet).

# Compliance with ADHA standard

- Complex PCB stack-ups for managing HSSLs

HSSL links at backplane connector interface require very controlled PCB stack-up and tracks design to minimize insertion losses. New PCB materials and processes (e.g. Megtron-6 and backdrilling) and project level qualification could be required.

- Risks linked to maturity of the ADHA standard (PDR level)

ADHA standard could evolve until reach higher TRL
Risk of PCB redesign is possible but modifications should be minor

# Development Status and way-forward


 

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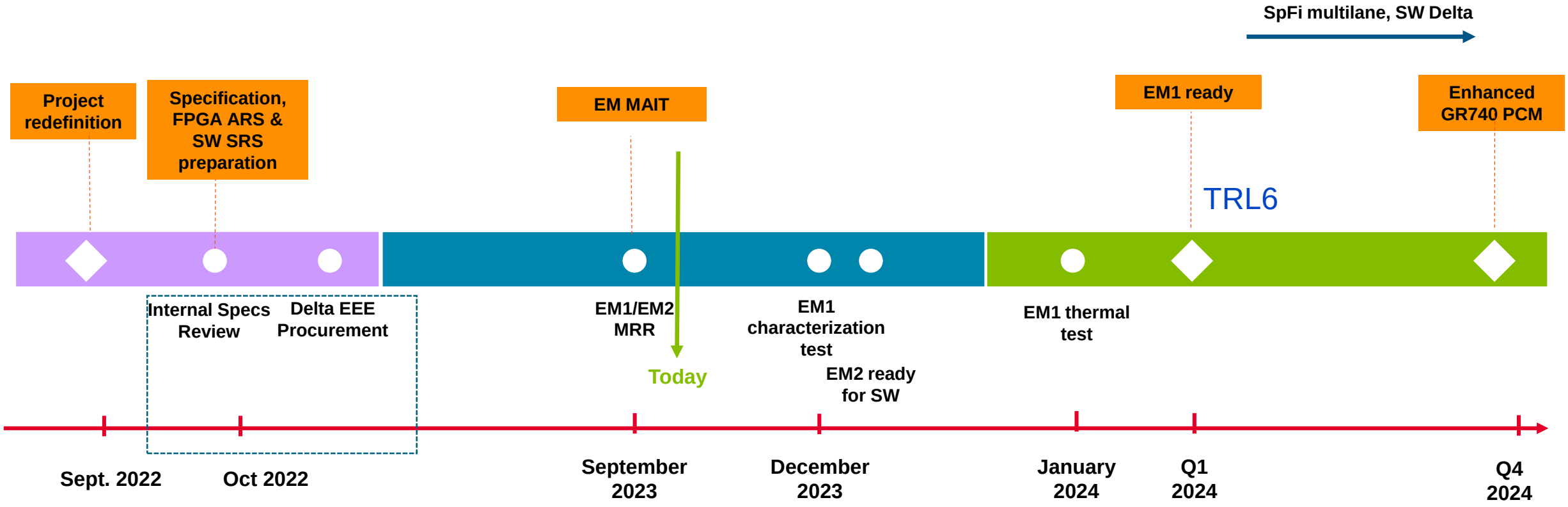
- Development of the GR740 PCM product is accomplished in two stages:
  - 1st stage consists of full HW design (including PA activities), basic SW and FPGA functions design, 2x EM manufacturing with full characterization testing (including thermal cycling) to reach TRL6.
    - FPGA design: currently developing the required basic functionality in the FPGA for board operation and full characterization:
      - Boot control
      - Mass memory controller
      - Other functions required for the application (SpW, time datation functions, etc.)
    - SW design: SW for board operation and full characterization:
      - Initialization routines (self-check and ASW loading)
      - HDSW (module drivers, including GR740 processor)
      - Other functions required for the application

1st stage:
From 2Q2022 to 1Q2024

  - 2nd stage will cover the development of enhanced performances/functions
    - Complete HW characterization including advanced features (SpFi over fiber)
    - FPGA complete functionality
      - SpFi interfaces, optical and electrically coupled
      - External (optically coupled) SpFi links with single and multi-lane capability
    - SW design:
      - SW drivers to C&C enhanced functions

2nd stage:
From 1Q2024 to 4Q2024

# Development Status and way-forward



# Conclusion

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- The GR740 PCM processing module currently in development will be the baseline of Airbus Crisa for future Payload Controllers in ADHA compliant equipment
- The GR740 PCM can provide enough flexibility to be used as a system controller (or extended peripheral with deviations). This allow to easily adapt the board at manufacturing time to the target application, not only devoted to payload control but also to others such as navigation, spacecraft on-board computers
- TRL6 will be achieved by beginning of 2024 with a basic functionality in FPGA and SW items
- Enhanced capabilities will be added to the product along 2024
- ADHA standard is currently well mature (PDR hold by 2Q23) however some minor evolutions could appear. Risk of PCB redesign is possible but modifications should be minor and not affecting the overall qualification status of the product

# Thank you



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