





The Development of an Onboard Processing Environment within the Flexible and Intelligent Payload Chain Sub-system for Small EO Satellites

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# The EO Data Bottleneck Challenge & Onboard Processing

 Earth Observation (EO) satellite platforms face prominent challenges surrounding efficient data delivery in the face of a growing onboard data bottleneck

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- However, advancements in onboard processing architectures can be exploited by mission integrators, satellite customers and data end-user alike
- Whereby, developing and deploying capabilities to maximise usable data delivery throughputs and timely information extraction can increase the effective return on investment of EO satellites

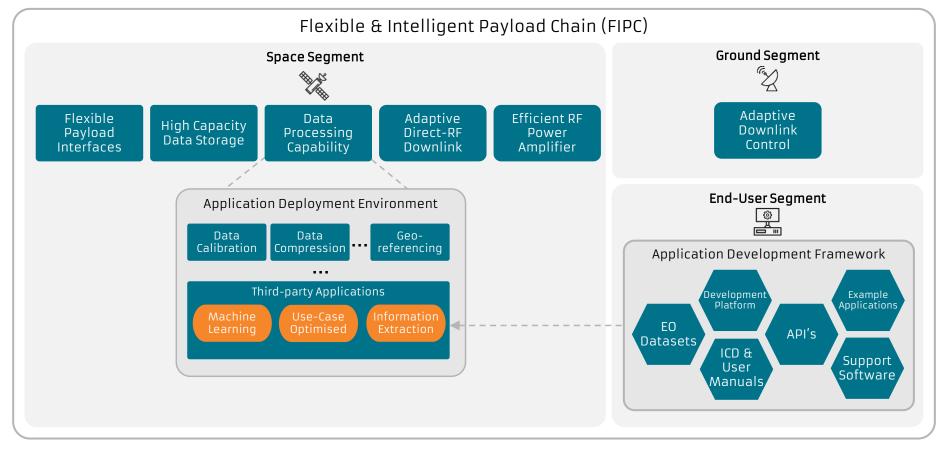
### A New Small Satellite Payload Chain Architecture

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SSTL's new Flexible and Intelligent Payload Chain (FIPC) is designed specifically to tackle the data bottleneck with advanced hardware and new software defined onboard data processing pipeline



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### **FIPC Architecture Overview: HSDR-X**

HSDR-X: High Speed Data Recorder with eXciter

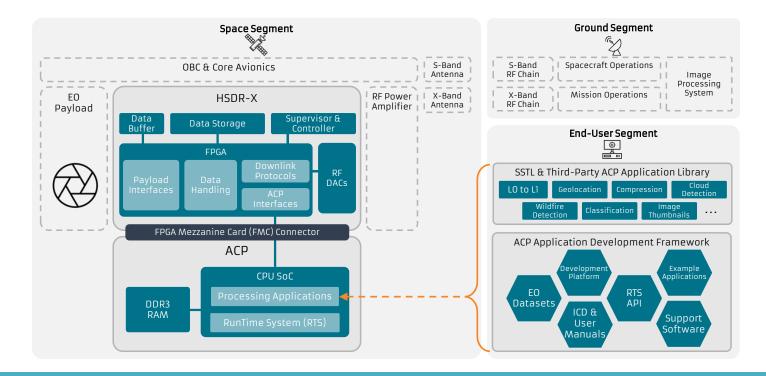
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- Central space segment module in the FIPC sub-system architecture:
  - Flight qualified in-orbit reconfigurable COTS FPGA for payload interfacing & low-level data handling;
  - Non-volatile high-capacity NAND flash for payload data storage;
  - Mezzanine interface for expansion/ tailoring of the product to meet mission specific requirements;
  - Bridge between the payload electronics and RF downlink in the satellite data delivery chain



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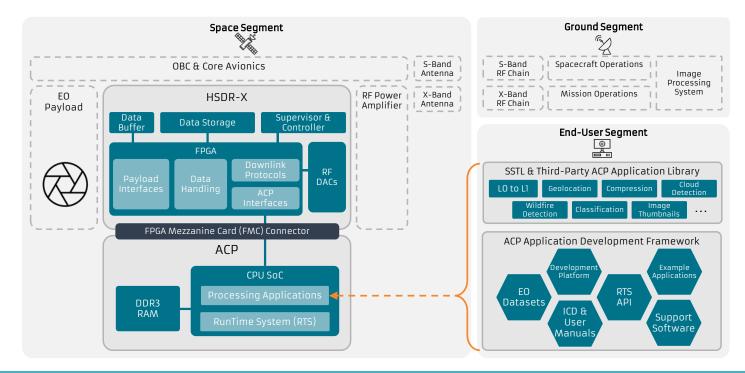
### **FIPC Architecture Overview: ACP**

• ACP: Auxiliary Compute Peripheral

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- Daughterboard to addresses the need for greater computing resources on-board:
  - Based around a flight-proven embedded multi-core CPU with on-die FPGA hardware;
  - Features architecture optimised high-speed data interfaces to the HSDR-X;
  - Support execution of computationally intensive tasks e.g. image processing & ML information extraction;
  - Software defined capabilities are facilitated by the new Run-Time System (RTS) deployment environment

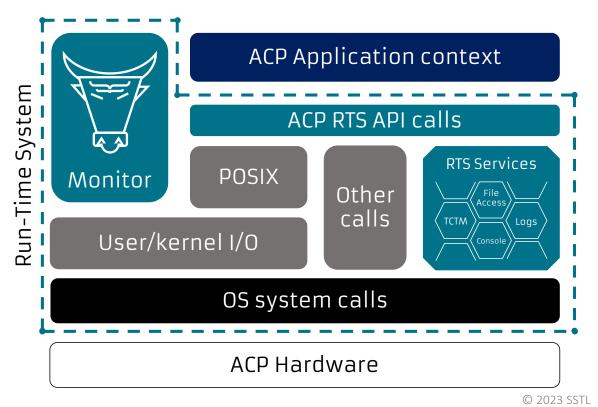


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## **Design of the ACP RTS Environment**

- The RTS is a new client-server based portable & modular functional software environment for onboard data processing Application execution on the ACP
- It provides the Application context access to hardware resources & software interfaces on the ACP & HSDR-X
- It employs a high degree of separation & segmentation between:
  - the underlying hardware architecture
  - the core firmware infrastructure
  - the software systems needed spacecraft module operations
  - onboard data processing elements
- This ensures the RTS is not an overly restrictive 'sandbox' & aids third-party Application development



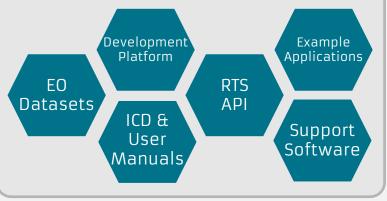
### FIPC End-User Segment: ACP Application Development Framework

- The FIPC product offering is more than just space hardware and software;
- The accompanying development framework is critical to enable third-parties and customer to effectively deploy end-user tailored & high performance onboard processing capabilities

End-User Segment

SSTL & Third-Party ACP Application Library

ACP Application Development Framework



- The ACP RTS currently includes C and Python API's
  - The RTS also supports third-party libraries and packages, such as OpenCV, NumPy, Pandas, Tensorflow Lite and PyTorch
- All Applications are deployable in-orbit for flexibility & adaptability over an entire mission lifetime

# ACP Application Demonstration - ESA InCubed Consortium

### Surrey Satellite Technology Limited (SSTL)

 Pioneers of audacious new satellite technologies, products and services leveraging extensive in-house capabilities & experience on end-to-end satellite mission design



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### Craft Prospect Limited (CPL)

 Deliver mission-enabling products & novel applications to realise SMART SECURE SPACE with expertise in areas including system engineering, autonomy, artificial intelligence & embedded systems

### University of Surrey (UoS)

 World-class university committed to research excellence and seeks to answer global challenges, drive innovation and deliver real-world impact 0 2023 S

# SSTL CCSDS-123 Image Compression Application

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- CCSDS-123 is a lossless and near lossless predictive image compression algorithm designed for low complexity processing of multispectral and hyperspectral data sets
- SSTL has implemented a C software Application compatible with the ACP RTS for deployment to the FIPC sub-system
- The Application was developed with the aims to demonstrate the benefits of deploying the CCSDS-123 algorithm on near-future SSTL small EO satellites
- Results from an initial test campaign conducted on a subset of 35 SSTL Carbonite-2 on the FIPC COTS Development Kit platform:

Average Runtime (Seconds)		Throughput (MSamples/Sec)			Compression Ratio		
1536x1536x4 (Pixels)	2560x2560x4 (Pixels)	Average	Min.	Max.	Average	Min.	Max.
9.71	27.0	1.23	1.18	1.34	1.88	1.69	2.04

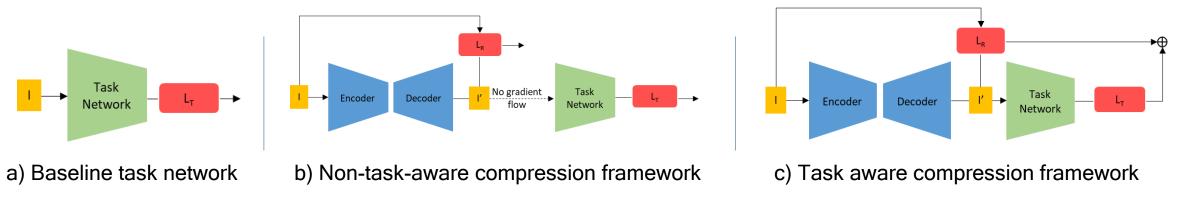
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# University of Surrey Variational Autoencoder Application

- A key novelty of this work and differentiation from traditional image compression schemes is that the reconstructed data will target specific features and data important for further onwards ML based processing and not human consumption.
- The work contains 3 sub-models which are split across the downlink chain and the autoencoder compression Application itself is configured as a python file

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 The proposed network architecture focuses on rapid and efficient decimation for the onboard FIPC application encoder, coupled with a more complex and compute heavy decoder on the ground side



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- SSTL's FIPC sub-system provides an innovative end-to-end solution harnessing the latest technologies & flexible use-case tailored approach to increasing the value for money to EO satellite customers
- New ACP RTS Application deployment environment and end-user development framework has been designed to facilitate both inhouse and third-party advanced onboard processing capabilities

 Novel FIPC compatible data processing Applications from SSTL, CPL and UoS will soon be deployed and verified on a flight representative hardware testbed



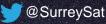




# Thank you

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