



Required Technology and Process Steps for Electrical Architecture and Harness Enhancements in Earth Observation and Science Missions

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DEFENCE AND SPACE

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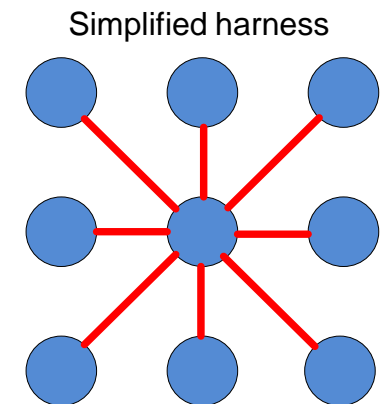
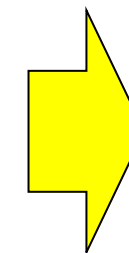
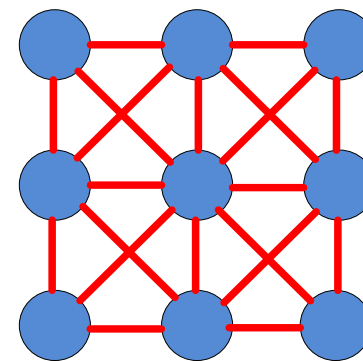
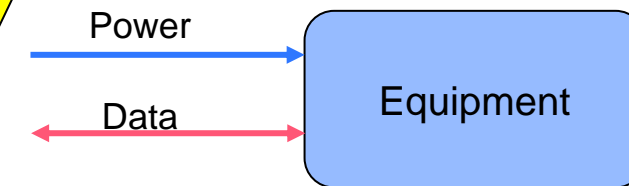
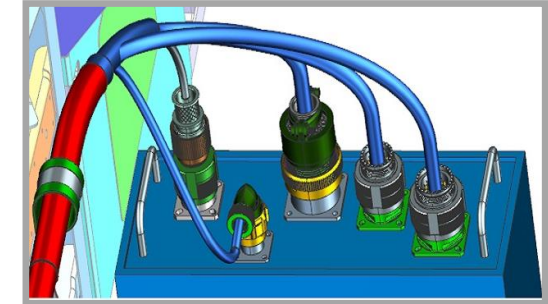
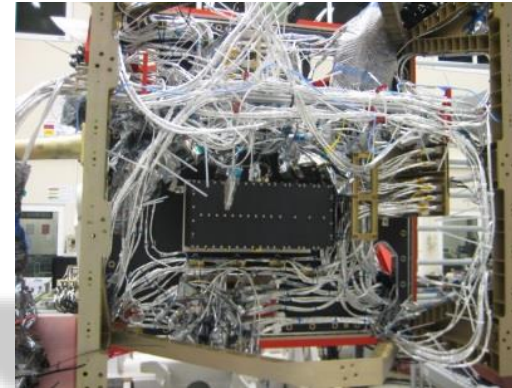
Electrical Architecture and Harness Enhancements

Introduction

- Electrical architecture is driven by available
 - products and heritage
 - processes and available tool environment
- Missing on-board digitalization still requires
 - many discrete interfaces
 - complex harness definition, implementation and verification effort
- Increase of data rates in future programs demands for proper resources for hardware and protocols
- Development, implementation and verification of electrical architectures in space programs lacks standardization

Overall, a standardized, efficient definition and efficient implementation of an electrical architecture seems desirable.

Electrical Architecture is key for cost efficient system design but often neglected



Reduction of interfaces and thus simplification of harness topology with reduced connections

Electrical Architecture and Harness Enhancements Expectations and Digitalization

Manifold expectations ... in many areas ...
towards lower cost and better industrialization

Design

Simplification: Best only power and data connections – no other discrete interfaces

Digitalization: Supported by trend to FPGAs and miniaturization → digital serial link for data communication available

Prerequisites: Cost efficient, standard interface components, standard functional allocation

Payload chain: Compatible with on-going increase of data rates for communication links and processing power

Standardized and modular for scalability and exchangeability

Design effort and impact of electrical architectures often underestimated as it fixes the functional allocations and interconnection complexity, mass and integration time

Proper industrialization, testability and accelerated integration and testing

Support distributed architectures with de-centralized computing functions like instrument control units or remote interface units for dedicated discrete interfaces

Design Process

Efficient, digitalized design process from top level architecture to functional channels to harness pin to pin definition

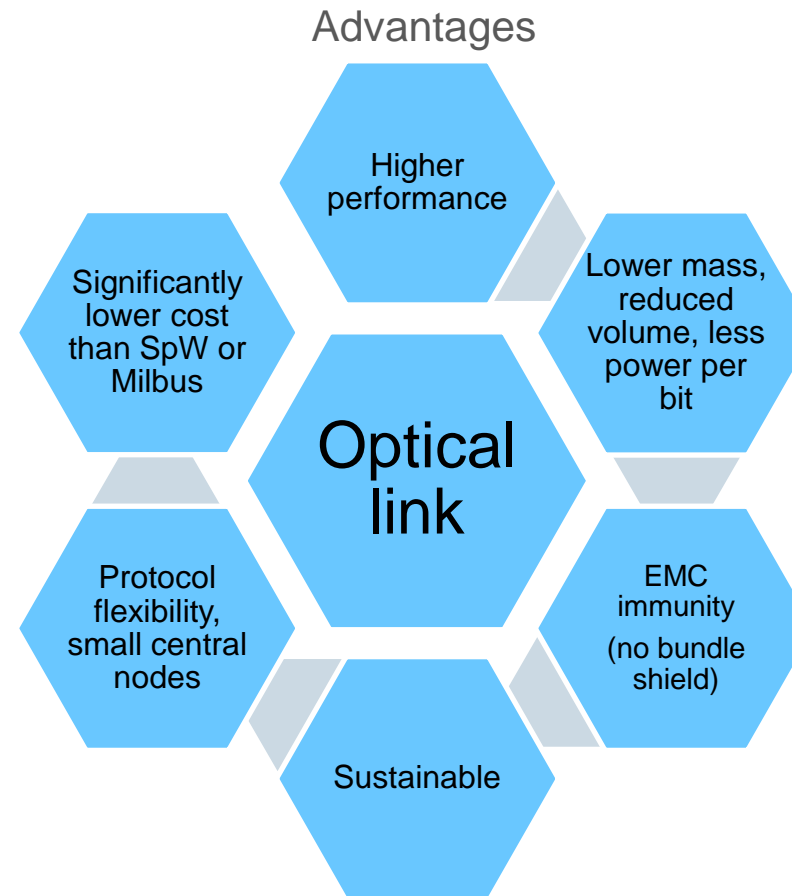
Digitalization supports harmonization, automation and product re-use

Exchangeability of data

Electrical Architecture and Harness Enhancements

Optical Links

- Optical link = Glass fibre with connector and transceiver
- Future data handling systems (also ADHA and APA) to include optical links as opportunity
- GSTP activity planned on optical links involving major primes and equipments
- Standardized approach to be envisaged for transceiver, connector, splitter, coupler, protocol
- Router could be in VHDL



Game changer for future space electrical architectures – for platform and payload

Electrical Architecture and Harness Enhancements Roadmap and Measures

Common European Reference Electrical
Architecture and its Building Blocks

Future Electrical Architecture

Standardization

- Fosters innovation, distributed developments and competition
- Standardized interfaces
- Standard optical link
- Standard protocols (SpF, Ethernet, ...)

Technologies

- Optical links (P/L, P/F)
- ADHA / APA develop.
- Communication topologies
- Modular
- Common hardware, software defined functions
- Harness optimization

Design

- Digital Design Process
- Design to consider complexity
- Visualization before built

ADHA / APA

- Transition from equipment to modules
- Modular
- Standardized frame / form factor and HW / SW interfaces
- Platform and payload

Electrical Architecture and Harness Enhancements

Benefits and Example

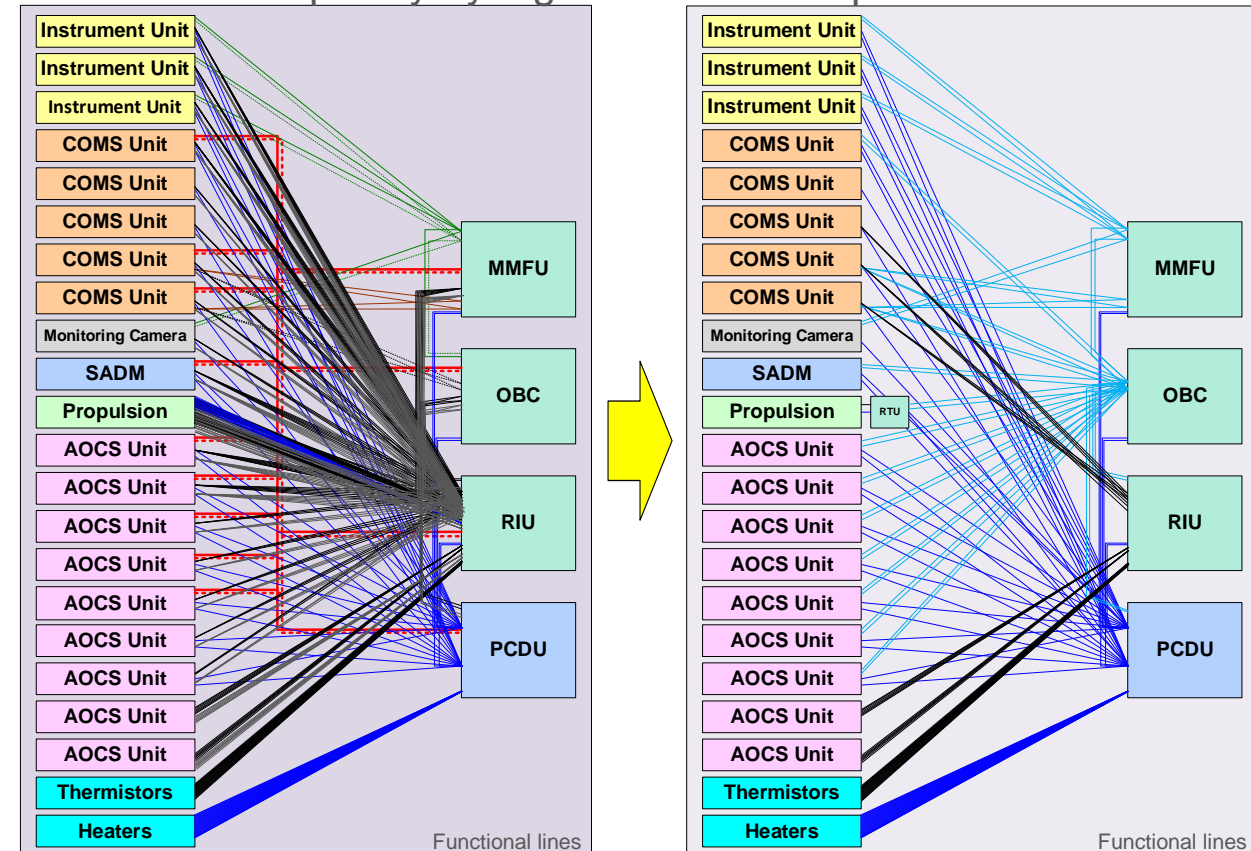
Significant reduction of interconnection complexity by digitalization and optical links

Obvious Benefits

- Design: Higher efficiency expected for automated design process for electrical architecture and harness
- Harness hardware: Reduced complexity with lower hardware cost, less integration / testing effort and repair

Hidden Benefits

- Mass and volume: Less PCB surface, housing surface, unit mass and volume, brackets mass
- EMC: Better bundle separation, less analysis, less ground loops
- Accommodation: Overall easier, less / smaller corridors, lower AIT cost
- Electrical: Less analysis and failure propagation, less I/F types
- Programmatic: Better overall schedule, reduced risk (less harness, errors and failure investigations), reduced interface data and handling effort on all levels, product re-use



Overall cost reduction is expected to be
at least 1%
of project cost

Thank you