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# The Application Software of the Ariel Instrument Control Unit

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(from M. Focardi's presentation)

# ARIEL Mission summary

- ✓ Selected (3/2018) and adopted (11/2020) as **M4 Mission of Cosmic Vision Prog**. by ESA
- ✓ AMC composed of more than 50 Institutes from 17 ESA Countries led by **RAL Space (UK)**
- ✓ Contributions from **NASA, JAXA and the Canadian Space Agency (CSA)**
- ✓ Science target: study and chemical characterisation of a sample (survey) of **exoplanets atmospheres** by means of primary and secondary eclipse (transit) spectroscopy and spectrophotometry in the VL and NIR bands (0.5-8 µm range)
- ✓ Single telescope of 1m class (M1)
- ✓ All aluminium mirrors (M1-M5)
- ✓ 3 DoF on secondary mirror (M2)
- ✓ Two Instruments: **AIRS** and **FGS** + an **ACS**
- ✓ Science data volume: 235 Gb/week
- ✓ PL PDR – successfully closed
- ✓ S/C PDR KoM on 5/10
- ✓ Prime Contractor: **AIRBUS** Defence and Space
- ✓ Launch scheduled in **2029** to L2

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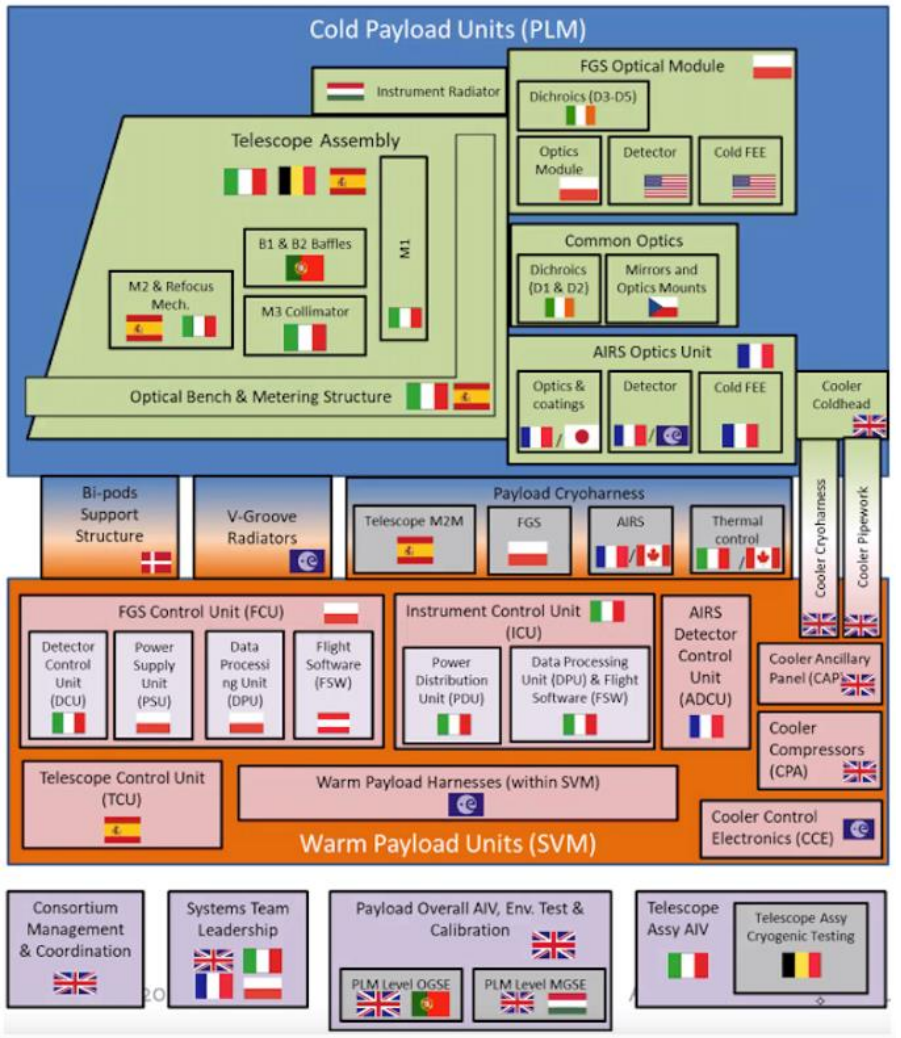
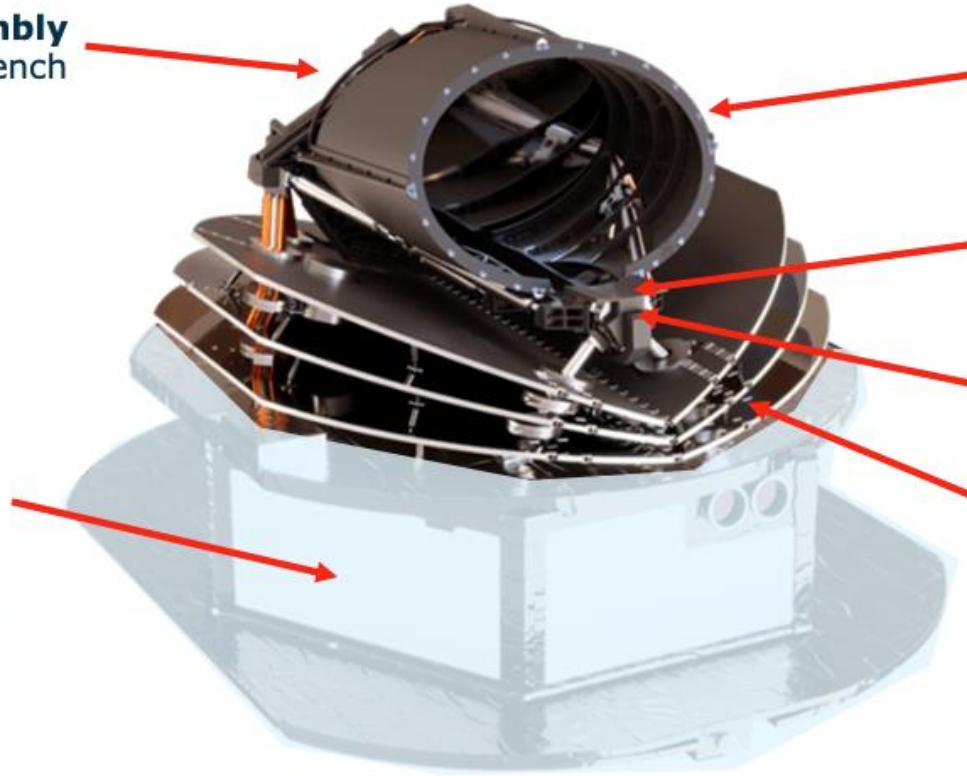


# ARIEL PLM and SVM



**Telescope Assembly**
Common Optical Bench

**Telescope Assembly**
M1 Baffle Tube

**Telescope Assembly**
M2 Baffle Plate

**Telescope Assembly**
M2 Mechanism

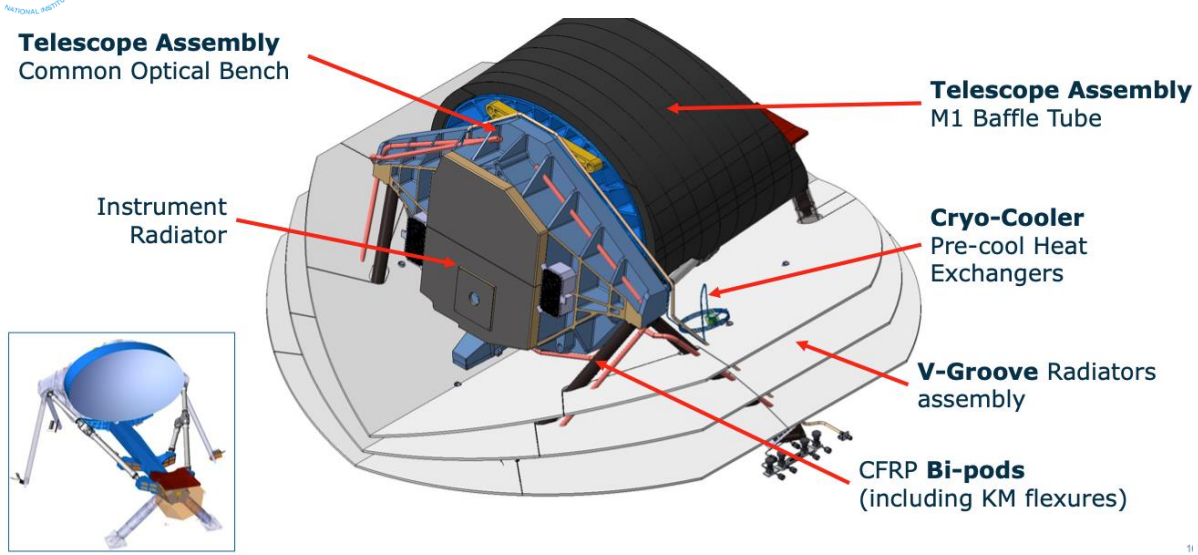
**V-Grooves**
Radiators assembly

**Spacecraft Service Module**
(nominal representation) containing:

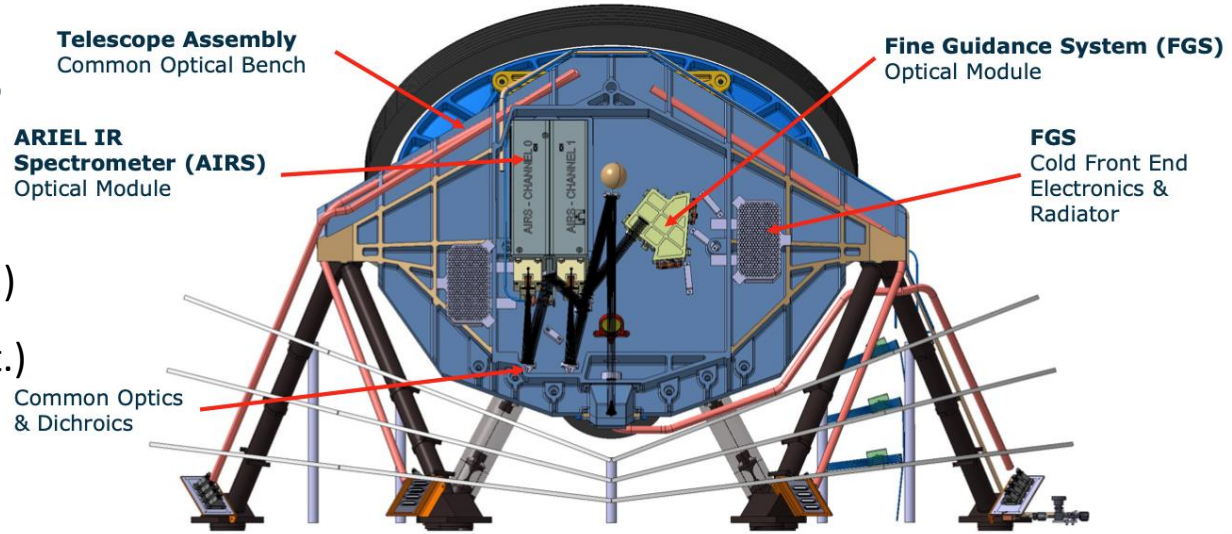
- Instrument Control Unit
- AIRS Detector Control Unit
- FGS Control Unit
- Telescope Control Unit
- Cooler Control Electronics
- Cooler Compressor Assembly
- Cooler Ancillary Panel

**Sun direction**

# ARIEL PLM – Payload Module

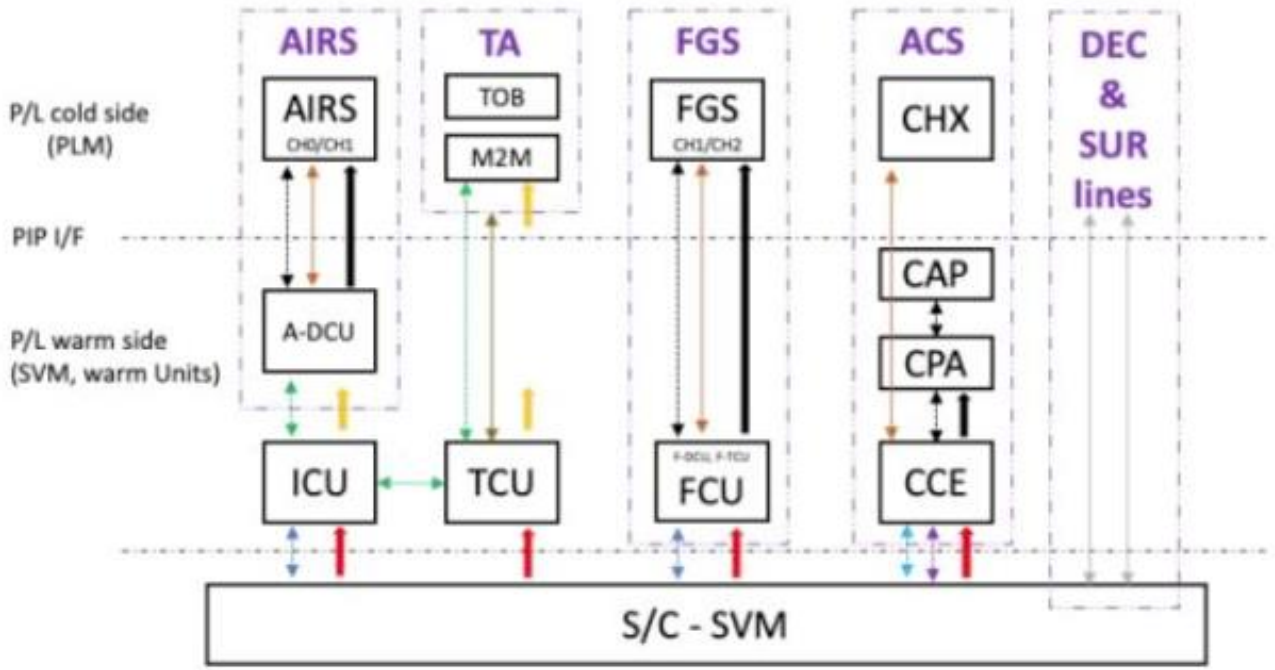



- ✓ Telescope Assembly (TA) operating @ 60 K
- ✓ Active Cooler System (ACS) including a Ne-based Joule-Thomson cooler
- ✓ AIRS detectors (HgCdTe) cooled down to 42 K
- ✓ FGS detectors (HgCdTe) operating close to 55 K




- ✓ **AIRS channels**:
  - I. Channel 0 (CH0) for the 1.95−3.90 µm band (low res. spect.)
  - II. Channel 1 (CH1) for the 3.90−7.80 µm range (low res. spect.)
- ✓ **FGS channels**:
  - I. low resolution NIR spectrometer for the 1.1-1.95 µm range
  - II. 3 photometric channels (2 used for guiding and science) between 0.5-1.1 µm

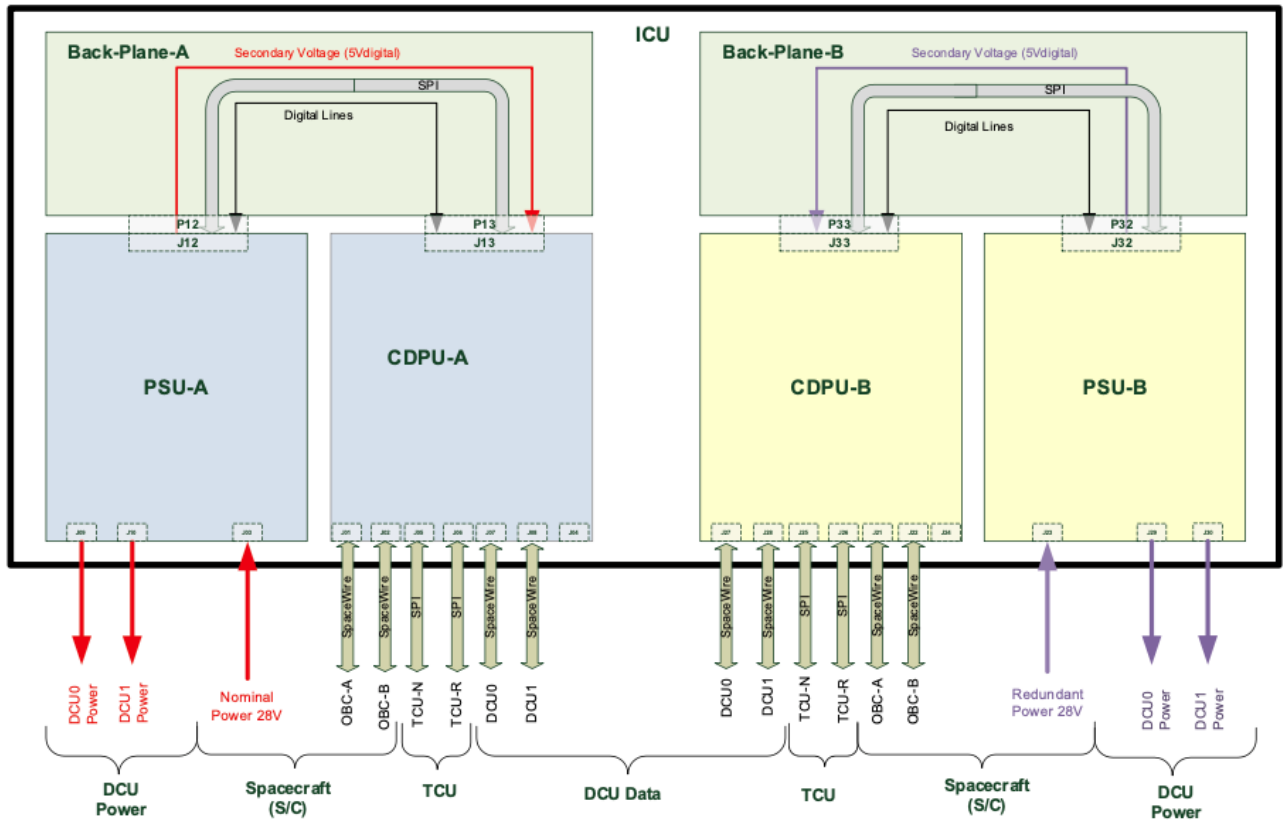
# ARIEL electronics architecture

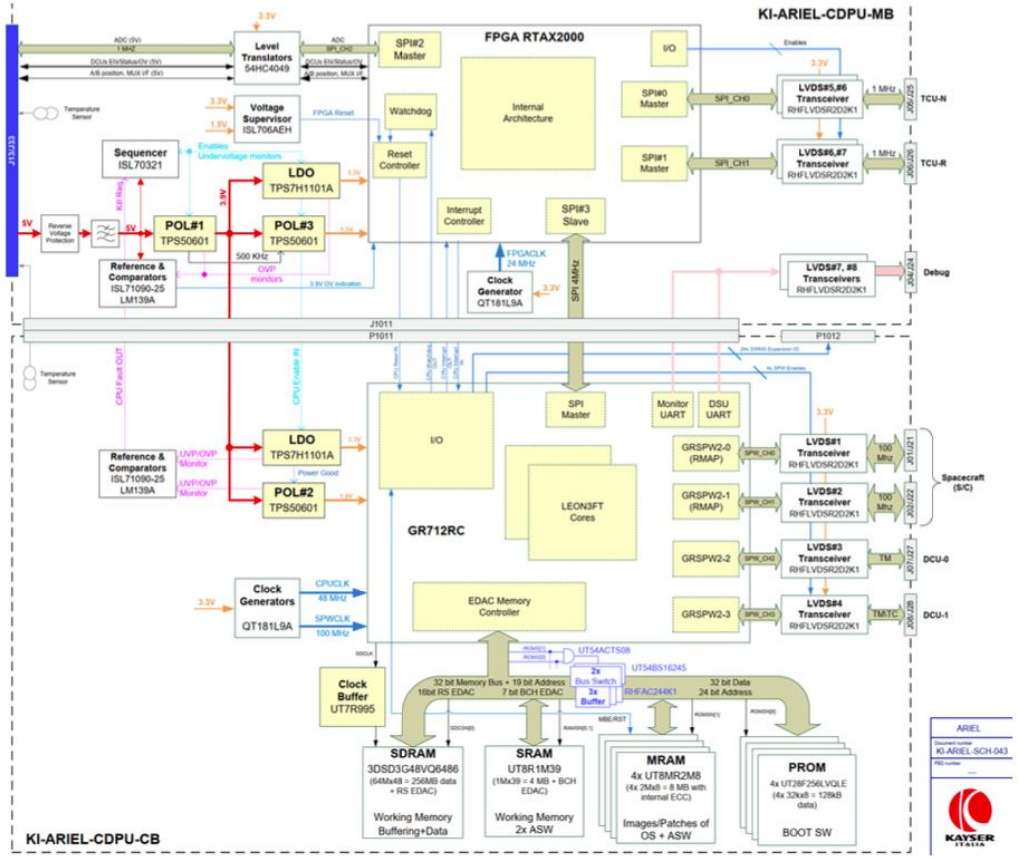



**Legend:**

- Primary Power lines (+28V)
- Secondary Power lines
- Instrument Secondary/Bias lines
- Primary TMTC I/F (Spacewire for ICU and FCU)
- Primary TMTC I/F (MIL-BUS-1553B for CCE)
- Secondary Data & Signals I/F
- Instrument Secondary Data & Signal I/F
- HPC/BSM and Launch Lock I/F
- DEC & SUR lines Thermal Control
- Thermal Control and Monitoring
- Thermal Monitoring

# AIRS ICU


ICU
Back-Plane-A
Secondary Voltage (5Vdigital)
SPI
Digital Lines
P12
J12
P13
J13
Back-Plane-B
Secondary Voltage (5Vdigital)
SPI
Digital Lines
P33
J33
P32
J32
PSU-A
CDPU-A
CDPU-B
PSU-B
SpaceWire
SPI
DCU0 Power
DCU1 Power
Nominal Power 28V
OBC-A
OBC-B
TCU-N
TCU-R
DCU0
DCU1
Redundant Power 28V
DCU Power
Spacecraft (S/C)
TCU
DCU Data
TCU
Spacecraft (S/C)
DCU Power


KI-ARIEL-CDPU-MB
FPGA RTAX2000
Level Translators 54HC4049
Voltage Supervisor ISL706AEH
Sequencer ISL70321
LDO TPS7H1101A
POL#1 TPS50601
POL#3 TPS50601
Reference & Comparators ISL71090-25 LM139A
Clock Generator QT181L9A
Watchdog
Reset Controller
Internal Architecture
Interrupt Controller
SPI#0 Master
SPI#1 Master
SPI#2 Master
SPI#3 Slave
LVDS#5,#6 Transceiver RHFLVDSR2D2K1
LVDS#6,#7 Transceiver RHFLVDSR2D2K1
LVDS#7, #8 Transceivers RHFLVDSR2D2K1
TCU-N
TCU-R
Debug
GR712RC
LEON3FT Cores
I/O
SPI Master
Monitor UART
DSU UART
GRSPW2-0 (RMAP)
GRSPW2-1 (RMAP)
GRSPW2-2
GRSPW2-3
LVDS#1 Transceiver
LVDS#2 Transceiver
LVDS#3 Transceiver
LVDS#4 Transceiver
Spacecraft (S/C)
DCU-0
DCU-1
LDO TPS7H1101A
POL#2 TPS50601
Clock Generators QT181L9A
Clock Buffer UT7R995
EDAC Memory Controller
SDRAM 3DSD3G48VQ6486
Working Memory Buffering+Data
SRAM UT8R1M39
Working Memory 2x ASW
MRAM 4x UT8MR2M8
Images/Patches of OS + ASW
PROM
BOOT SW
KI-ARIEL-CDPU-CB

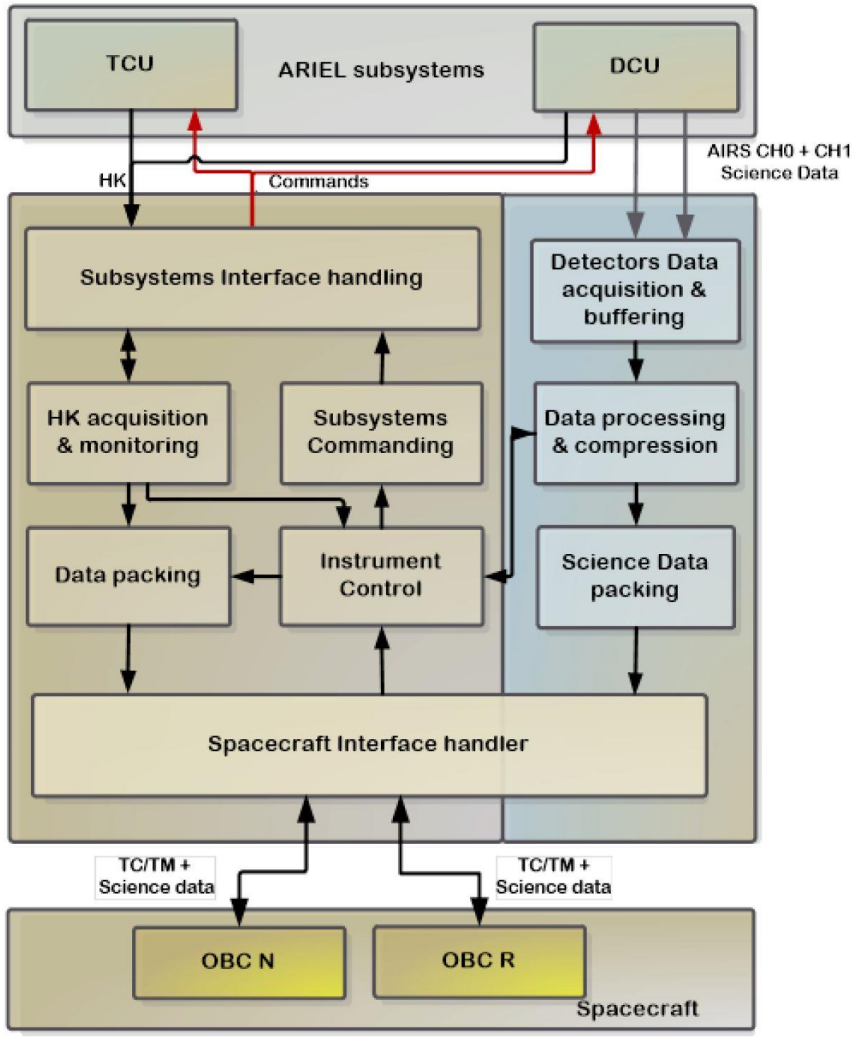
# Ariel ICU SW

- The SW onboard the ARIEL ICU has two components: the ICU Boot SW (BSW), i.e. the start-up application resident in PROM, which is non-patchable; and the Application SW, i.e. the instrument control and data processing SW, stored in a Non Volatile Memory and patchable.

- Boot SW and HW dependent SW (i.e. all SW drivers to handle HW components) are strictly related to the ICU HW. Their development is part of the activities included in the industrial contract for the ICU provision.
- Kayser Italia is providing all models of the ICU HW, as well as the Boot SW and the Board Support Package
- INAF will provide the Ariel Application SW

# ASW concept

- The ASW will be based on the RTEMS operating system; we will use the RTEMS SMP version, since we plan to use the SW in Symmetric Multiprocessing (SMP) mode
- The ASW code (in particular for the standard services) will be mostly based on our team expertise gained in the Euclid and Plato missions
- Our team is also responsible for the ASW of the Instrument Control Unit for the X-IFU instrument of the Athena mission
- The ICU is controlling the DCU detectors; it collects, compresses and packetizes the DCU data
- Some limited data processing is foreseen; in addition to windowed mode also full frame (1024x1024 px$^2$) is needed, mostly for on-ground testing
- The ICU is also controlling and monitoring the TCU



# PUS C implementation

TC and TM packets will be based on the ECSS PUS protocol, Issue C
The standard services implemented are shown in the table and the subservices implemented allow great operational flexibility.

The definition of the Ariel private services have still to be finalized
The private services will cover TCU commanding and DCU configuration, operations and FDIR functions, as well as management of internal ICU functions

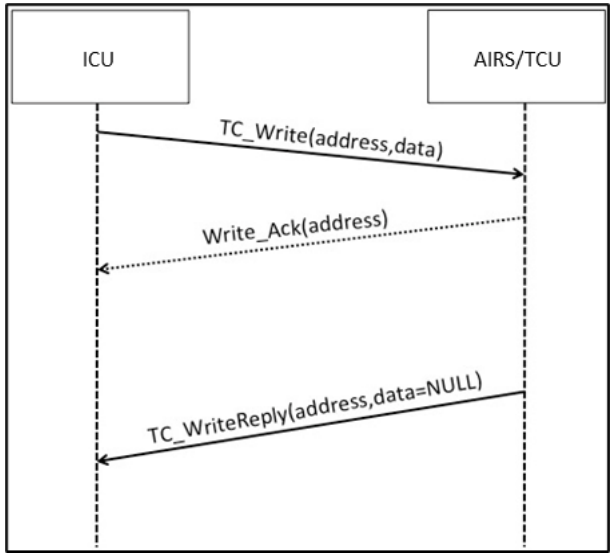
The use of On-Board Control Procedures is up to now considered not necessary

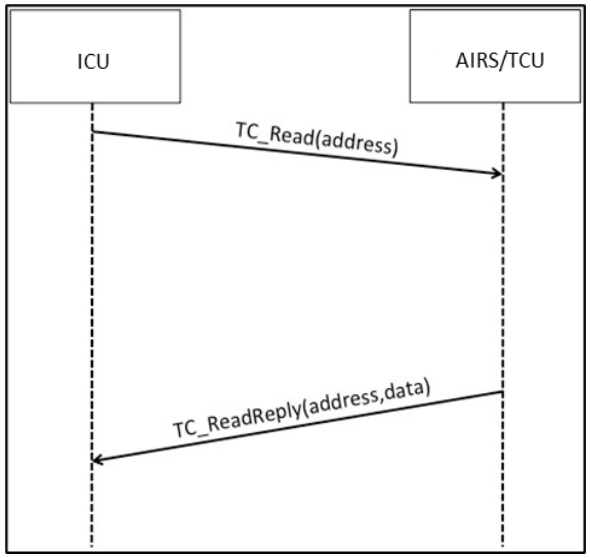
| PUS Services | Description |
|---|---|
| 1 | Telecommand verification |
| 3 | Housekeeping and Diagnostics |
| 5 | Event Reporting |
| 6 | Memory Management |
| 9 | Time Management |
| 12 | On-board Parameter Monitoring |
| 17 | Connection Test |
| 20 | On-board Parameter Management |

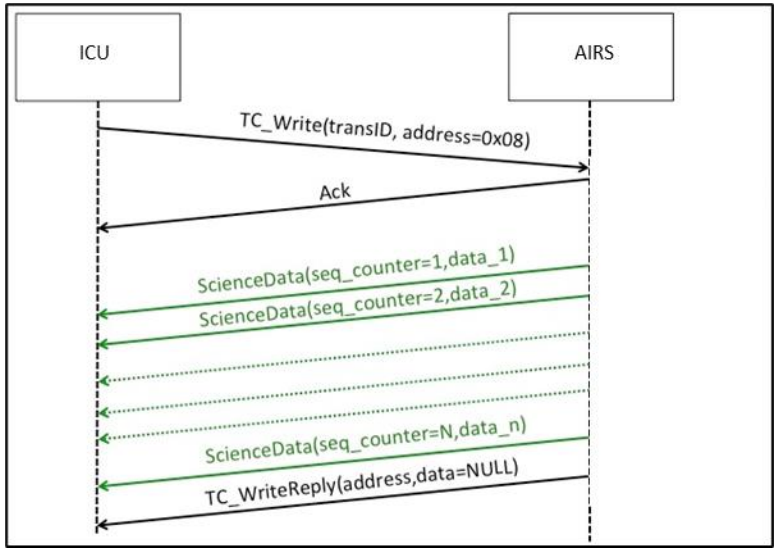
# Communication protocols

The ICU is connected to the DCUs via Spacewire links, and to the TCU and PSU via SPI links.

The higher level protocol for internal communications with TCU and DCUs is based on a Master-Slave approach and is derived from the RMAP protocol. A similar approach has been adopted also in the PLATO mission. An acknowledge of the write command can be requested, while read commands have only the TC  ReadReply packet with the requested data. The TC to go in SCIENCE mode will cause the production of the N data packets expected, followed by a WriteReply packet.



# TC TM packets

## General Read/Write packets

| Byte 0 | Byte 1 | Byte 2 | Byte 3 |
|---|---|---|---|
| **Destination Address** | Protocol ID (0x03) | Source Logical Address | PaketType, Ack, Err |
| **Transaction ID** | | Data Length | |
| **Command Id\|Address** | Transaction Sequence Counter | | |
| **Cargo** | | | |
| **Footer** | | | |

## AIRS Science data packets

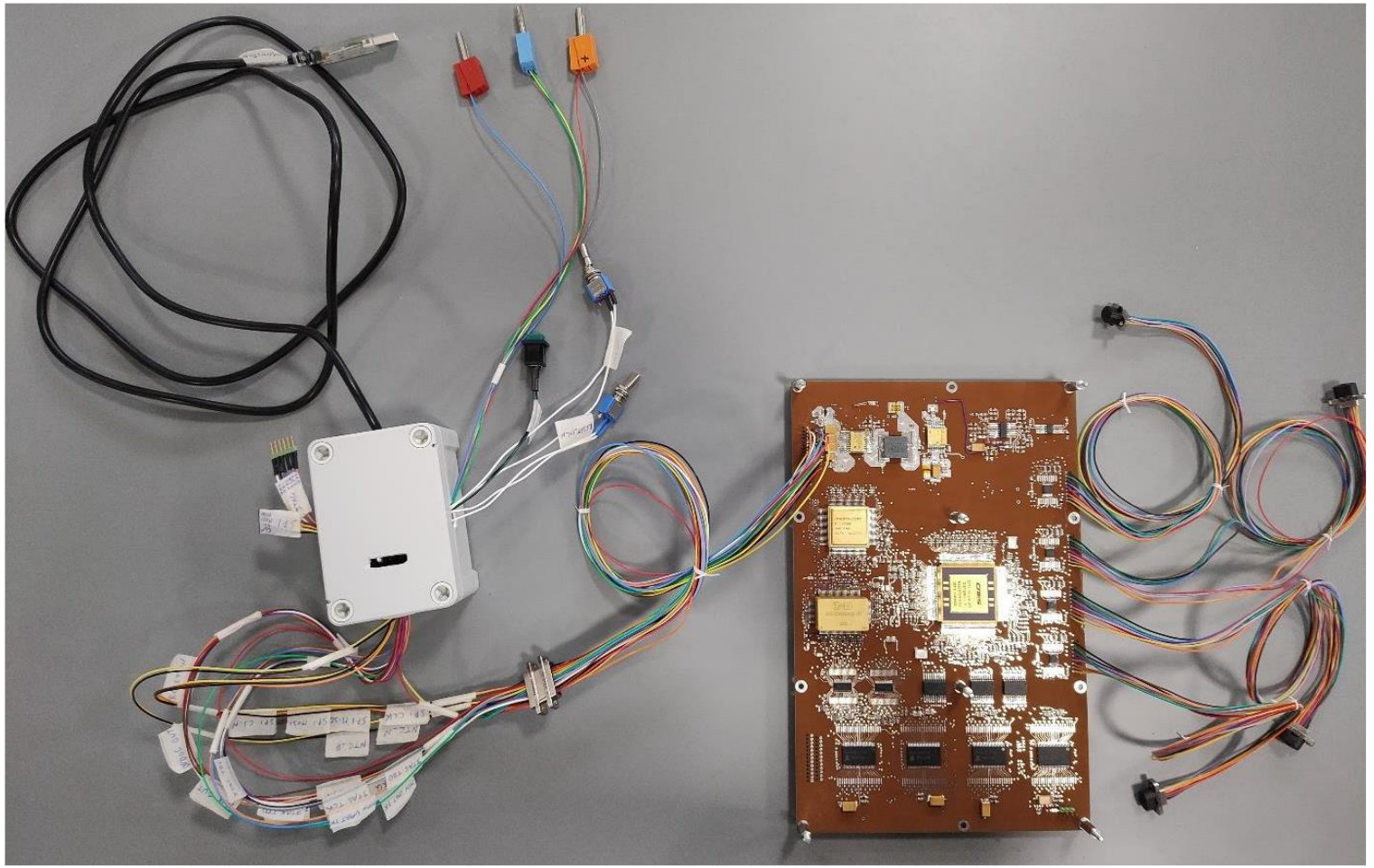
| Byte 0 | Byte 1 | Byte 2 | Byte 3 |
|---|---|---|---|
| **Destination Addr** | Protocol ID | Source Address | 0xC0 |
| **Transaction ID** | | Data Length | |
| **Address/Cmd ID (0x08)** | | Sequence Counter | |
| **Science data** | | | |
| **CRC-16 MSB** | CRC-16 LSB | EOP | |

# Development strategy

- In order to speed up the development of the ASW we started the development activities during 2023 using a development board GR712RC already available at our institution; recently (end of September, 2023) a more representative board has been provided by our industrial partner (Kayser Italia) together with a first version of the low-level software, and our prototype ASW will now be ported to this HW; all the SW components will be tested in an incremental cycle on the available HW.
- In parallel to the normal review cycle, we will prepare prototype SW versions to allow early testing of the ICU-DCU communications as well as ICU-TCU and ICU-SC communications, using simulators that should be available at the end of 2023
- Currently SW PDR is foreseen by Q1 2024 and the prototype SW will be ready in the same time frame

# CDPU EM board

The ICU CDPU EM board with a setup for running laboratory tests has been delivered to INAF by Kayser Italia at the end of September 2023, to start ASW development and tests on the target HW.
Currently only the Spacewire connections can be operated; the SPI module will be delivered in the coming weeks.
Currently we are integrating the Kayser BSP with RTEMS SMP



# Qualification

- As already mentioned, the RTEMS version used is the one provided by ESA in the RTEMS SMP Qualification Datapack (https://rtems-qual.io.esa.int/) which is a tailored version of RTEMS together with a suite of qualification tests.
- The qualification test suite will be run on the target HW to ensure that it is adequate to run RTEMS SMP; INAF will be in charge of performing these tests and, if necessary, will request the support from Kayser Italia
- Additional specific features not included in the pre-qualified profile (in particular drivers) will be tested and qualified by INAF with Kayser Italia support
- A full set of qualification tests will be developed in parallel to the ASW covering all nominal operations plus anomalies injected by our subsystem simulators

# Unit tests and continuous integration

- We plan to use Ceedling in order to perform unit tests on all functions.
- The code versioning will be made in a Gitlab environment; we plan to implement a continuos integration system in order to allow, at every commit, to produce all the artifacts foreseen as well as to run all the test producing the related test reports
- Bugs and issues will be also managed on the Gitlab server
- A similar environment has been used during the development of the ASW for the Euclid NISP ICU and is currently available for the Euclid post-launch maintenance activities

Thank you!