Olympe: a NG-Ultra based processing board demonstrator ESA EDHPC October 5 2023

DEFENCE AND SPACE

Matthieu NOUARD



Space Electronics key figures & facts









450 France workforce

> 1200 boards /y > 150 unit /y **150 M€**Revenues
40% export







size companies



Agencies



Satellite Operators

Governments, institutional and enterprises from multiple areas/ fields





> 60 M€ Export
Order Intake in 2022

Spacecraft Electronic Unit Supplier



Elancourt

Toulouse

Our Ambition



Be worldwide Electronics and Sensors / Actuators reference for Space



Master New Space & Conventional Space solutions from design and technologies, up to manufacturing & test processes



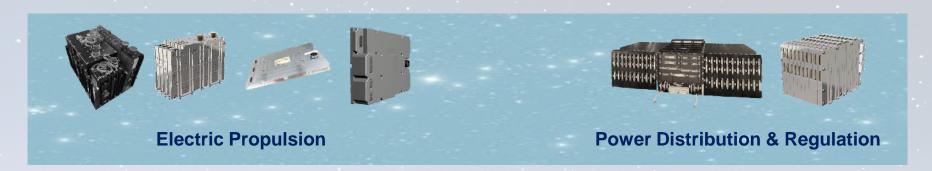
Pioneer and qualify space technologies for future spacecrafts, launchers & space systems



Be attractive for talents by offering key competences acquisition and efficient collective knowledge management



Space Electronics reliable & large unit portfolio



Power & Propulsion Units



Platform & Payload Processing Units



Sensors & Actuators

www.airbus.com/en/products-services/space/equipment

Introduction

General Support Technology Programme

From innovation to engineering steps towards future mission adoption

Main objectives

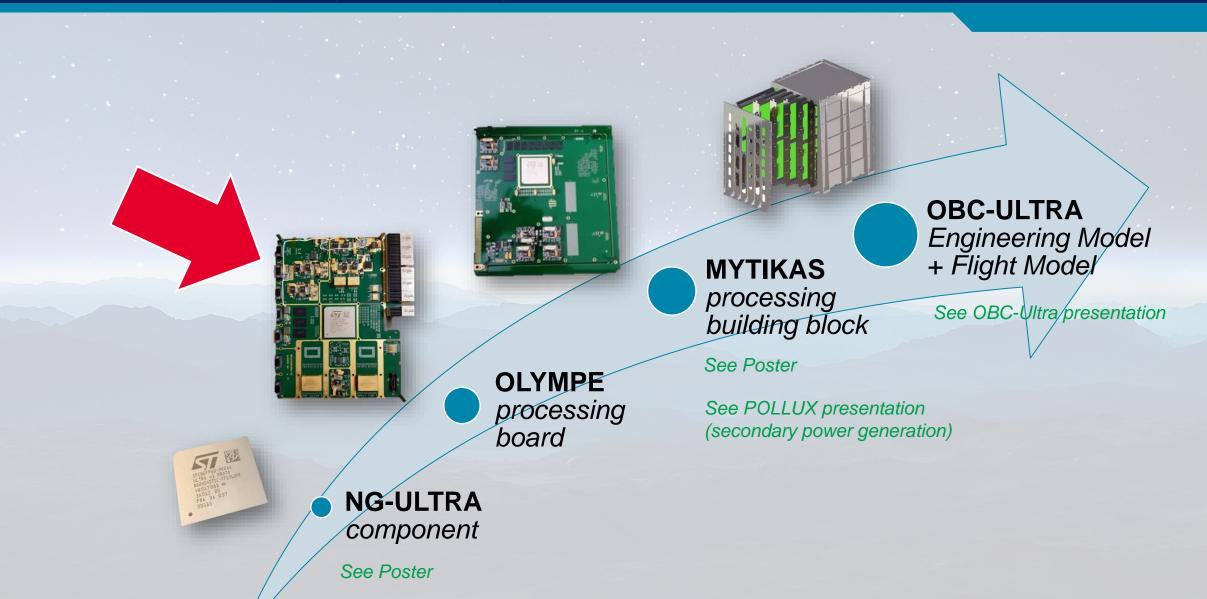
- ➤ High-speed links demonstration
- ➤ High data rate access to DDR and Flash NAND memories through FPGA
- ➤ PS/PL interface performance
- ➤ Multi-core application compatibility
- ➤ Typical platform application

Perspectives

- ➤ OBC-Ultra: NG-Ultra based On-Board Computer
- ➤ Mass Memory equipment
- ➤ Instrument Control Unit



An 8-year journey from chip to On Board Computer



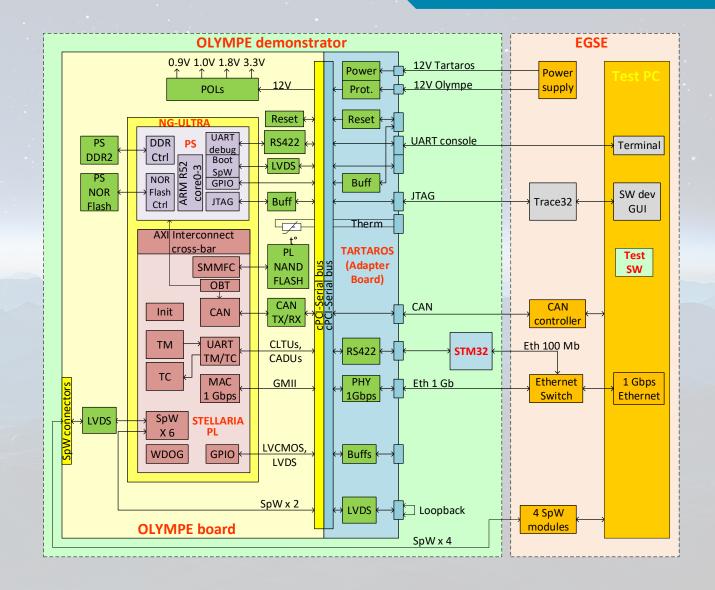
Functional description

Demonstrator boards:

- **≻Olympe board:**
 - NG-Ultra-based processing board
- >Tartaros board:
 - Backpane board

EGSE (Electrical Ground Support Equipment):

- ▶PC with STM32-based board
- Send or receive data from the different interfaces following the demo phase
- ➤ Displays the data rate



Olympe board



Memory:

- 1 GB DDR2
- 16GB Flash NOR: Bootloader, bitstream and ASW storage
- 32 GB Flash NAND: processed data storage

Communication interfaces:

- 6x SPW (100 Mbps)
- cPCI-serial connector

ADHA cPCI-serial connector:

- Power supply
- 2 x CAN (1 Mbps)
- 1 x Ethernet (1 Gbps)



Demonstration steps

Demonstration principles

- EGSE sends TCs to the Olympe demonstrator
- Olympe initiates a demonstration phase with specific actions:
 - Data reception from EGSE on multiple links (SPW, Ethernet and CAN)
 - Data processing
 - Internal operation (Flash NAND storage, PS/PL communications)
 - Data sending to EGSE
- EGSE displays the phase and the Olympe system behaviour all along the demonstration phases:
 - Link data rate
 - HouseKeeping TM
 - Received images



EGSE HMI



Phase description

Interface data rate informations

Demonstration

phase

Processing

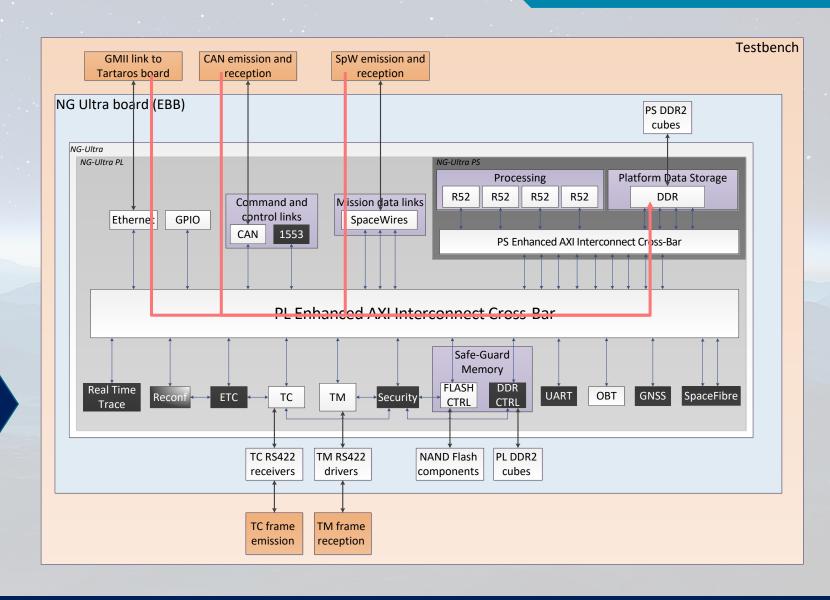
cores status

Description

- Data sent to Olympe via:
 - 6 x 100 Mbps SPW links
 - 1 x 1 Gbps Ethernet link
 - 1 x 1 Mbps CAN link
- DDR2 storage

Focus:

- **High-speed links**
- DDR2 access from FPGA at a high data rate





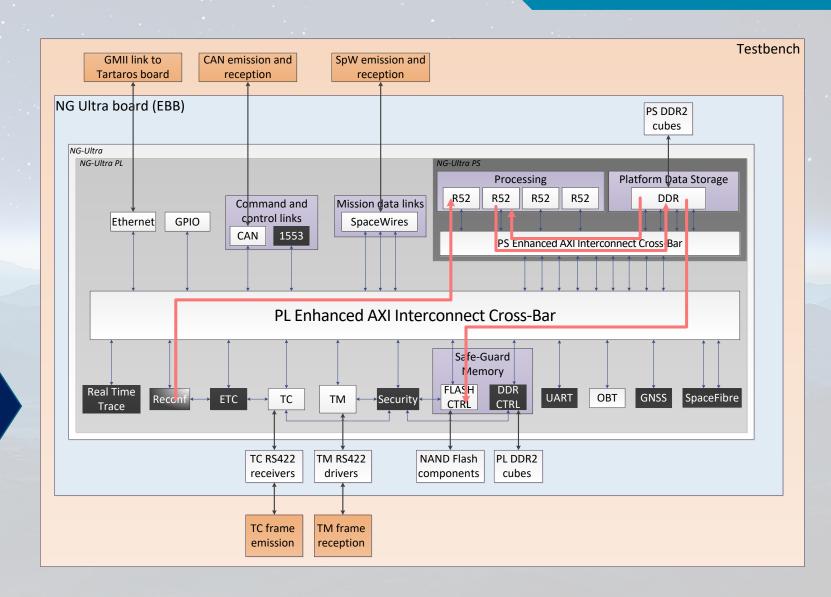
October 5th 2023

Description

- ASW operations:
 - Reading data in DDR2
 - Processing data
 - Writing back data in DDR2
 - Writing a part of the data in Flash NAND

Focus

- DDR2 access from ASW
- Flash NAND writing from **ASW**

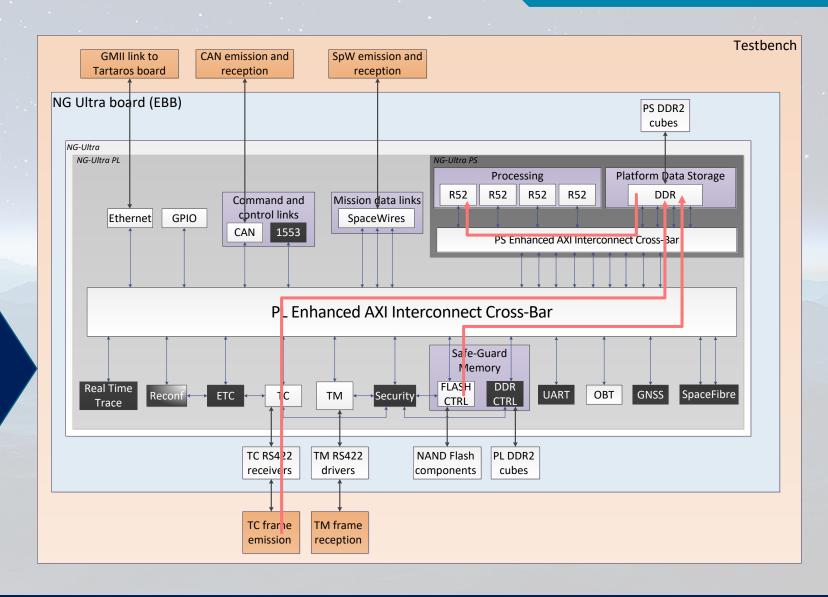


Description

- ASW operations:
 - Flash NAND data retrieving
 - TM sending programmation
 - Previously received data

Focus

- **Platform application** (TM/TC) on one core
- Interface handled on other cores
- Flash NAND reading from **ASW**

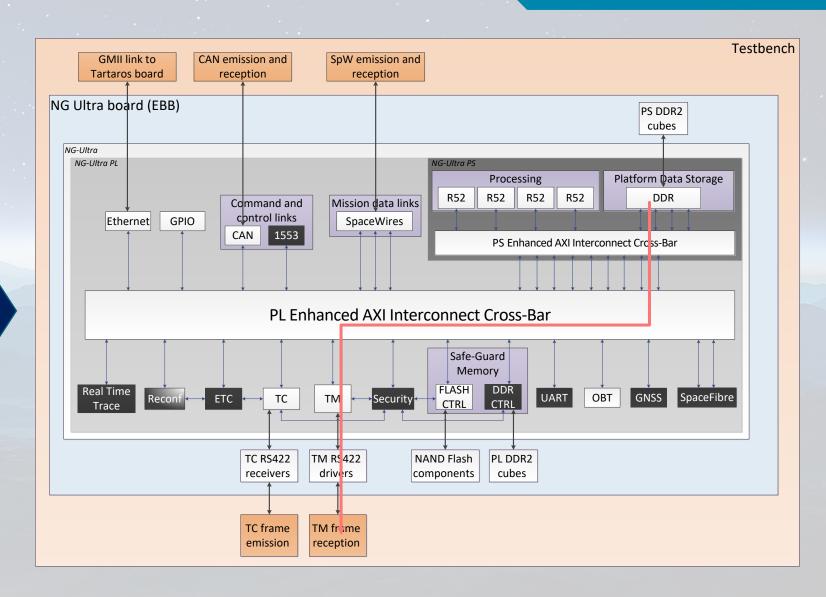


Description

- TM sending data back to EGSE
- Watchdog expiration alarm TM

Focus

- **High speed communication** between PS and PL part
- **TM** transmission

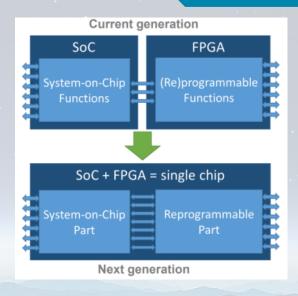


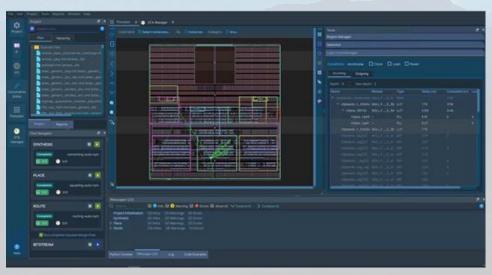
HW design keypoints

- NG-Ultra report
- Re-usable block designs
- NG-Ultra within an electronic design

FPGA design keypoints

- SoC + FPGA
- **HW/SW** architecture
 - Shared DDR access between PL and PS part
 - PL interconnect design
 - Interrupt management
- **Airbus / NanoXplore collaboration**
 - Impulse: NX tool for FPGA design
 - Synthesis, place and route
 - Consolidation
 - **Dedicated features**
- **Airbus benefits**
 - FPGA fabric design comprehension
 - Filling rate and frequency improvement
 - Specific workflow





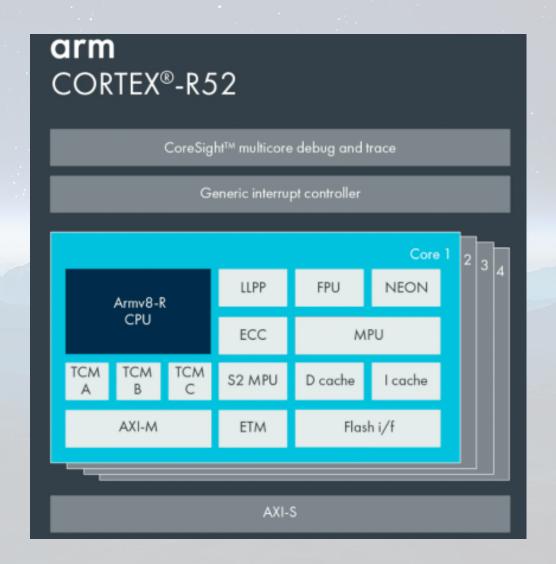
SW design keypoints

ASW execution environment

- 4 ARM Cortex-R52 cores
- DDR2

Used ARM specific functionalities

- Tightly Coupled Memory (TCM)
- Data and Instruction cache
- Memory Protection Unit (MPU)
- General Interrupt Controller (GIC)
- Coresight debug and trace



SW design keypoints

Drivers

- NanoXplore SDK
 - Main elements of the NG-Ultra PS part
 - DDR controller for DDR2 and DDR4 usage
- Olympe specific drivers
 - MMFC, OBT, Reconf, Ethernet, Spw, ...

Bootloaders

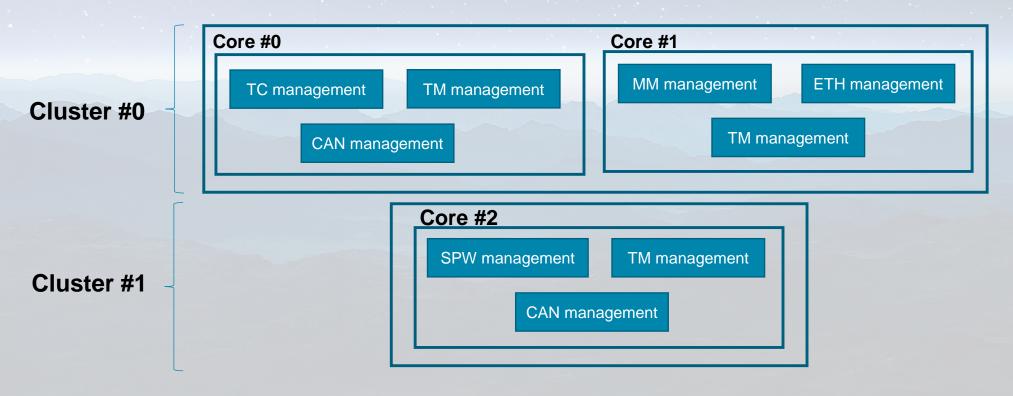
- BL0
 - Load and start BL1 execution
- BL1
 - DAHLIA design and development
 - Load and start ASW execution in DDR memory



SW design

RTEMS

- Open source RTOS
- Multi-tasking and IPC features
- Used on current Airbus equipment units (OBC, MM, ...)
- Support of NG-Ultra multi-core (AMP)



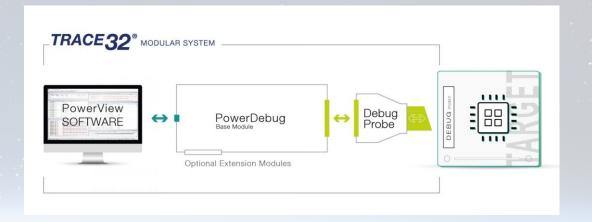
SW debugging

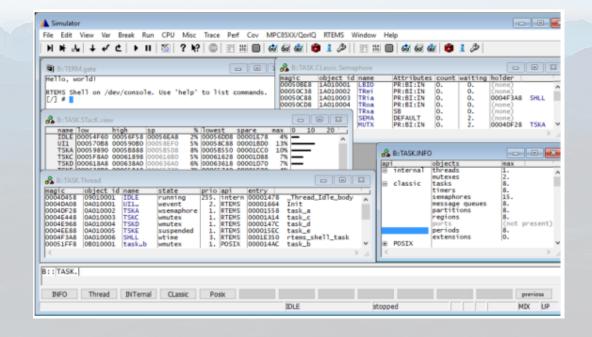
Lauterbach debugging probe

- **Relies on ARM Coresight** debug and trace features
- **Trace32 Software:**
 - Basic debug features
 - Scripting language
 - NG-Ultra support
 - RTEMS support
 - Parallel and serial trace

Main tool through different steps:

- **FPGA** integration
- **Drivers integration**
- Multi-task ASW debugging
- **Multi-core ASW debugging**



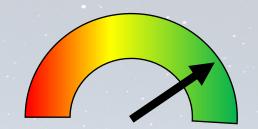




Performance

OSCAR MK4

- Current Airbus OBC generation
- Based on a SCOC3 SoC
- Used in more than 15 LEO satellites



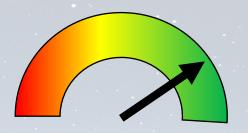
Data-rate link comparison:

Link	OSCAR MK4	OLYMPE	Comments
TC	64 kbps	10 Mbps	
TM	5 Mbps	10 Mbps	Total data rate
SPW	64 Mbps (x7)	64 Mbps (x6)	
CAN	N/A	1 Mbps	Total data rate
Ethernet	N/A	200 Mbps (theoretical)	TFTP protocol
1553	700 kbps	N/A	

Performance

Olympe

- Improved TM/TC data rate
- Similar data rate on multiple SPW links
- New interfaces implementation:
 - 1 Mbps CAN
 - 200 Mbps Ethernet
- PL filling rate: 40 %
 - Possibility for other IP implementation/integration



Conclusion

- Harnessing NG-Ultra environment on multiple topics
 - Electronic design, FPGA and SW part
- Running a typical application platform on a NG-Ultra based system
 - TM/TC
 - High-speed link: SPW (x6), Ethernet, CAN
 - Data processing
- Strategic building blocks for upcoming Airbus product line
 - OBC-Ultra
 - Mass Memory
 - ICU



Thank you

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