Time Sensitive Networking (TSN) as reliable communication bus for micro-launchers

INNOVATING SOLUTIONS

Introduction - What is TSN?

Time Sensitive Networking - TSN

Time Sensitive Networking (TSN) is a set of standards developed by the Time-Sensitive Networking task group of **the IEEE 802.1** working group. These standards define mechanisms for the time-sensitive transmission of data over **deterministic Ethernet** Networks.

Introduction - Advantages

- ✓ High performance
- ✓ Determinism
- ✓ Flexibility
- ✓ Enables Hard real time constraints
- ✓ Fault Tolerant
- ✓ Precise Time Synchronization (few nanoseconds)
- ✓ Extension of the widely used IEEE 802 Medium Access Control (MAC)
- ✓ Enables Mixed criticality data on a single harness
- ✓ Up to 100 m physical layer length at 100 Mbps
- ✓ Open standard - Compatibility – No vendor lock

Introduction - Data Classification in a Spacecraft Modular Avionic System

Critical Data – Priority 1

Real time needs
Up to Catastrophic consequences

HIGH PRIORITY

Essential Data – Priority 2

No Real time needs
Up to major consequences

ESSENTIAL

Best Effort Data – Priority 3

No real time needs
Minor or negligible consequences

BEST EFFORT

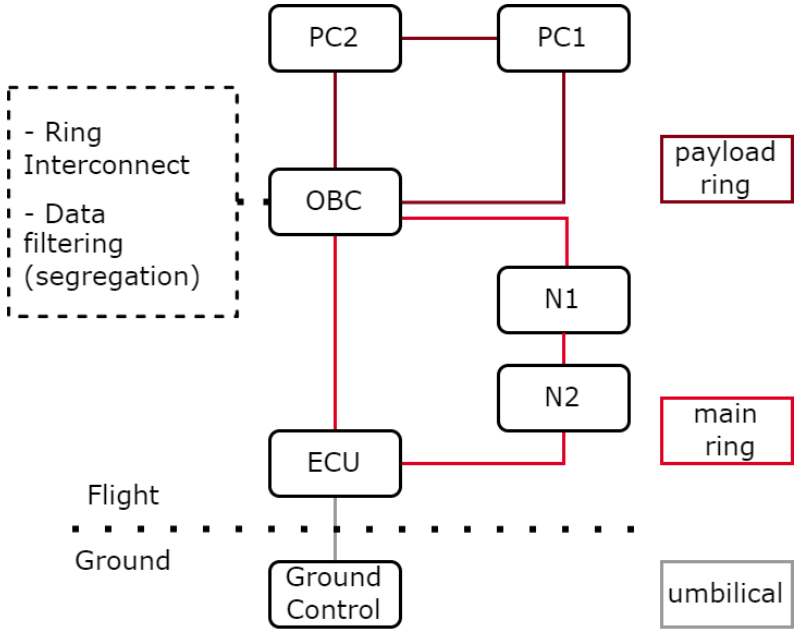
MIURA-1 Use Case

PLD Suborbital launch vehicle

- Single Stage
- Liquid oxygen and kerosene
- Thrust Vector control and ARCS

Avionic System

- Six processing nodes
- Two daisy chains
- Ground connection to **National Instruments** equipment
- Interfaces: TSN, CAN, Sensors, RS422, GPIOs, Ethernet



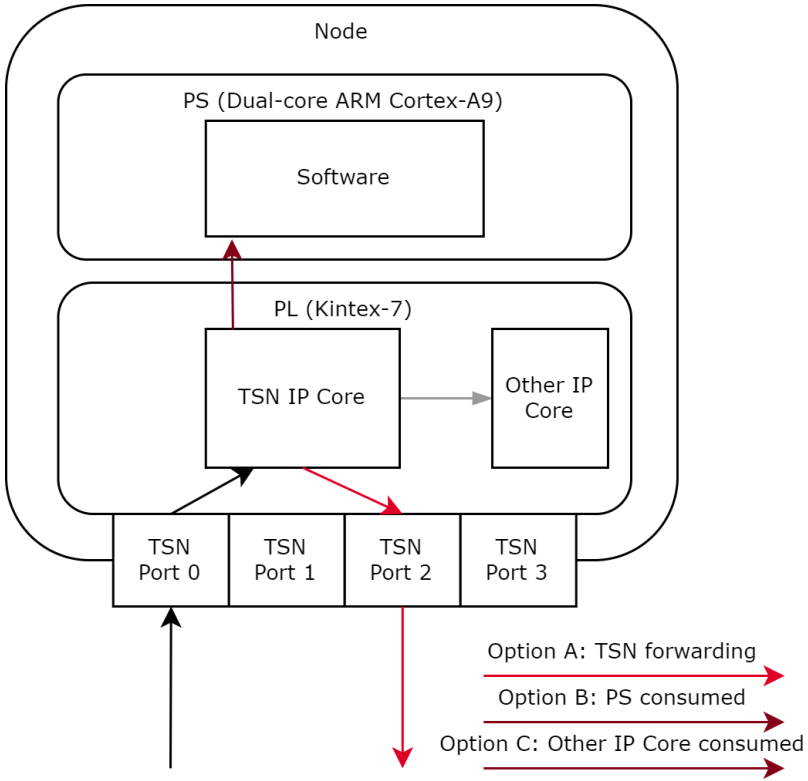
Standard Subset

Selected

- **IEEE 802.1AS** gPTP synchronization (including Best Master Clock selection BMC)
- **IEEE 802.1Qbv** Enhancements for Scheduled traffic – Time Aware Traffic Shaping
- **IEEE 802.1Qbu & IEEE 802.3br** Frame preemption and Interspersing Express Traffic

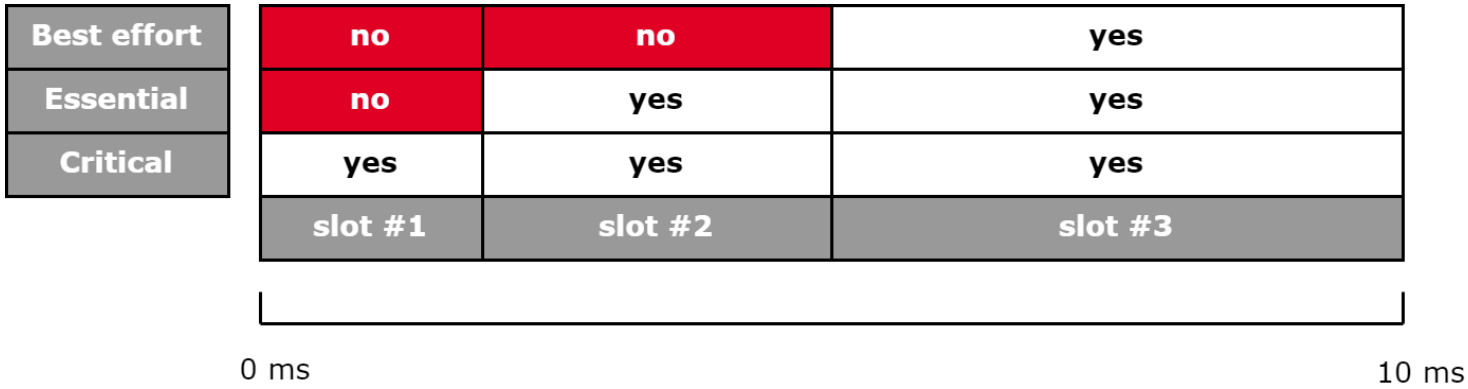
Topology

- **Flexible** packet management based on configurable rules
- No software intervention to forward packets to **reduce the CPU usage**
- **Redundancy** management based on CRC (Paired ports)



TSN Configuration

- **Flexible** configuration established at initialization time
- Data traffic **worst case analysis** needed to obtain the configuration



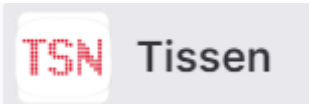
TSN Configuration

Problem

- Configuration can be complex, i.e a dedicated VLAN needs to be defined per each destination ID and data priority.
- Every node need to know what to do with each VLAN.
- I.e, MIURA 1 TSN configuration file has around 1500 lines

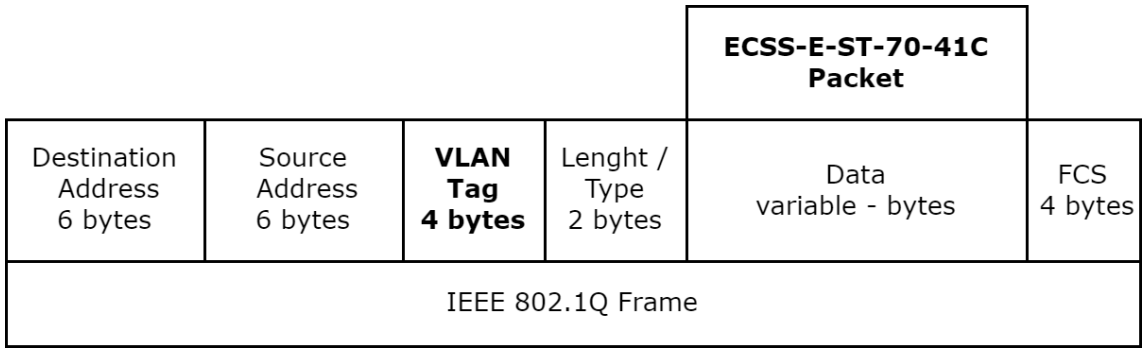
Solution - Tissen

- A dedicated tool has been created to support the TSN configuration.
- It automatically generates the configuration file based on the network topology and the data traffic definitions.



PUS over TSN

- Minimize overhead
- Reuse on-board and ground software
- Configurable translation from APID to address similar to IP routing tables

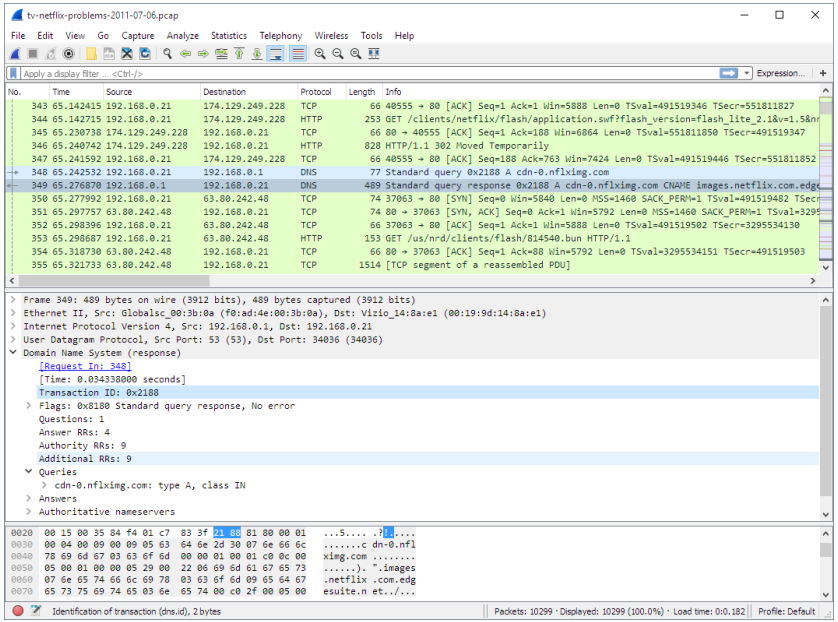


Testing and Qualification

Debug and troubleshooting

- Quick and efficient debug thanks to mature ethernet COTS tools
  - **Wireshark**
  - **Zero delay sniffers**

- Base ethernet protocol is well known by engineers (smooth learning curve)



Testing and Qualification

Integration Test – Development and EM boards

- Software ECCS Criticality B

Validation Tests – Avionic Qualification model

- **Environmental**
  - Vibration and shock
  - Thermal
  - Vacuum
  - EMC
- **Avionic Test Bench (ATB)**
  - Full Mission
  - Mission scenarios
  - Contingencies

System Tests – Avionic Integrated in the Micro-launcher

Testing and Qualification

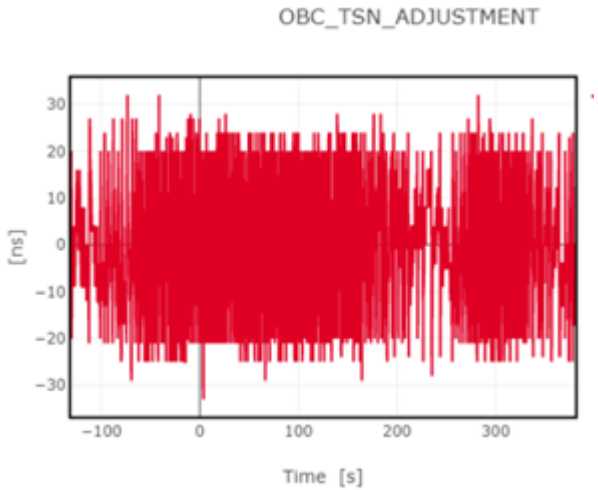
Commnication architecture performances

Data rates MIURA1 use case

- 0.5 Mbps of critical data
- 2 Mbps of essential data
- 1 Mbps of best effort data

Results – Including avionic qualification, flight model tests and launch attempts.

- No packet lost
- No synchronization lost
- No real time constraint violated
- Clock adjustment under 60 ns
- Link delay under 500 ns



Portability

Software driver available for:

RTEMS 5.0 → Bare Metal → AIR Hypervisor

Easy porting to other RTOS / Hypervisor

Resources

FPGA

- **<60%** LUTs, **<40%** Slice registers, **<55%** BRAMs, **<15%** DSPs – **4 port** implementation in a **Xilinx Zynq 7030**

FPGA RESOURCES NEEDED FOR THE TSN IMPLEMENTATION.

TSN Conf.	LUTs	Slice Reg.	Multiplexers	BRAMs	DSPs
4 TSN Ports	46408	62587	566	136.5	50
2 TSN Ports	34649	48643	313	88.5	42

Processor

- Around **10%** in a single core ARM Cortex A-9

MIURA 1 Status

At the moment of preparing this presentation …

- System qualification completed including hot tests
- Two launch attempts:
  - **31/05/2023** Abort due to altitude winds
  - **17/06/2023** Abort due to anomaly detected in the umbilical release
- Next attempt foreseen in autumn 2023

Conclusion

- A novel **communication architecture** for modular spacecraft avionic system has been design, implemented, and **qualified** for flight within the MIURA 1 micro-launcher.
- The results indicate the communication architecture can exceedingly fulfill the needs of a launcher.
- The communication architecture is very **flexible** and can be instantiated in reduced boards.
- The communication architecture is **portable**, software driver available for RTEMS, AIR hypervisor and bare-metal.

Thank you

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