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A heterogeneous simulation platform with LEON5 and IEEE standard real-time operating system

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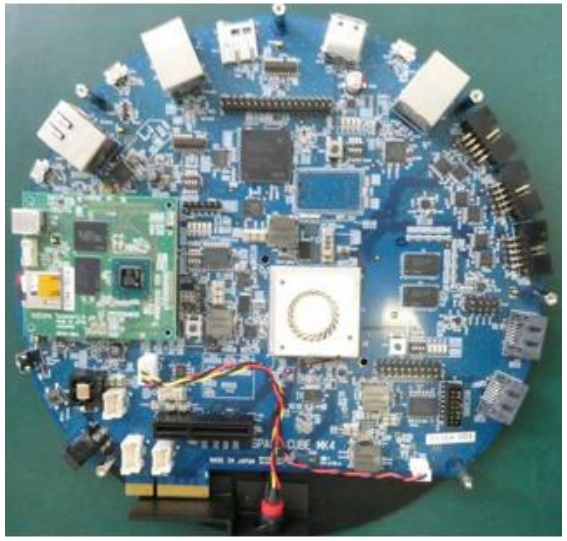
Contents

1. Introduction
2. DESTINY+
   - The first application of MBD with Space Cube® mk4
3. Space Cube® mk4
   - Heterogeneous processing edge node
4. IEEE 2050-2018
   - IEEE standard for a Real-Time Operating System
5. MODEL-BASED DEVELOPMENT (MBD)
6. Conclusion

Introduction

- Model-based development (MBD)
  - Reducing the development duration of satellite systems
- Space Cube® mk4
  - HILS (a Hardware-in-a-loop simulator) for MBD
  - Verification including hard real-time requirement
  - Heterogeneous computing edge node
    - Field Programmable Gate Array (FPGA), and Dynamically Reconfigurable Processors (DRPs)
    - SpaceWire/SpaceFiber interfaces for onboard equipment verification
    - PCI Express interfaces for ground support equipment
- DESTINY+
  - The first application of Space Cube® mk4



The outlook of Space Cube® mk4 and its interior assembly

DESTINY+ : The first application of MBD with Space Cube® mk4

- Mission objectives
  - Science and technology demonstration mission to asteroid (3200) Phaethon
    - Phaethon: the parent body of the Geminids meteor shower.
    - The associated cosmic dust is considered as a source of the organic matter on the Earth.
  - Expanding the opportunities for small body exploration by acquiring advanced asteroid flyby exploration technologies
  - Developing spaceflight technologies using electric propulsion and expand the range of its utilization
  - The chance for Phaethon flyby is only one time
    - The simulation on the ground requires higher accuracy which requires MBD
- Nominal launch window : FY2024
- 480 kg / 3kW spacecraft with Ion Engines

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Space Cube® mk4 – Heterogeneous processing edge node

- Three types of processing elements (PEs) are integrated on a Space Cube® mk4.

  - FPGA
    - Xilinx Kintex UltraScale KU060
    - Open-source hardware IP processor : LEON5 provided by Frontgrade Gaisler AB
    - FPGA with a micro-processor LEON5 IP

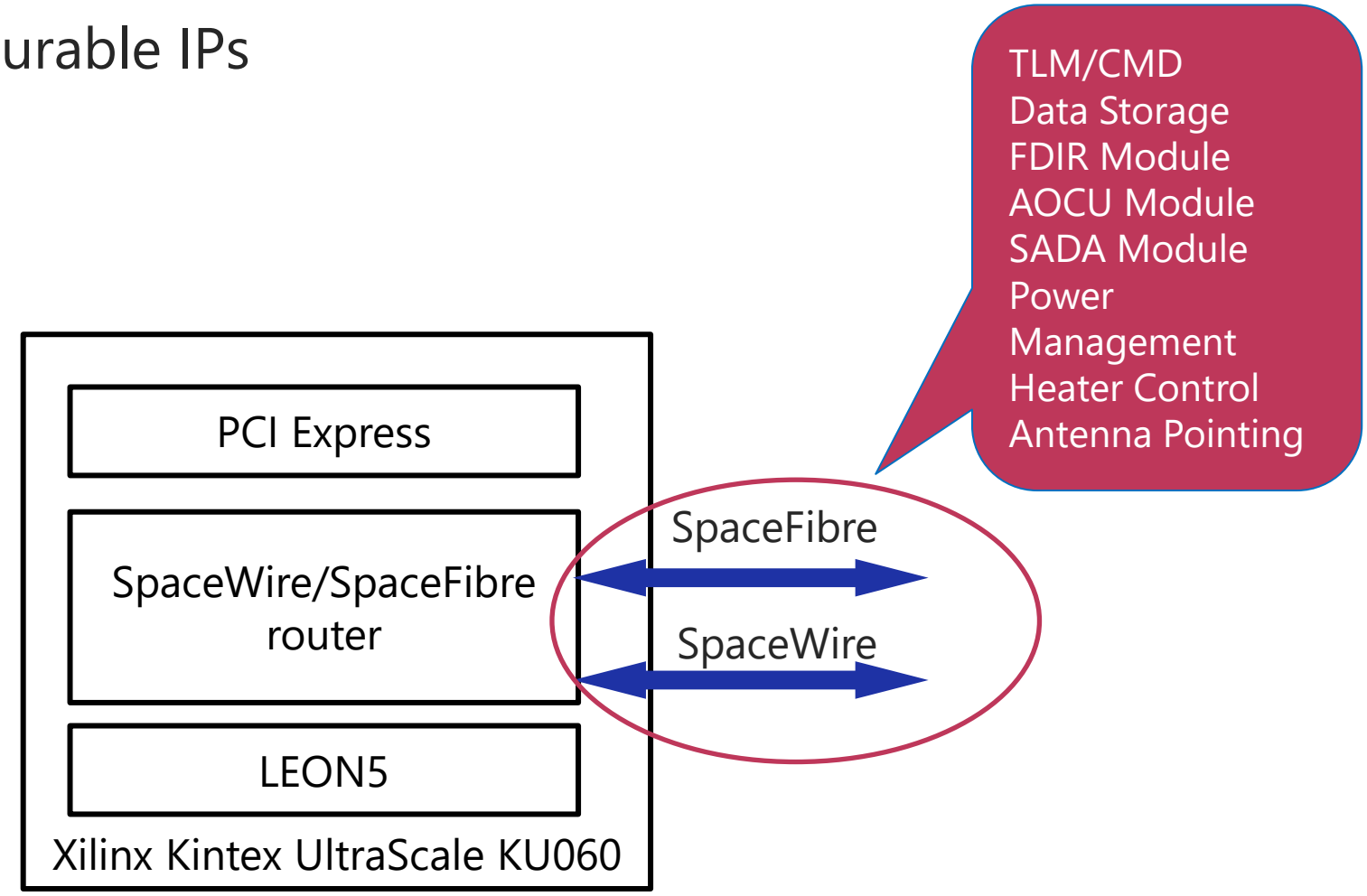
  - RZ/V2M
    - DRP (Dynamically Reconfigurable Processor)
    - AI Accelerator (DRP-AI)
      - a high-speed AI inference and low power consumption
      - realizes 1TOPS/W class power performance.

  - RZ/A2M
    - DRP with high-speed peripherals

The outlook of Space Cube® mk4 and its interior assembly

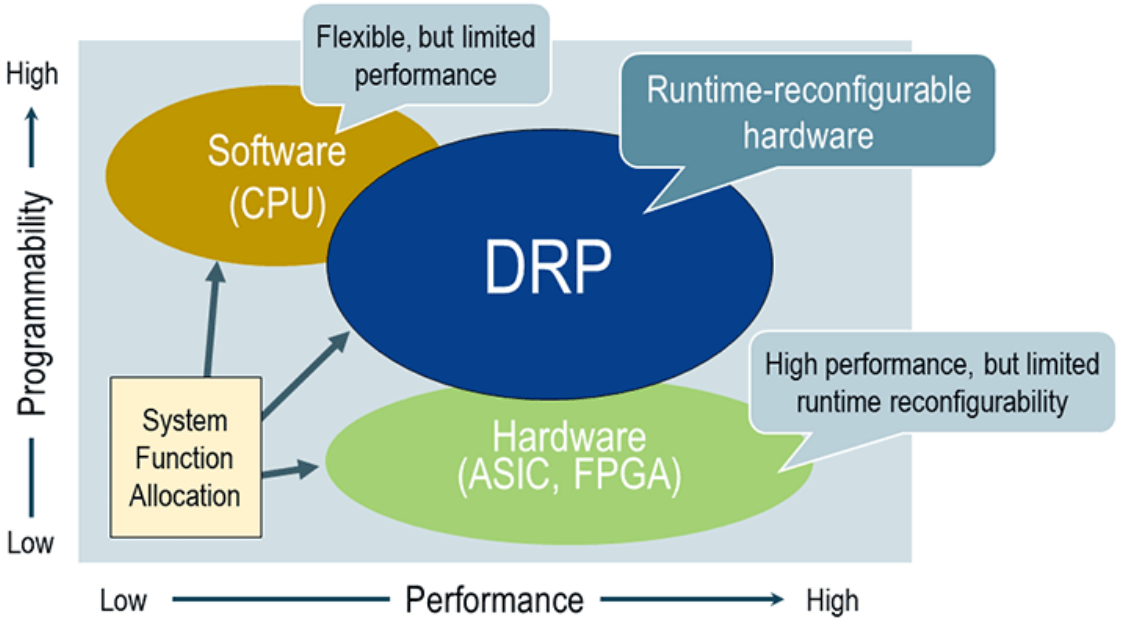
Main controller of Space Cube® mk4

- MBD controller using reconfigurable IPs
- LEON5 micro processor core
  - provided by Frontgrade Gaisler AB
- SpaceWire/SpaceFibre router
  - developed by NEC
- IEEE standard open source Real-time operating system
  - provided by TRON Forum

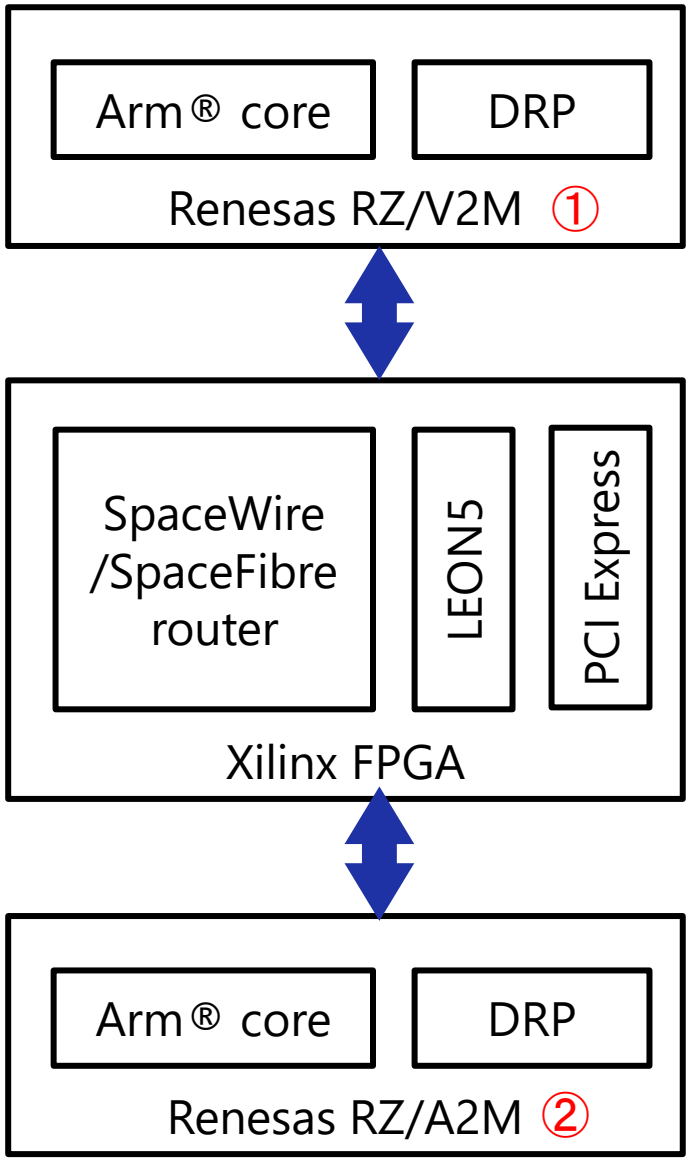


Dynamically Reconfigurable Processor (DRP) (1/2)

- RZ/V2M -①
  - Heavy load processing as neural network functions for artificial intelligence applications can be implemented with sufficient low power consumption as an edge node processor.
- RZ/A2M -②
  - RZ/A2M is used as a small-scale embedded controller with an Arm®-based micro-controller.

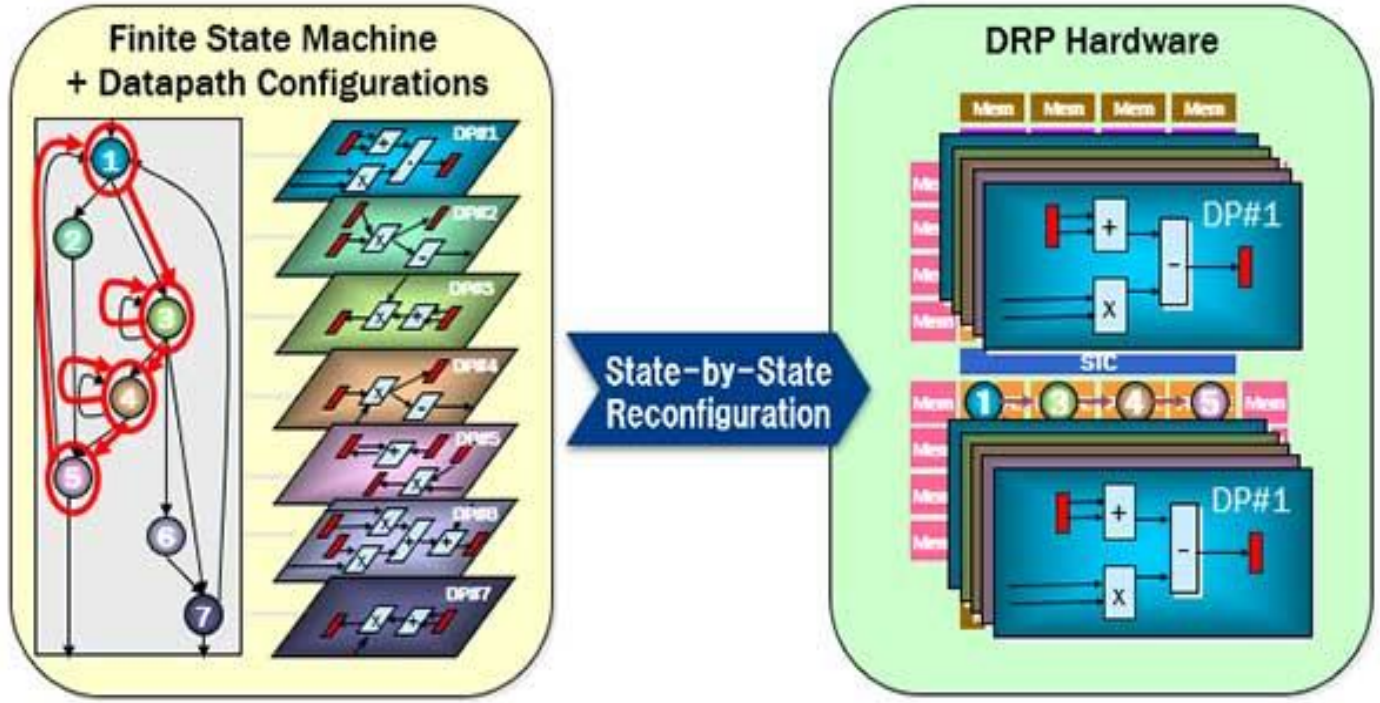


https://www.renesas.com/jp/en/application/key-technology/artificial-intelligence/voice-face-recognition/drp



Dynamically Reconfigurable Processor (DRP) (2/2)

- Dynamic Reconfiguration
  - Several context planes in a chip
  - Context switching even in every clock cycle.
  - Wire rate processing capability up to 10 MHz by programmable software



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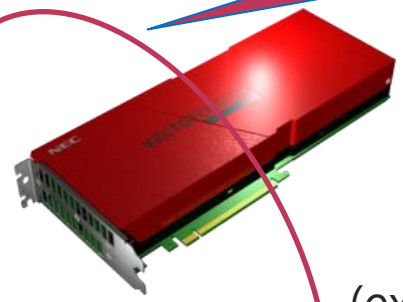
https://www.renesas.com/jp/en/application/key-technology/artificial-intelligence/voice-face-recognition/drp

High speed interface for scalability

- Giga-bit signal transmission interfaces
- SpaceFibre interfaces for high speed mission data processing
- PCI Exress intefaces for the simulation of orbit models and orbit environment



https://www.nec.com/en/global/solutions/hpc/sx/vector_engine.html

(ex.) Aurora Vector Engine
GPGPUs, etc.

IEEE 2050-2018

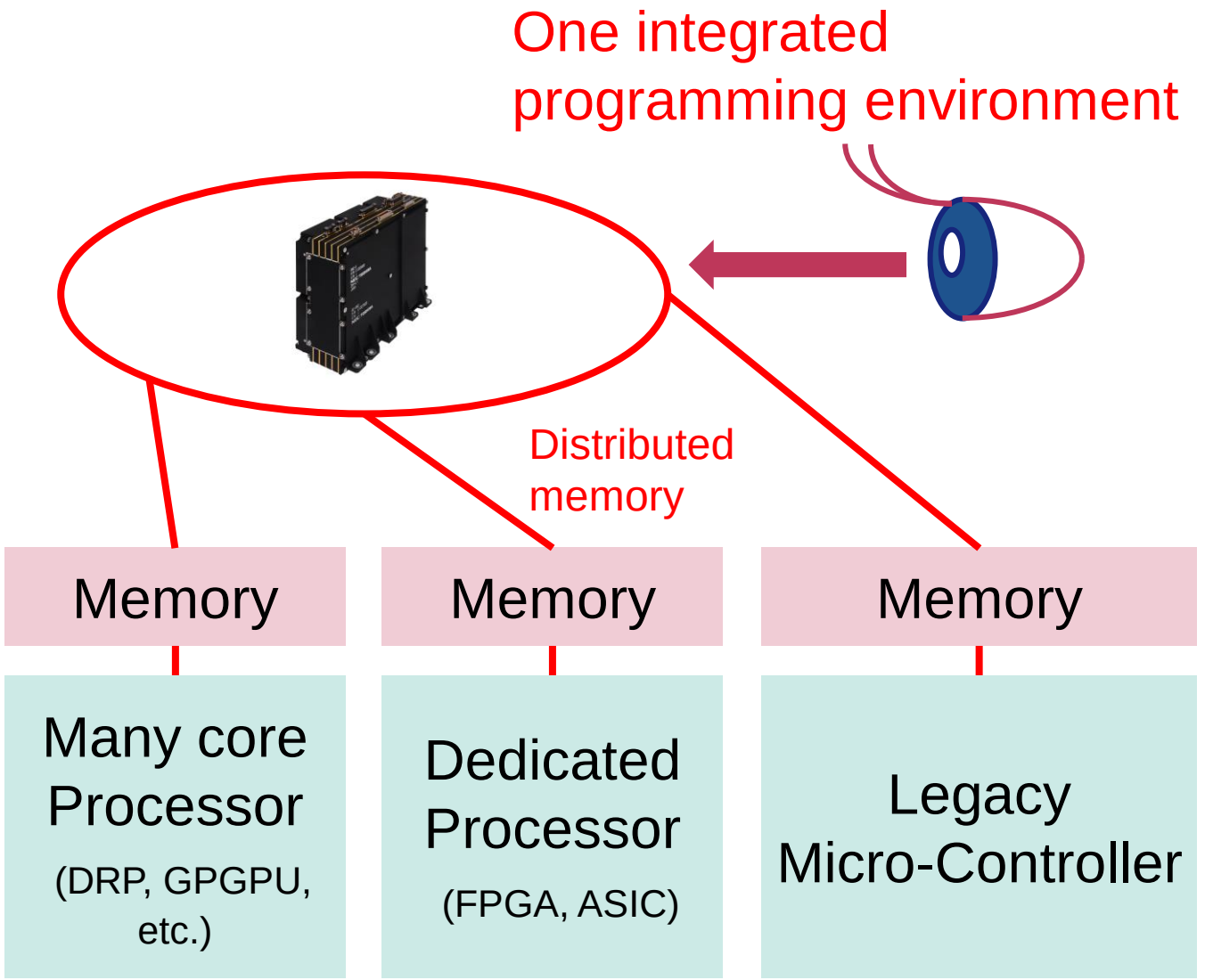
- IEEE Standard for a Real-Time Operating System (RTOS) for Small-Scale Embedded Systems
  - https://standards.ieee.org/ieee/2050/7178/
  - TRON Real-Time OS (RTOS) Family recognized as IEEE Milestone
  - https://www.tron.org/blog/2023/06/press0622/

- Aerospace oriented implementation is available as open-source software
  - T-Kernel 2.0 Aerospace has been ported on LEON5
  - https://www.uctec.com/iot-products-en/iot-products/os/tkas/

µT-Kernel 2.0

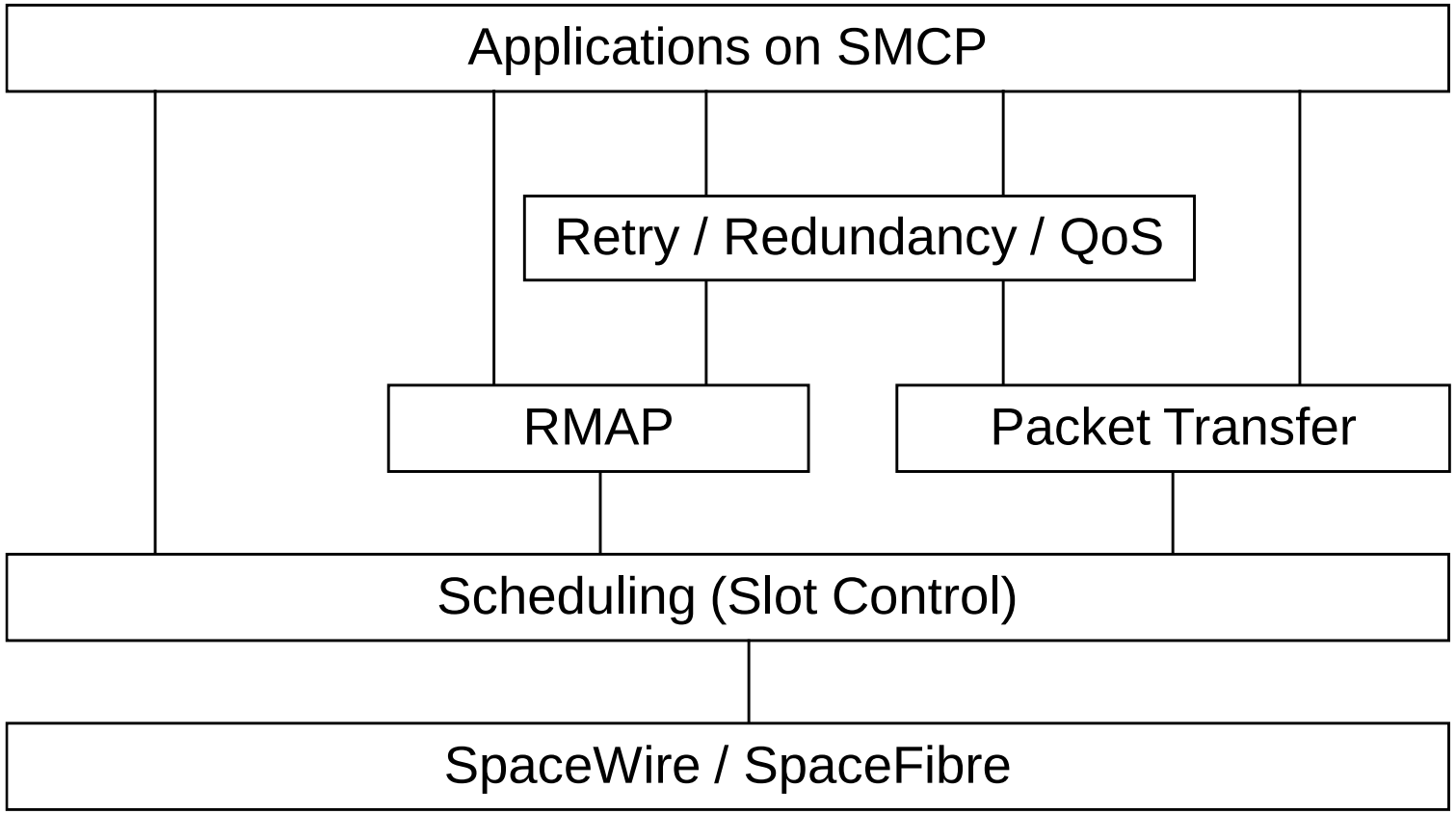
Issues to encapsulate heterogeneous processing element

- Example: ICU4SAT
  - A RISC-V core and a soft-core GPU are integrated using LLVM compiler.
    - P. Nannipieri, G. Giuffrida, L. Diana, S. Panicacci, L. Zulberti, L. Fanucci., H. Gerardo, M. Hernandez, M. Hübner, “ICU4SAT: A General-Purpose Reconfigurable Instrument Control Unit Based on Open Source Components,” Proc. 2022 IEEE Aerospace Conf. (AERO), 2022, DOI: 10.1109/AERO53065.2022.9843414 .a conventional micro-processor
- Our approach :
  - System level object model
    - Spacecraft Monitor & Control Protocol (SMCP)
  - C-language level integration
    - High level/behavioral synthesis based on 4-layered model
  - Middle-out approach
    - A dedicated programming language to encapsulate heterogeneous PEs



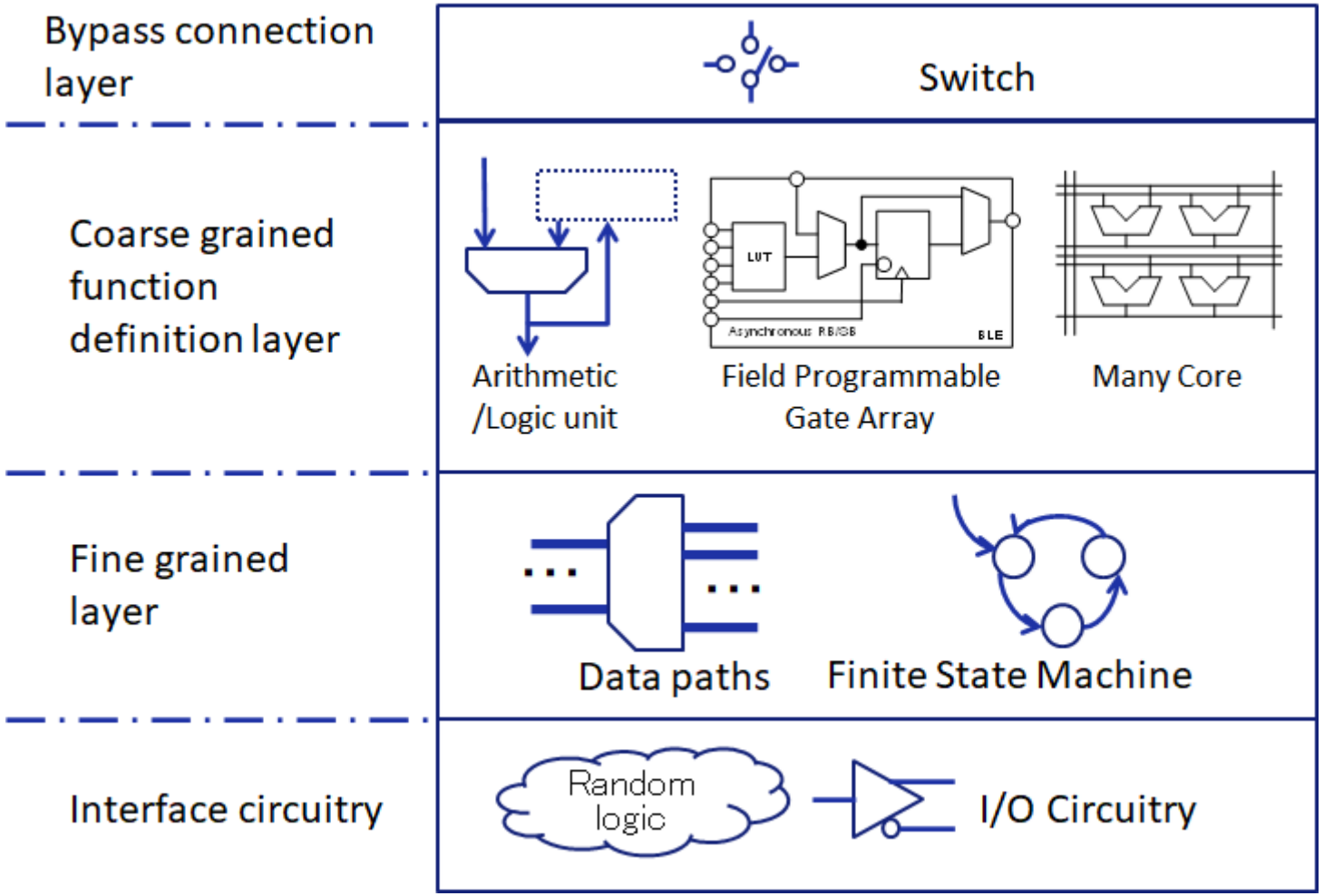
MODEL-BASED DEVELOPMENT (MBD)

- Space Monitor & Control Protocol (SMCP)



Layered design framework of heterogeneous computing edge node

- PE (Processing Element) design with the four-layered design framework



Conclusion

- Versatile simulator
  - Space Cube® mk4 accommodates three types of processing element, a conventional micro-processor, an FPGA, and a DRP.
- Established design framework based on SMCP and 4-layered model
  - The method to exploit hybrid and reconfigurable computing technology has been established based on Spacecraft Monitor & Control Protocol (SMCP) and 4-layered model.
- Model-based development
  - The process is employed prior to system level integration test to follow the tight development schedule.
- DRPs and a SpaceWire/SpaceFibre router are key components
  - Extensive simulation is performed by a hardware-in-the-loop simulator.

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