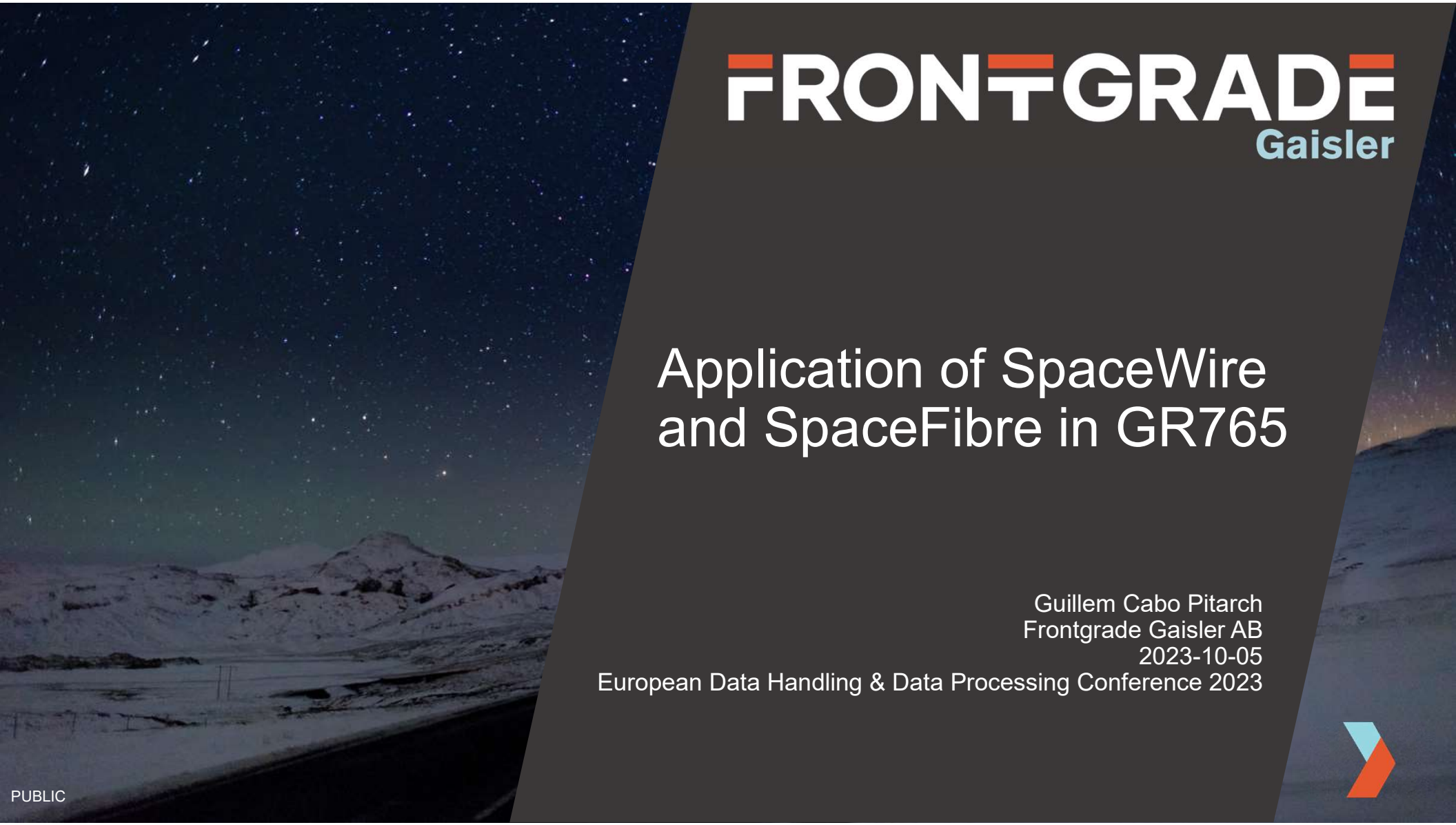


FRONTGRADE Gaisler

# Application of SpaceWire and SpaceFibre in GR765

Guillem Cabo Pitarch
Frontgrade Gaisler AB
2023-10-05
European Data Handling & Data Processing Conference 2023

PUBLIC

# Agenda

**01** Background: GR740

**02** GR765 – next generation SoC

**03** SpaceWire and SpaceFibre in GR765

**04** Conclusions

FRONTGRADE Gaisler

01

# Background: GR740

Quad-Core LEON4FT Processor

# GR740 - Quad-Core LEON4FT Processor

### Value proposition

- High performance, wide range of interfaces
- SPARC V8 compliant, Radiation-hard and Fault Tolerant
- Designed as ESA's Next Generation Microprocessor, NGMP
- LEON Technology – re-use of Development and Software ecosystem
- Low risk, off-the-shelf product, QML Q/V
- Excellent performance/watt ratio
  - Very low power, < 3 W (core typical)
  - Performance 1700 DMIPS (1000 MIPS)

| STANDARD MICROCIRCUIT DRAWING | PREPARED BY Phu H. Nguyen | DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime | |
|---|---|---|---|
| THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE | CHECKED BY Phu H. Nguyen | | |
| | APPROVED BY Muhammad A. Akbar | MICROCIRCUIT, PROCESSOR, DIGITAL, CMOS, RADIATION HARDENED, QUAD CORE LEON4 SPARC V8 PROCESSOR, MONOLITHIC SILICON | |
| | DRAWING APPROVAL DATE 22-04-18 | | |
| AMSC N/A | REVISION LEVEL | SIZE A / CAGE CODE 67268 | 5962-21204 |
| | | SHEET 1 OF 51 | |

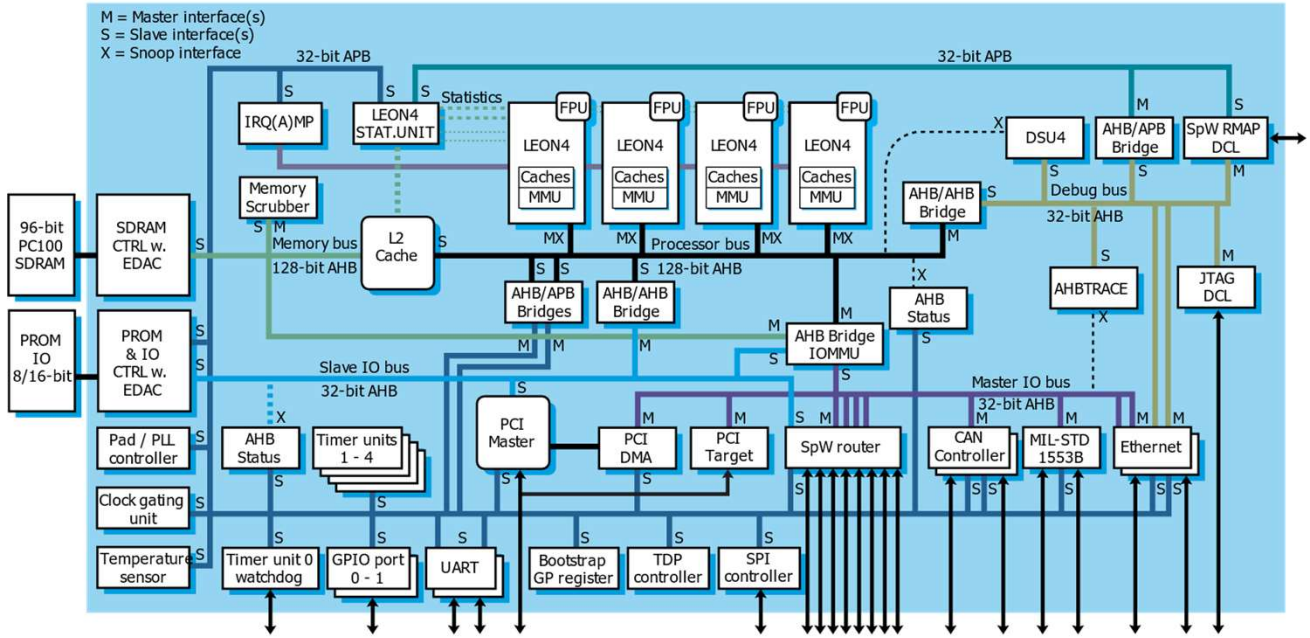
DSCC FORM 2233
APR 97
5962-E021-21

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

# GR740 - Quad-Core LEON4FT Processor

## Features

- Fault-Tolerant **Quad-processor SPARC** V8 integer unit with 7-stage pipeline, 8 register windows, 4x4 KiB instruction and 4x4 KiB data caches
- Double-precision IEEE-754 FPU (1 FPU/Core)
- **250 MHz**
- >1700 DMIPS
- Power consumption < 3W (core, typical)
- 2 MiB **Level-2** cache
- 64-bit PC100 SDRAM memory interface with Reed-Solomon EDAC
- 8/16-bit PROM/IO interface with EDAC
- CPU and I/O memory management units
- Multi-processor **interrupt controller** with support for asymmetric and symmetric multiprocessing
- **SpaceWire TDP** controller and support for time synchronisation




**Interfaces**

- **SpaceWire router** with **8 SpaceWire links** (200 MHz)
- 2x 10/100/1000 Mbit **Ethernet** interfaces
- 2x MIL-STD-**1553B** interface
- 2x **CAN** 2.0 controller interface
- 2x **UART, SPI**, Timers and watchdog, 16+22 pin GPIO
- PCI Initiator/Target interface
- JTAG

FRONTGRADE Gaisler

02

# GR765

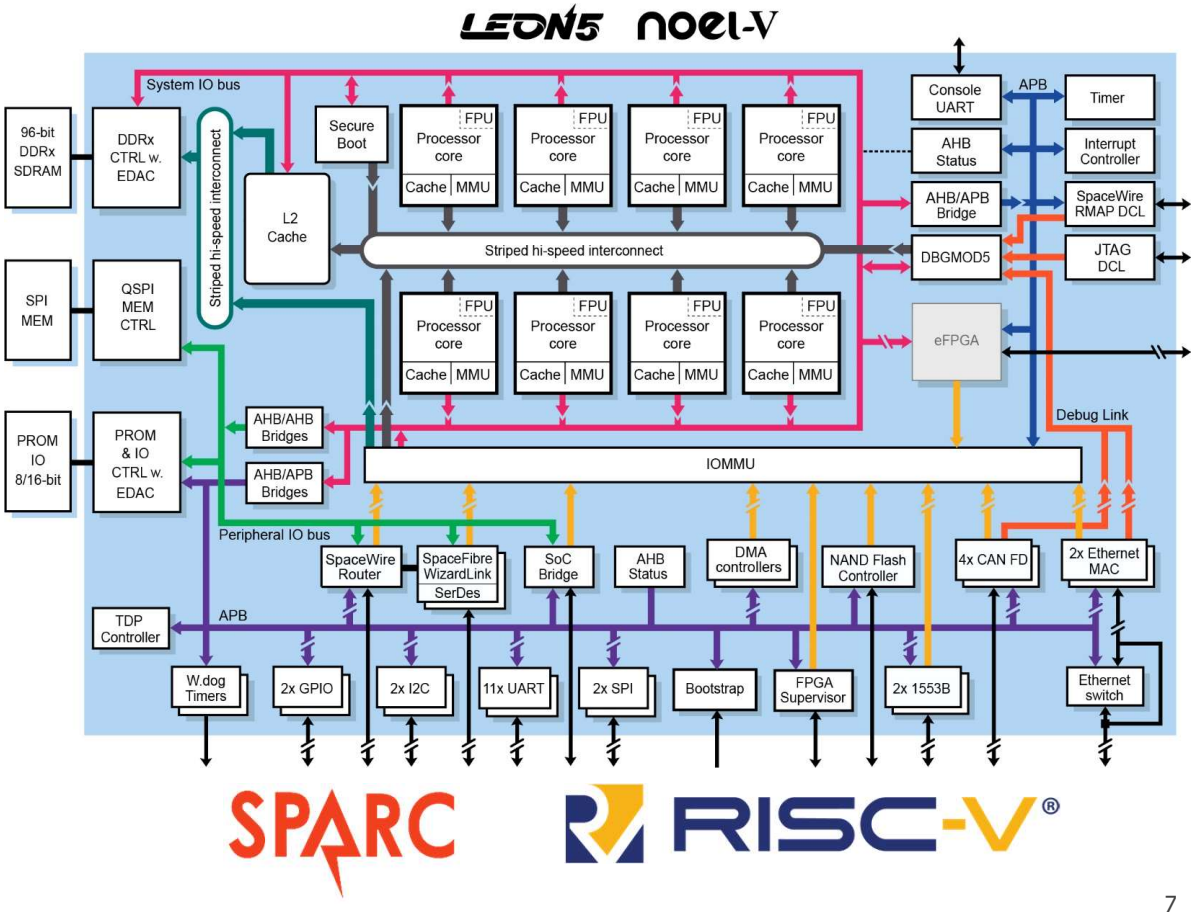
Next-Generation SoC

# GR765 – Octa-Core Processor

**Baseline Features**

- Fault-tolerant **octa-core** architecture
  - **LEON5FT SPARC V8 or NOEL-V RV64GCH**
  - Dedicated FPU and MMU, 64 KiB per core L1 cache, connected via multi-port interconnect
- **1 GHz processor frequency - 26k DMIPS**
- 2+ MiB L2 cache, 512-bit cache line, 4-ways
- **DMA** controllers
- **DDR2/3/4**(TBD) interface with dual x8 device correction capability
- 8/16-bit PROM/IO interface
- **(Q)SPI and NAND** memory controller interfaces
- **Secure Element,** providing boot image authentication
- **NX eFPGA ~30k LUT** (option)
- **High-pin count – LGA1752** package allows reduction of pin sharing
- **Target technology: STM 28nm**

**In development**
**No guarantee of product launch**

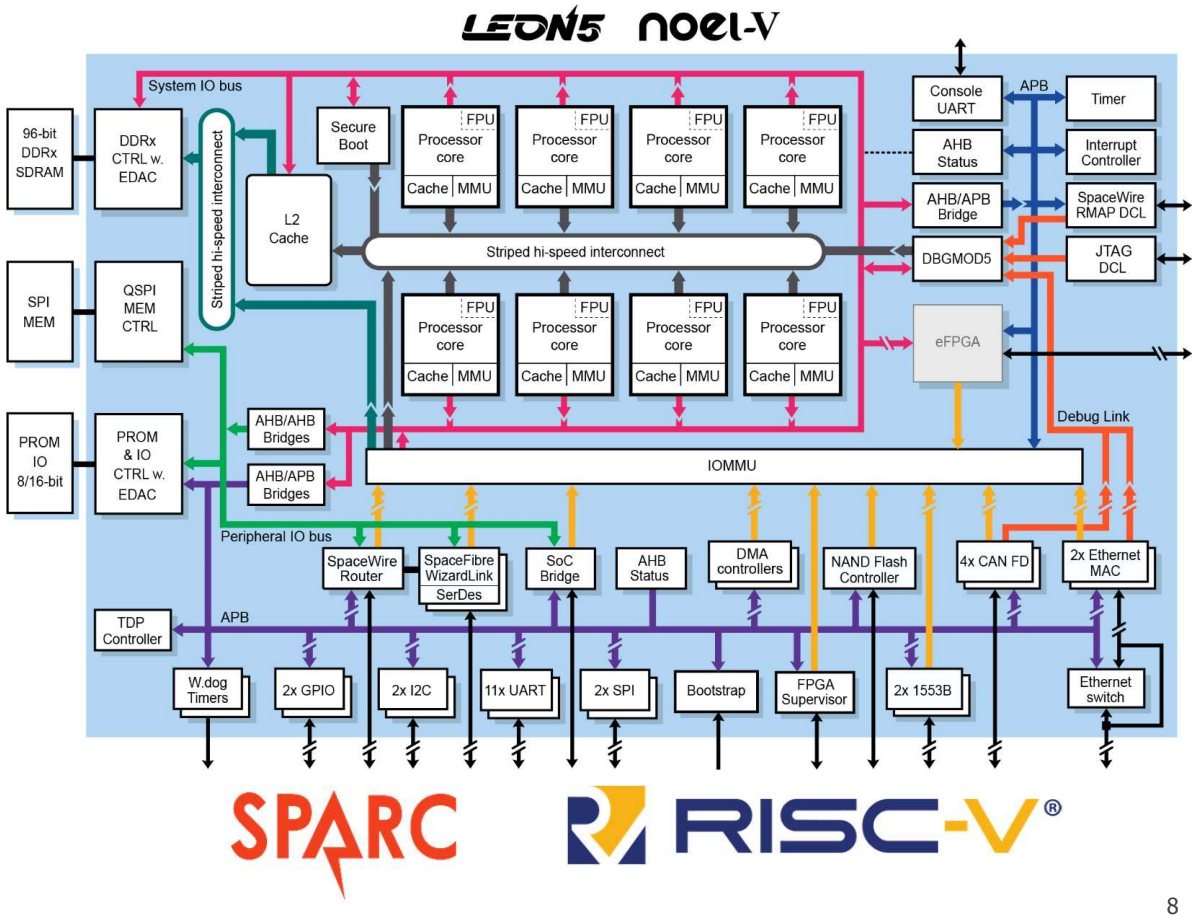


# GR765 – Interfaces

**Interfaces – SPARC and RISC-V mode**

- **SpaceFibre x8 lanes 6.25 Gbit/s + WizardLink support**
- **12-port** SpaceWire router with +4 internal ports
- 2x 10/100/1000 Mbit Ethernet **w. TTEthernet capable switch**
- **2x** MIL-STD-1553B
- **4x CAN FD**
- **2x I2C interface, 12** x UART, **2x** SPI controller
- **SoC Bridge interface**
- **FPGA Supervisor interface**
- Timers & Watchdog, GPIO ports
- Debug links:
  - Dedicated: JTAG and SpaceWire
  - CAN, SpFi, Ethernet

**In development**
**No guarantee of product launch**



# Instruction Set Architectures

**Why RISC-V?**

- **Hardware and software potential** for future space applications: A new class of processors requires a modern architecture
- Enabling new technologies by **standardization**
  - Hypervisor support
  - Vector extension, …
- Growing base of **3rd party ecosystem**:
  - Toolsets
  - Libraries, engines etc.
- Attractive to talent entering the space domain
- Influx of know-how by talent entering the space domain

**Why SPARC?**

- Existing base of space **proven HW and SW** designs
- **Mature ecosystem** for today's space applications, e.g. qualified OS
- Accumulated development know-how in the industry
- Software **backward compatible** with existing LEON devices

**GR765 provides RISC-V and SPARC**

- Both architectures are needed by the industry
- Faster **time-to-market** for RISC-V while continuing SPARC – ease transition between the two architectures
- **Minimal silicon overhead** - sharing of resources on chip. User selects CPU (LEON5FT or NOEL-VFT), device cannot operate with both at the same time.

FRONTGRADE Gaisler

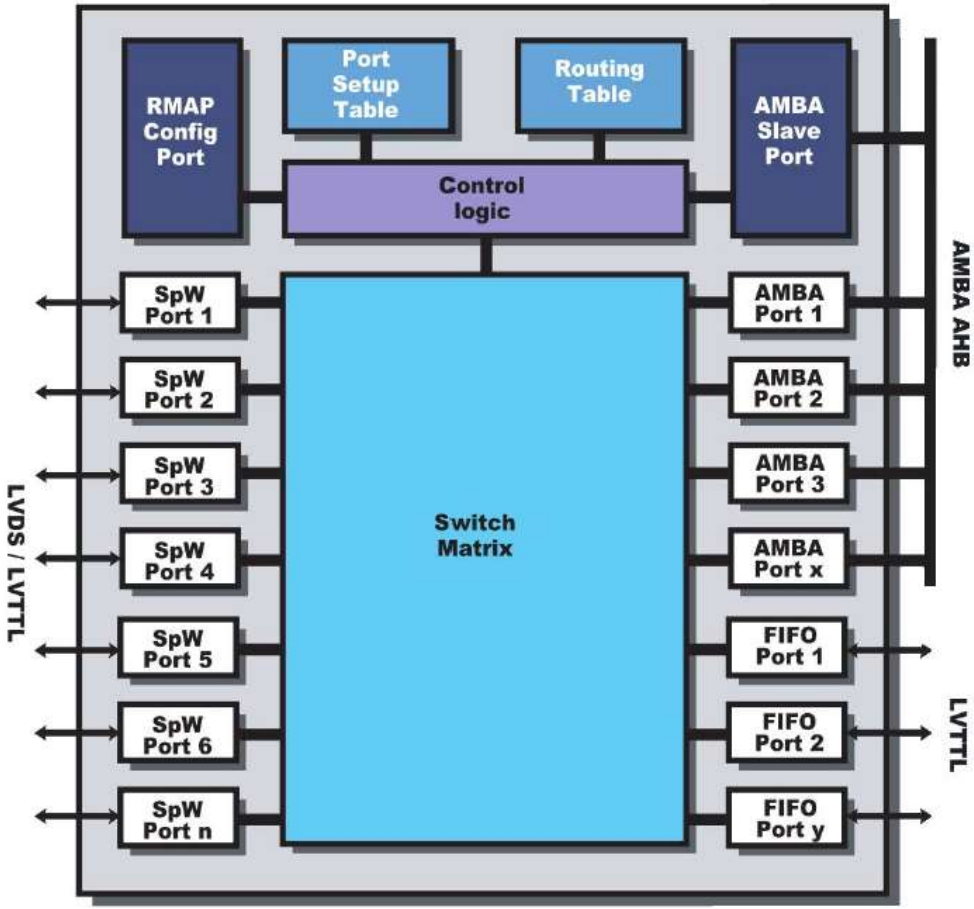
# 03

# GR765

SpaceWire and SpaceFibre support

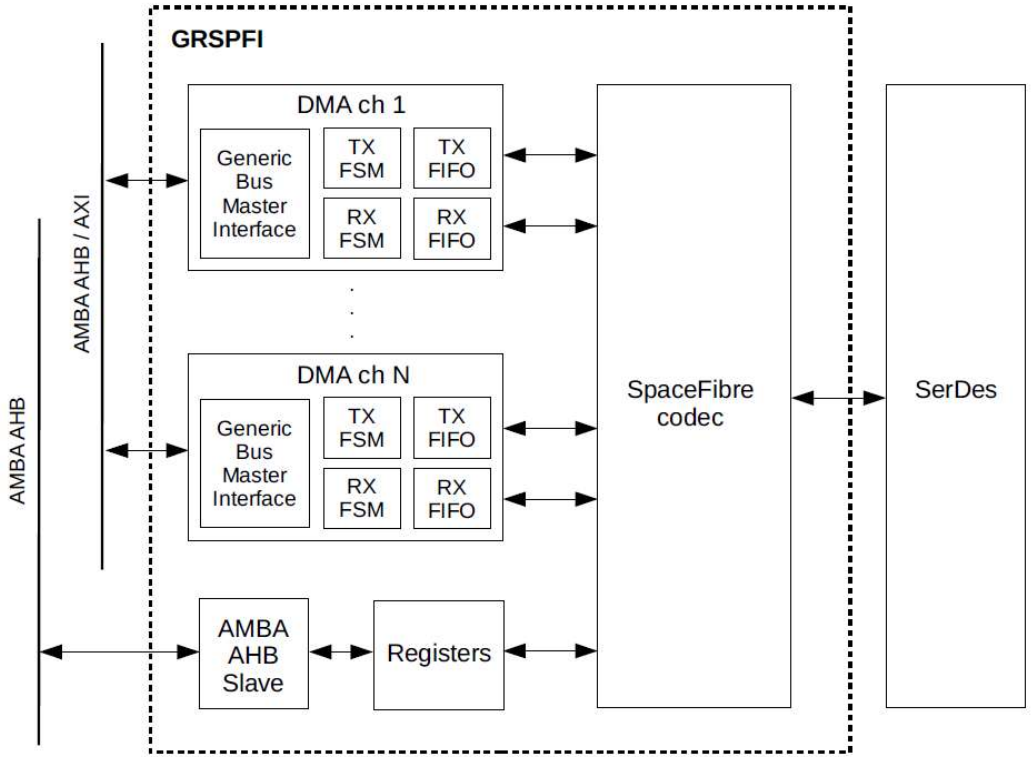
# GR765 – SpaceWire router

- GRSPWROUTER implemented as per **ECSS-E-ST-50-12C** specification
- Features three types of ports:
  - **SpaceWire ports** (external ports)
  - **FIFO ports** (internal ports)
  - **AMBA ports** (DMA)
- GR765 extends the **number of external ports** from 8 to **12**
- AMBA ports include an **RMAP target** and several **DMA** channels
- Configuration port with RMAP target to allow independent operation from the processor / software
  - The router can be configured by SpaceWire nodes without processor intervention
- Two main applications:
  - SpaceWire connectivity for the processor cores
  - Routing capabilities for external SpW nodes



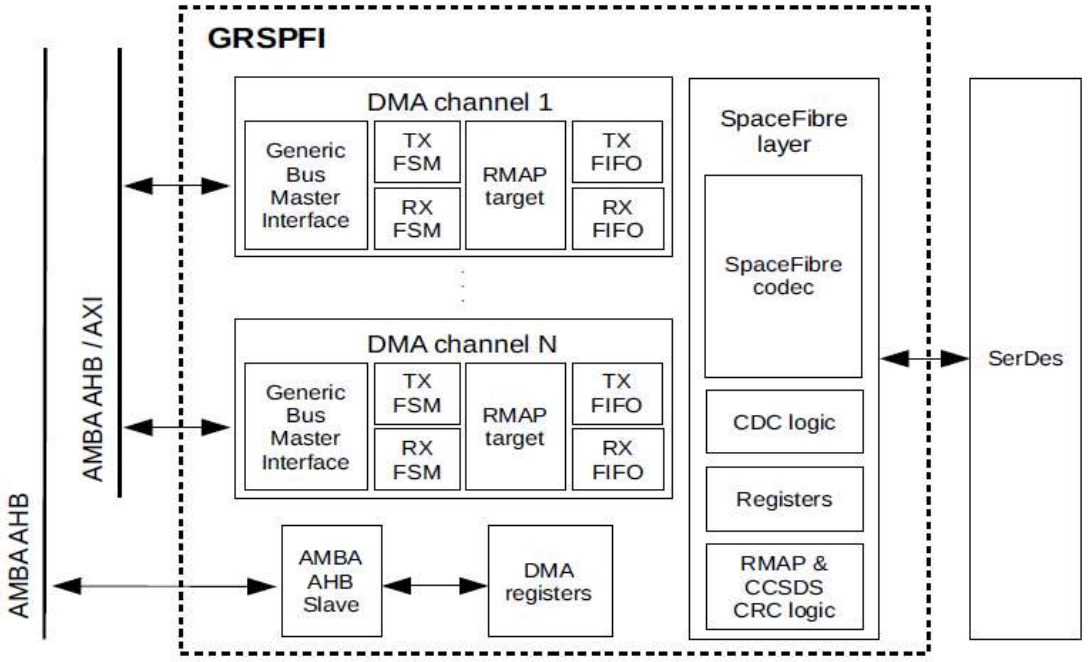
# GR765 – SpaceFibre interfaces

- GR765 will include **8 SpaceFibre** interfaces supporting up to **6.25 Gbps**
- SpaceFibre codec designed according to the **ECSS-E-ST-50-11C** standard
- **Single lane** implementation
- Flexible DMA engine with **multiple DMA channels**
  - Each channel has its own AHB/AXI master i/f
  - DMA channels operate in parallel and are assigned a subset of Virtual Channels and/or the Broadcast Channel
- **AHB slave interface** for configuration and control
- **On-chip SerDes** available on STMicroelectronics 28nm
- Required extensions for the GR765:
  - RMAP support
  - Integration with GRSPWROUTER
  - ST SerDes integration
  - Companion WizardLink controller



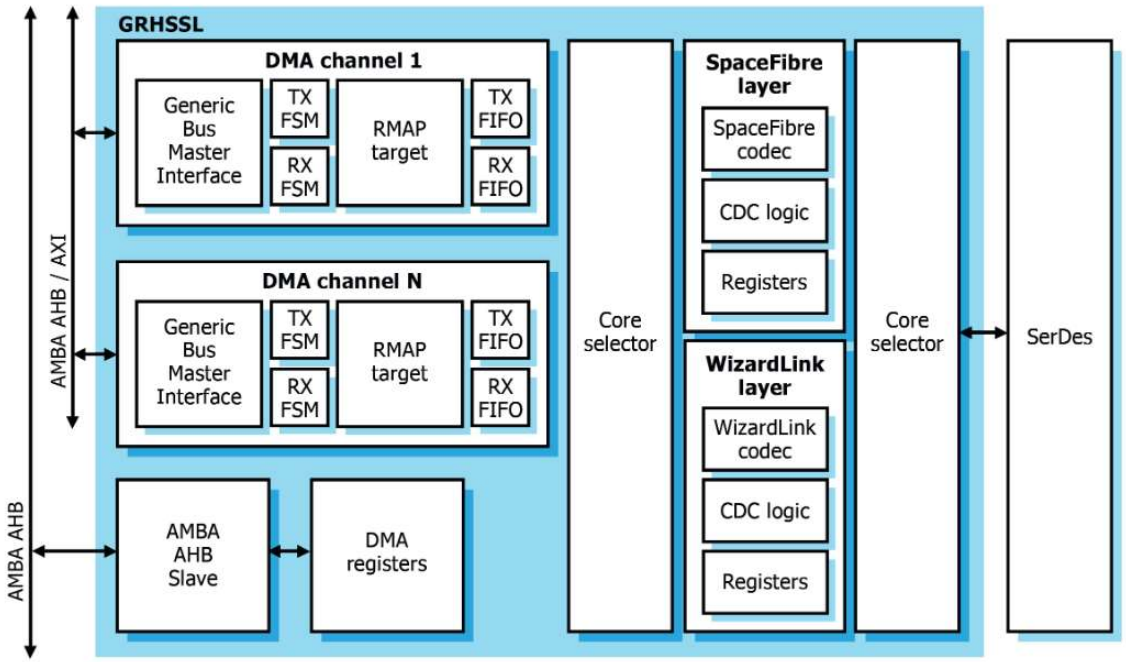
# GR765 extensions: SpFi RMAP support

- **RMAP** support added to the **SpaceFibre DMA** engine as per ECSS-E-ST-50-52C
- Same level of support as in **GRSPW2**, the SpaceWire controller in GRLIB:
  - Features may be extended, e.g., verify buffer size, alignment restrictions, etc.
- Dedicated **RMAP target per DMA** channel
  - Make use of the dedicated AHB/AXI master interface of every channel
- **RMAP** can be separately **enabled/disabled** and configured in **run time** for each virtual channel
  - Each VC has a dedicated node address and destination key register
- Standalone RMAP CRC-8, CCSDS CCITT CRC-16 and 16-bit Checksum (J.G. Fletcher, ISO 8473-1:1998) logic for generic packets



# GR765 extensions: WizardLink

- Companion **WizardLink** controller designed to interoperate the TLK2711 transceiver
  - Compatible also with other SerDes
- Enable the communication with **legacy equipment** using **custom protocols** over WizardLink
- Minimal hardcoded functionality, high degree of configurability
- Transmission and reception of packets handled via **hardware descriptors**
  - Control characters need to be handled by software
- **Configurable commands via AHB** registers to automatically insert or extract control words
  - IDLE characters are mandatory
  - Other control words are optional
- **Only one controller** (SpaceFibre or WizardLink) can be active at a time, selectable at **run-time** via AHB registers



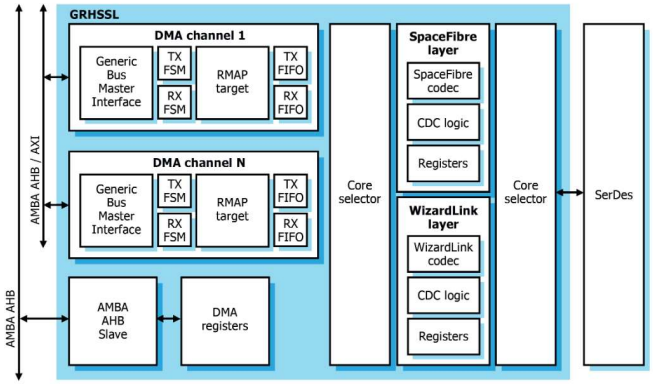
# GR765 extensions: SpFi integration with the SpW router

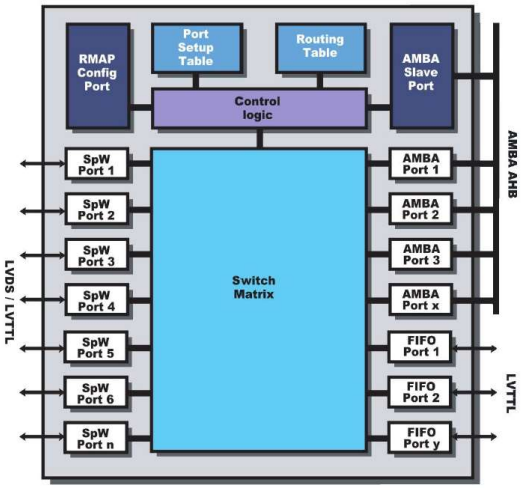
**Integration of SpaceFibre with the SpaceWire router**

- Bridge between SpaceWire and SpaceFibre traffic
- Configurable number of FIFO interfaces directly exposed as external ports
- Dynamic assignment of Virtual Channel to external FIFO interfaces at run-time via AHB registers
- Exposed Virtual Channels bypass the DMA engine
- SpaceFibre FIFO ports can then be connected to the SpaceWire internal FIFO ports
- External bridges to connect between GRSPFI and GRSPWROUTER:
  - SpaceFibre virtual channel data to SpaceWire characters
  - SpaceFibre broadcast messages to SpaceWire timecodes

**Bypass mode for WizardLink**

- External FIFO channel can still be used to expose codec to eFPGA
  - Stream high throughput data into a custom hardware accelerator



# GR765 extensions: integration with on-chip SerDes

**Integration with an ST SerDes macro**

- Ensure interoperability with the on-chip SerDes
- No modifications were needed on GRHSSL
  - Limited external glue logic mainly to adapt the register interface to the GR765 AMBA AHB infrastructure
- Aim is to support the full SpaceFibre range including 6.25 Gbps
  - Optionally up to 10 Gbps
- Exploit configurability of the SerDes IP via a memory-mapped register interface
  - Settings including the line rate can be configured in run time via registers (link reset required)

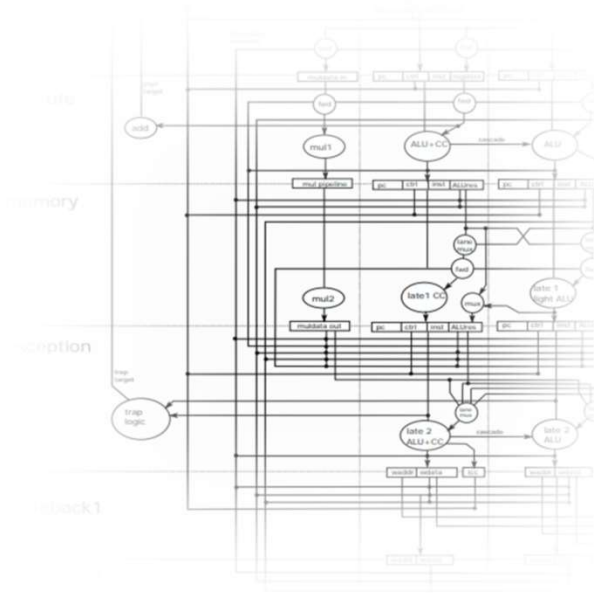
FRONTGRADE Gaisler

# 04

# Conclusions

# Conclusions

- The GR765 development builds on the successful GR740 quad-core LEON4FT component
- The GR765 is an **octa-core** microprocessor featuring **8 LEON5FT** and **8 NOEL-VFT** RISC-V 64-bit cores. Users can select between the two architectures via bootstrap signals
- GR765 supports **DDR2/3 SDRAM**, **high-speed serial link** controllers and several other extensions.
- **SpaceWire router** expanded: **12** external and **4** internal ports
- **8 SpaceFibre links** with **on-chip SerDes** supporting up to 6.25 Gbps
- **SpaceFibre DMA engine with RMAP** target based on GRSPW2 to facilitate SW migration
- **SpFi / SpW bridging** by mapping Virtual Channels to SpW router FIFO ports
- Companion **WizardLink controller** to enable communication with legacy equipment
- Progress to be reported via **www.gaisler.com/GR765**




Thank you for your attention!