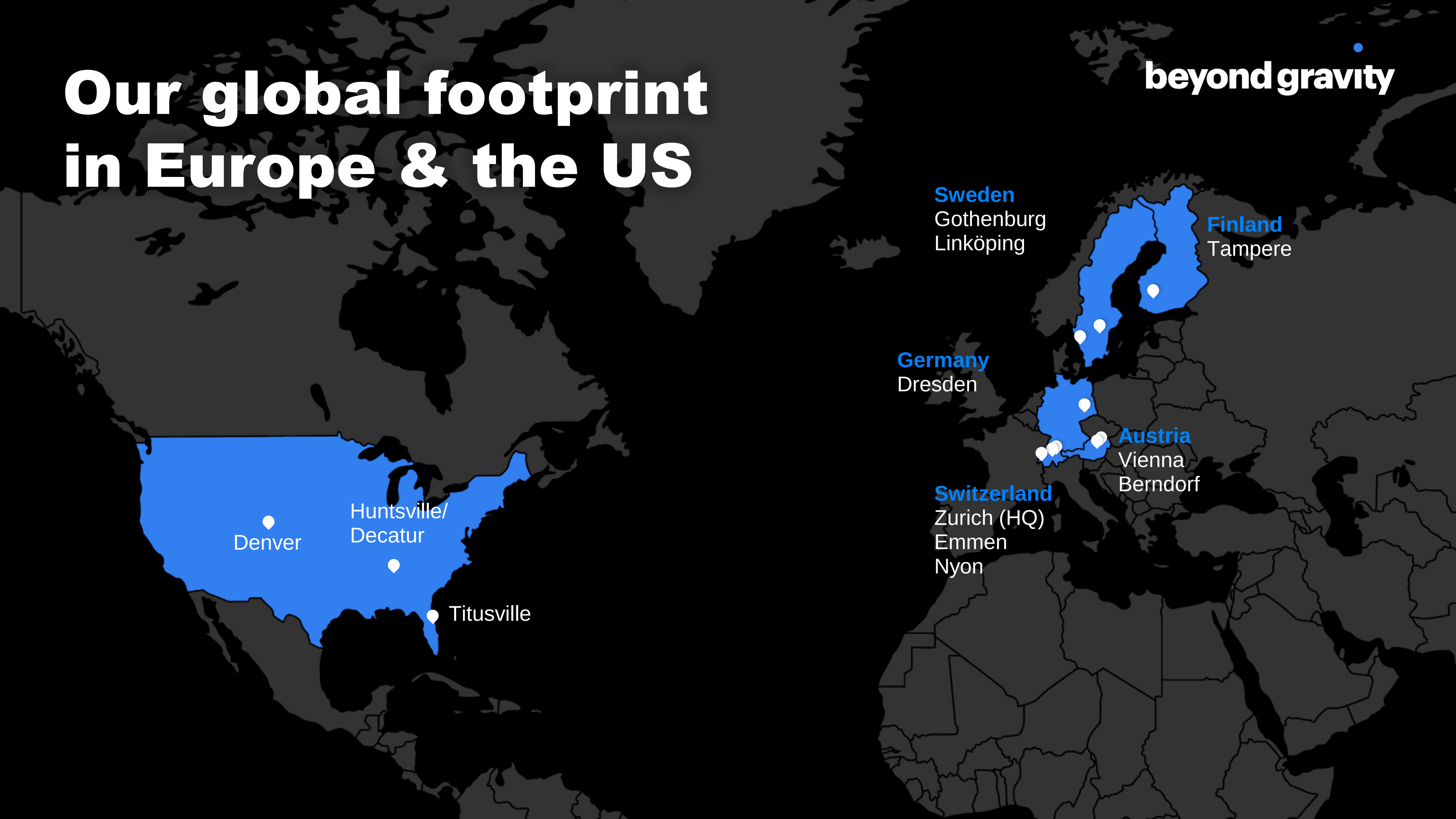
beyond gravity

Development of the CREOLE ASIC and the Next-Generation On-Board Computer

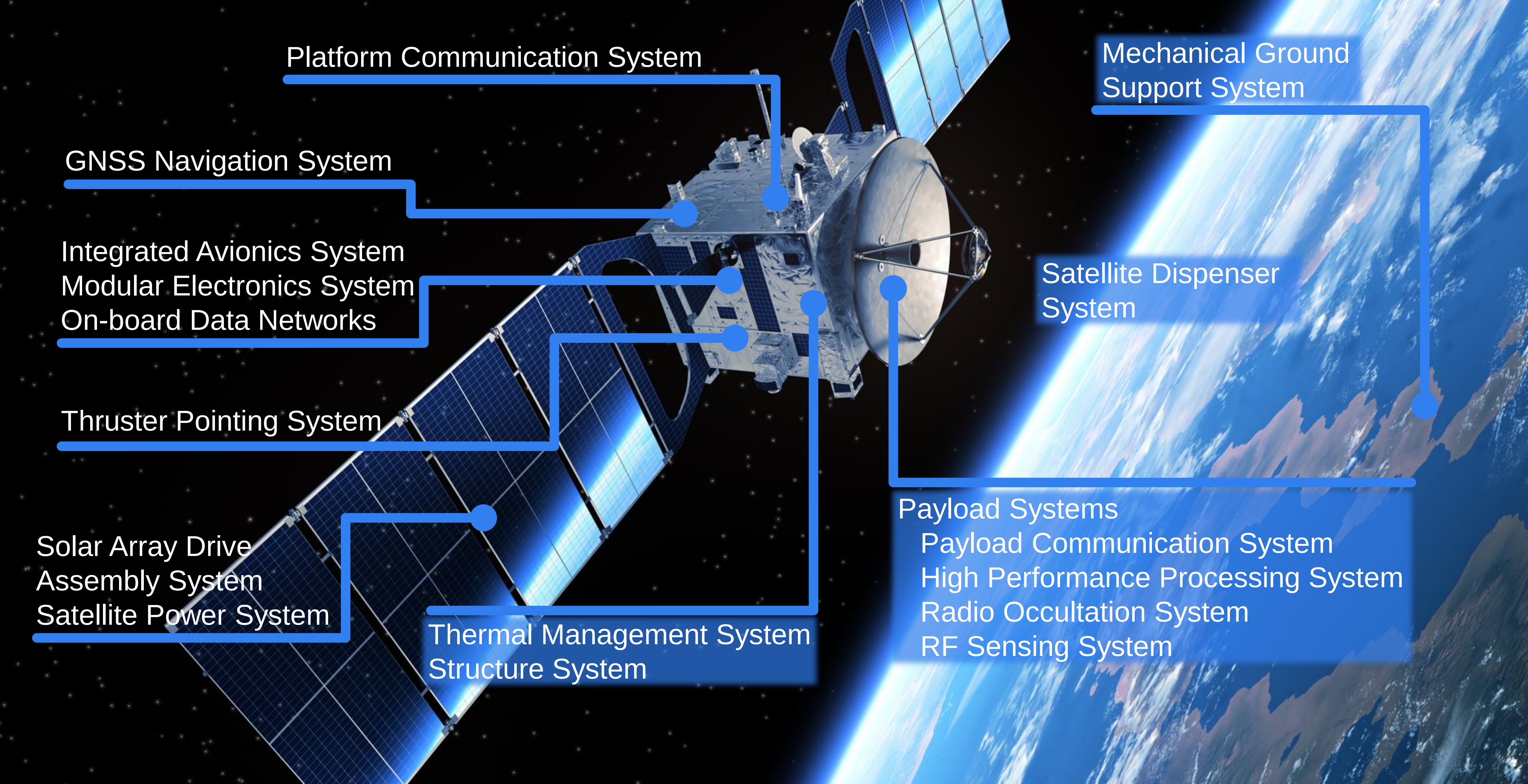
EDHPC2023 Juan-Les-Pins

06 10 2023 | Vilhelm Geijer

Our global footprint in Europe & the US



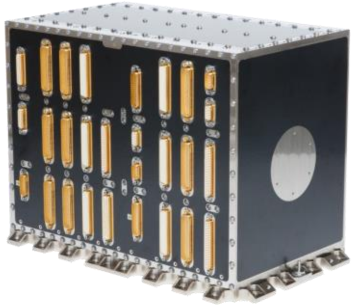
Satellite Systems

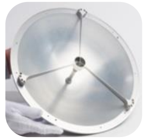


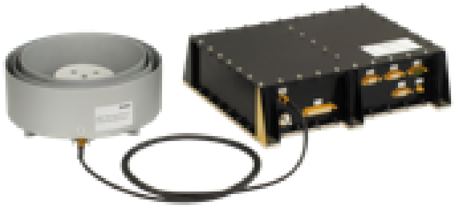
Satellite Electronics

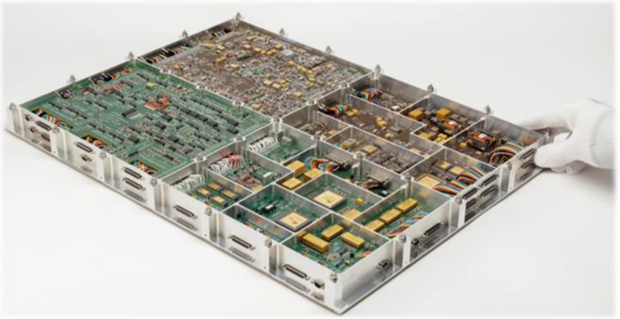
- Satellite On-Board Computer
- Remote Interface Units (RIU / RTU)
- Command and Data Handling Subsystems
- Data Processing
- Navigation Receivers
- Frequency Converters & Receivers
- Antennas








Introduction

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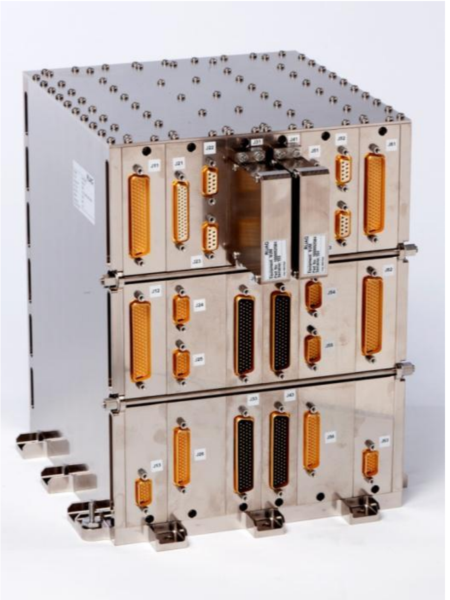
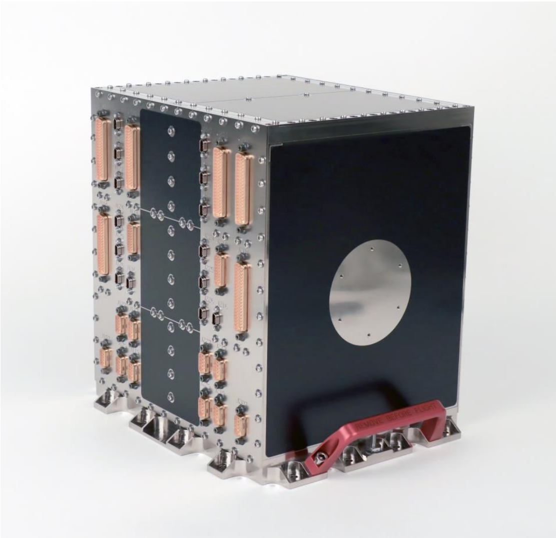
- The Single Board Computer Core (SBCC) activity was an ESA funded activity, with the aim at evolving Beyond Gravity's previous generation On-Board Computer.

- The previous generation OBC was based on three ASICs (COLE, CROME2 and Hamster).
- One major part of this activity was to integrate all three ASICs into one large SoC, the CREOLE ASIC.





Development Background

- The Single Board Computer Core (SBCC) study has been performed in three phases.
- Kostas Marinis (ESA) has been supporting all three phases as Technical Officer.

- Phase 1: Establishing the architecture of the next generation OBC as well as of the ASIC – called CREOLE – providing the functions of the OBC.
- Phase 2: Implementing the SBCC in a generic prototype HW, the CREOLE design in an FPGA, and performing verification of the concept.
- Phase 3: Implementing the CREOLE design in an ASIC, designing a dedicated HW, and performing verification of the final result.

Single Board Computer Needs

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- The up-to-date generation of OBCs and SMUs requires
  – reduced weight & volume
  – reduced power consumption
  – reduced cost

- Evolution of Standards
  – New CCSDS recommendations on security, CCSDS 355.0-R-3 (now released 355.0-B-2)
  – Updated SpaceWire standard: Time distribution, distributed interrupts, etc.
  – Deterministic SpaceWire traffic

- Evolution of Mission Needs
  – More memory (processing and mass memory)
  – File based operation (CCSDS File Delivery Protocol)
  – More SpaceWire links

Previous generation OBC Concept

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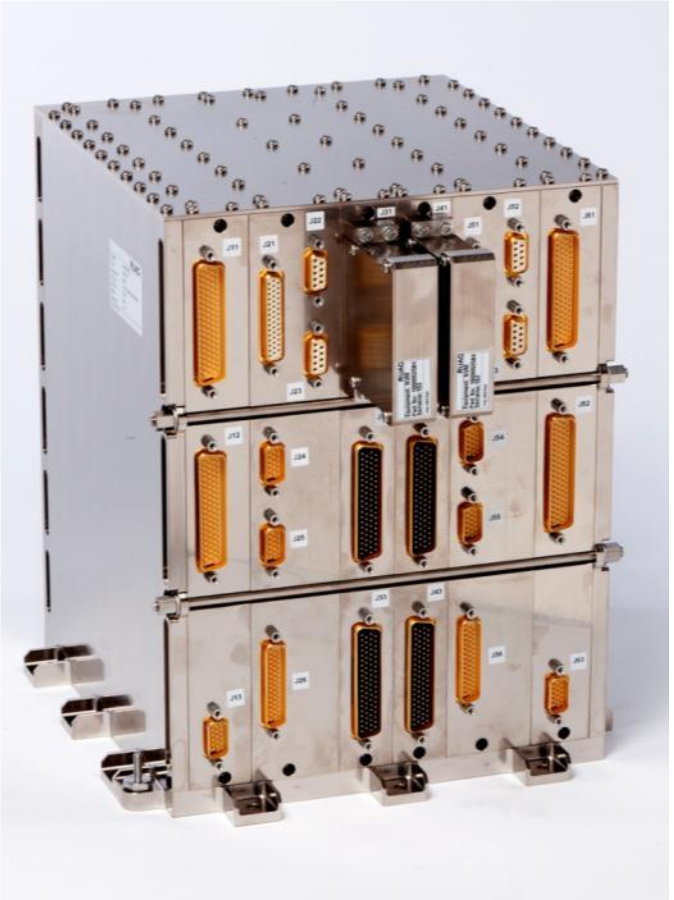
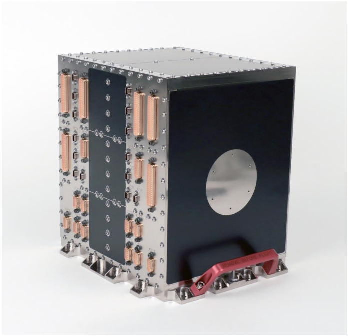
- Two digital boards per redundant OBC half; TTRM & PM
- TTRM (TM, TC, RM & MM)
  - Telecommand (TC)
  - Telemetry (TM)
  - Reconfiguration
  - Small Mass Memory
  - Two ASICs: CROME2 and Hamster
- PM (Processing Module)
  - LEON Processor
  - Control interfaces: MIL-STD-1553, SpaceWire, UART…
  - One ASIC: COLE
- Power board with High Priority Commands

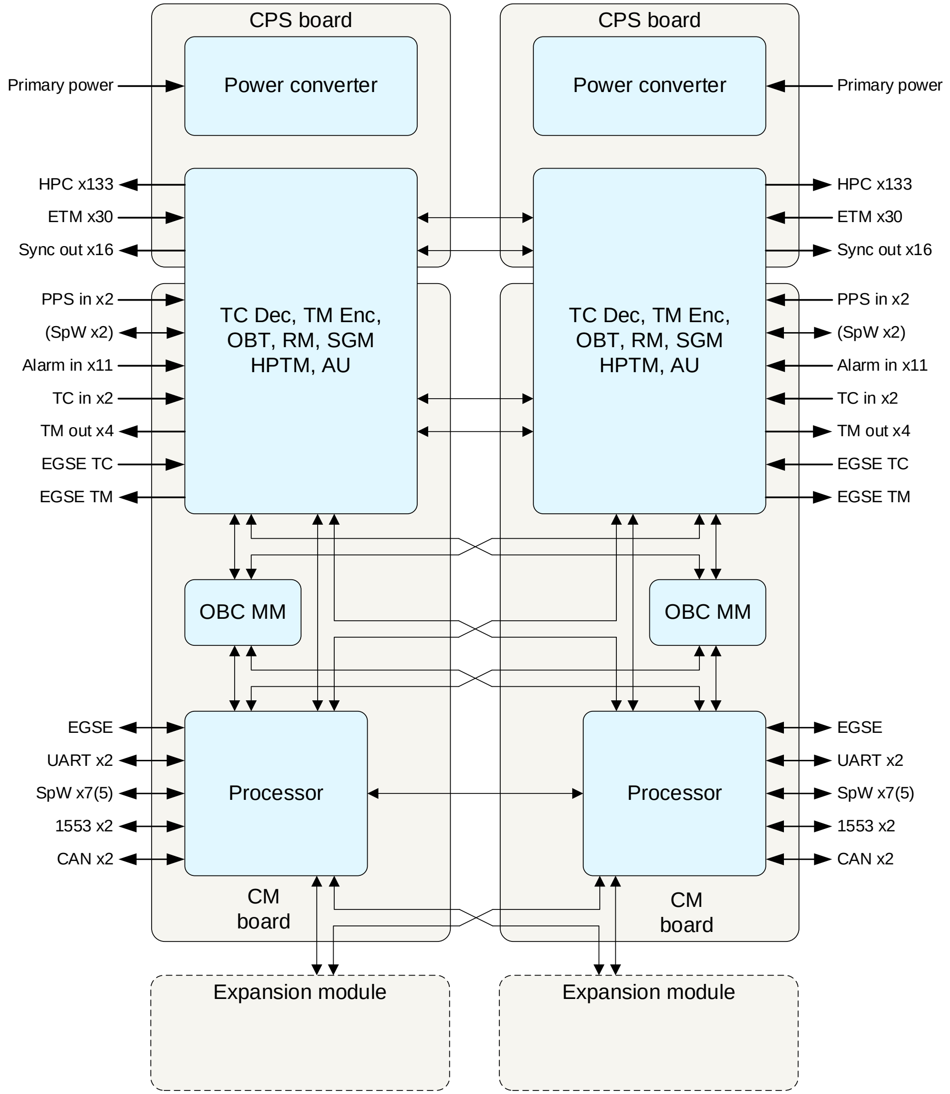


SBCC OBC Concept



- One digital board per redundant half
  - Combines and extends the functionality of the previous TTRM and PM boards
  - One System-on-Chip ASIC: CREOLE
  - Higher level of integration gives:
    - Reduced cost, less weight & volume, lower Power Consumption
- One power board per redundant half
  - Includes interfaces for High Priority Commands, Essential TM inputs, and Synchronisation pulses
  - Provides unit internal Telemetry acquisition

- Compliant with SAVOIR Avionics System Reference Architecture (ASRA) Generic OBC Specification
- Prepared for increasing performance significantly through additional add-on processor such as the GR740, or Field Programmable Gate Array (FPGA) for hardware acceleration.
- Prepared for expansion boards (in the middle) like Solid State Mass Memory (SSMM), SpaceWire router etc.



SBCC Functionality vs Savoir

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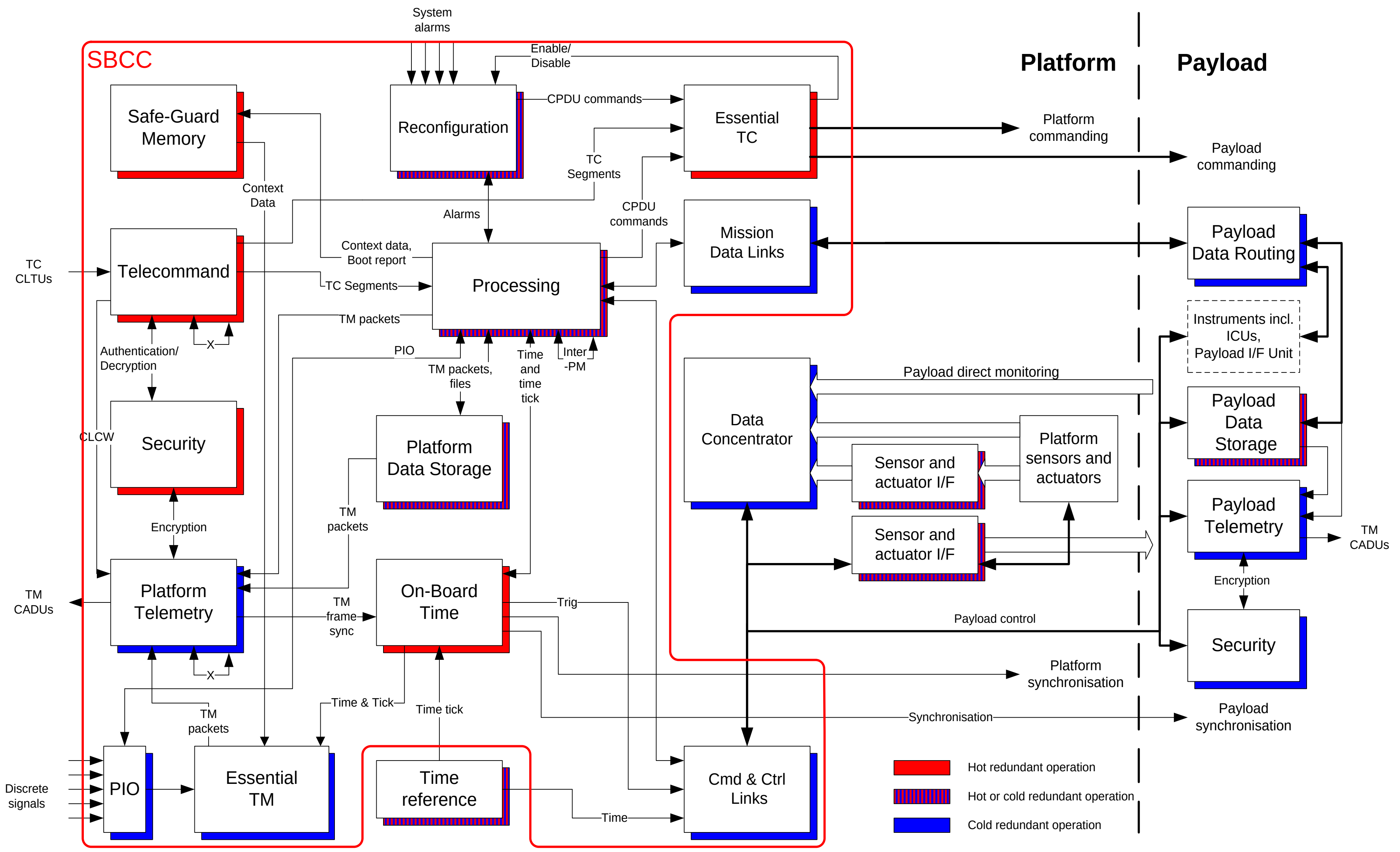
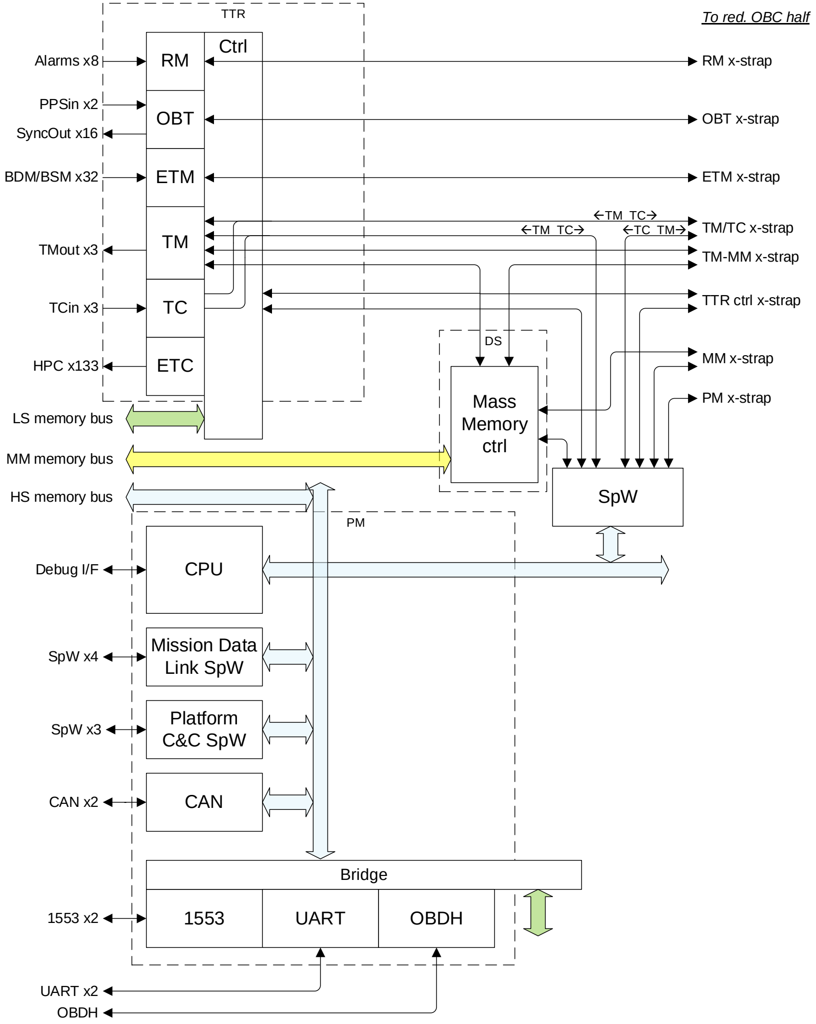


Red perimeter shows what is implemented in SBCC.

CREOLE ASIC SoC

- CREOLE implemented in the rad-hard ATMX150RHA technology, CCGA-896 pin package
  - LEON processor
  - SpaceWire network for internal communication
  - External links: SpW, 1553, CAN, UART
  - Telemetry, Telecommand and Reconfiguration
  - On-Board Time
  - NAND Flash Memory controller with CFDP support

- Implementation validated and SEE radiation effects tested with successful results.



Software

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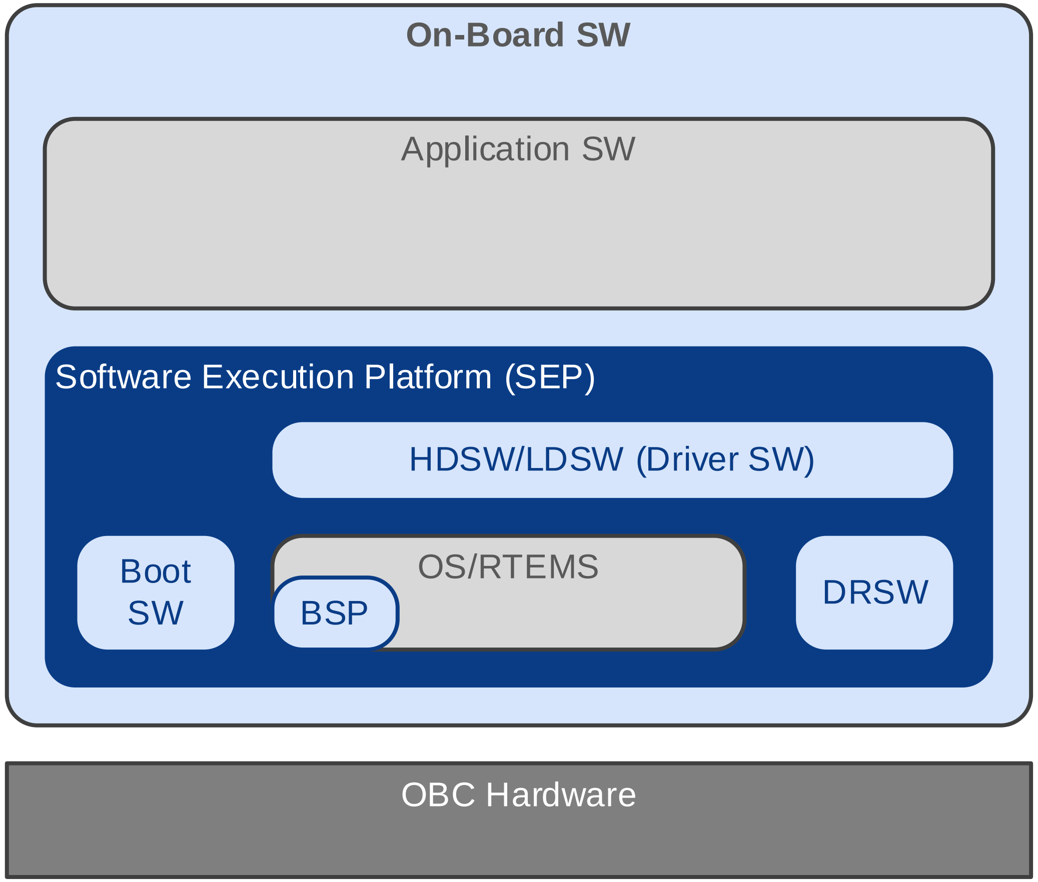
- Boot Software upgraded with support for SBCC/CREOLE.
- Low-level Driver Software (LDSW) was developed to be backward compatible with previous generation as far as possible.
- Hardware Driver Software (HDSW) provides the interface to the application and uses LDSW to access the hardware resources. (finalized in other activity)

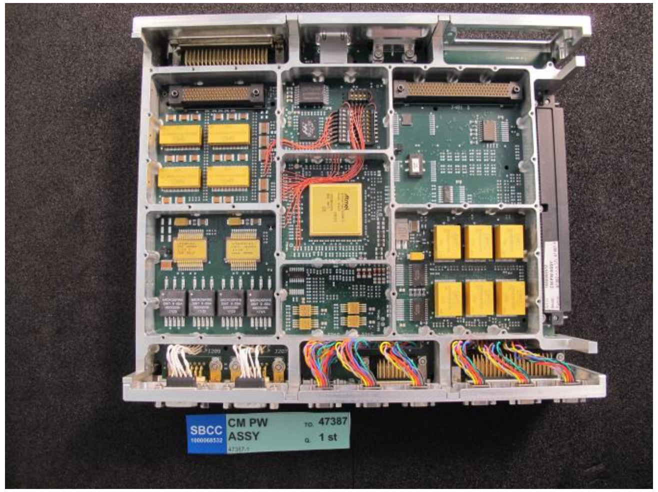


OBC-NG hardware

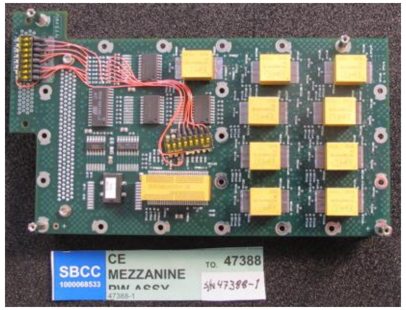
- Breadboard module was manufactured for the three different boards.
- Design later updated for EQM and Flight models.

- Core Module (CM)
  - CREOLE ASIC
  - OBC external interfaces
    - SpW, 1553, CAN, UART
    - TM/TC, Alarm inputs
  - CE Mezzanine with memories for Boot + SW image storage, Safe-Guard Memory (SGM)

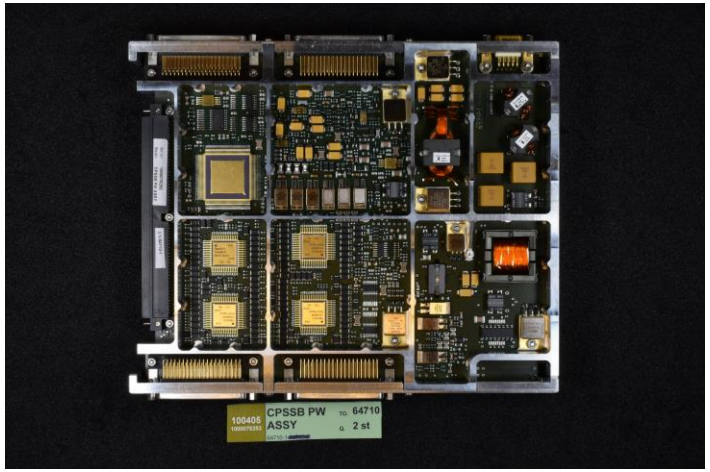
- Core Power Supply (CPS)
  - DC/DC
  - High Priority Commands (HPC)
  - Sync Pulses, Essential TM inputs



Core Module (BB)



CE Mezzanine (BB)



CPS(BB)

Verification/Validation

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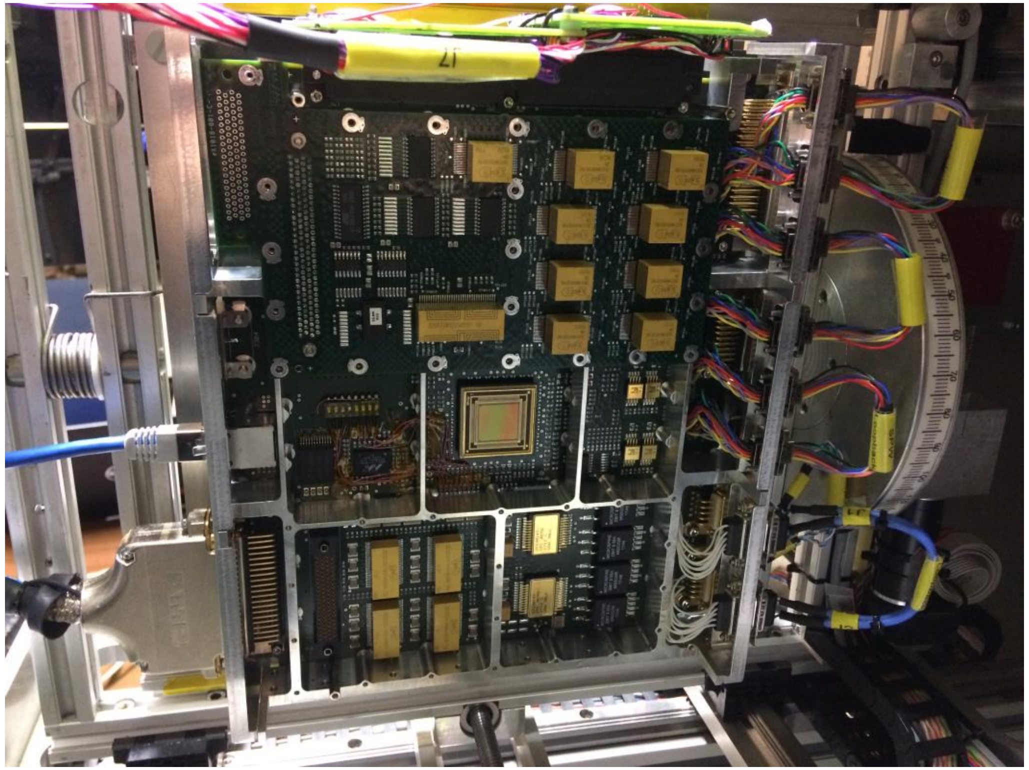
- The OBC breadboard was used for
  - CREOLE ASIC validation
  - Test system performance
  - Test system performance with with a high performant Application Processor (GR740)
- The CM BB was also used for SEE testing
  - Executing representative application test SW with scenario covering all CREOLE blocks
  - Good match between SEE rate result from test and earlier analysed SEE rate



CM BB module mounted in the radiation test fixture at UCL, Belgium

Qualification and Flight Projects

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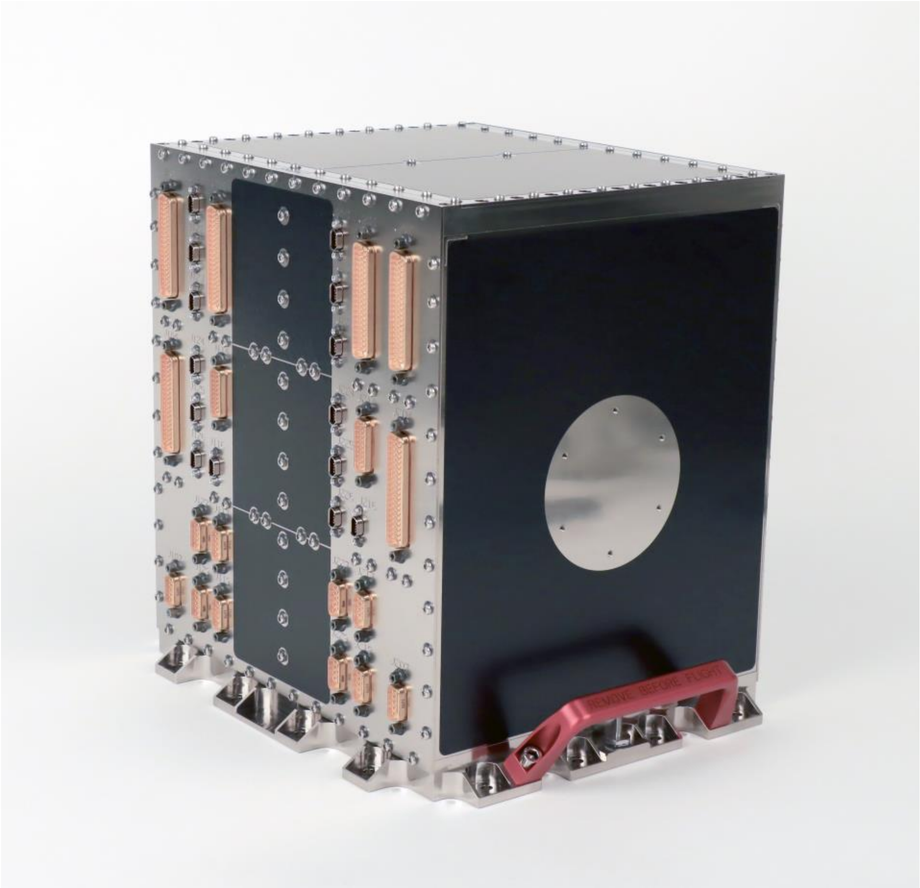
- OBC NG EQM unit built within BGS internally funded study for qualification of new mechanical concept.

- This design used by follow-on flight projects:
  – PLATO OBCM – EM unit delivered
  – CO2M OBC – PFM unit delivered
  – ARIEL OBC – recently started



OBC-NG EQM

Future Expansions and Upgrades

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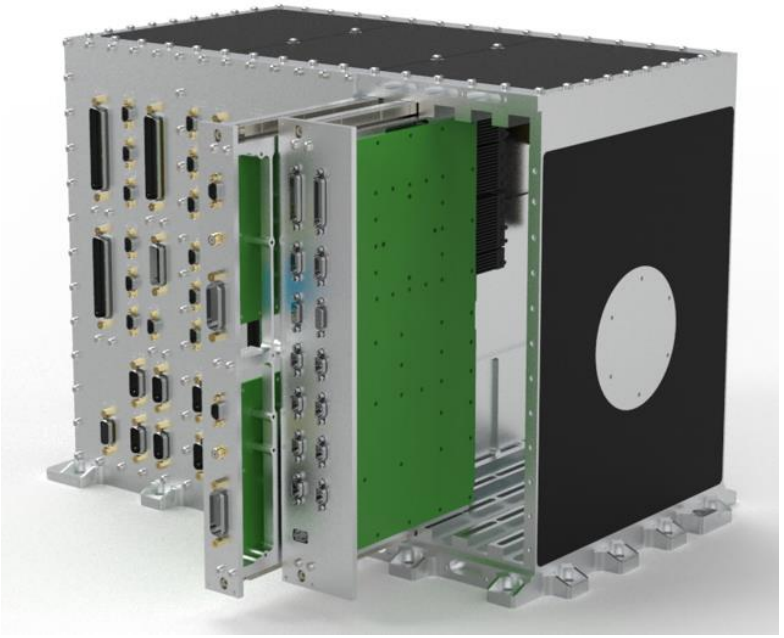
- There are plans to replace the two available expansion slots with ADHA compatible slots
  - 2-4 ADHA peripheral slots
  - CREOLE-based OBC core modules will remain intact
- Will enable the use of new ADHA modules while maintaining the optimized CREOLE-based OBC core.



OBC-NG CAD model with core modules (CPS+CM) to the left and 4 ADHA slots to the right.

Thanks for listening!