SITAEL
AN ANGEL COMPANY

APSOC: RECONFIGURABLE SOC-BASED OBC FOR FUTURE TELECOM APPLICATIONS

Alessandro Avanzi

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Introduction

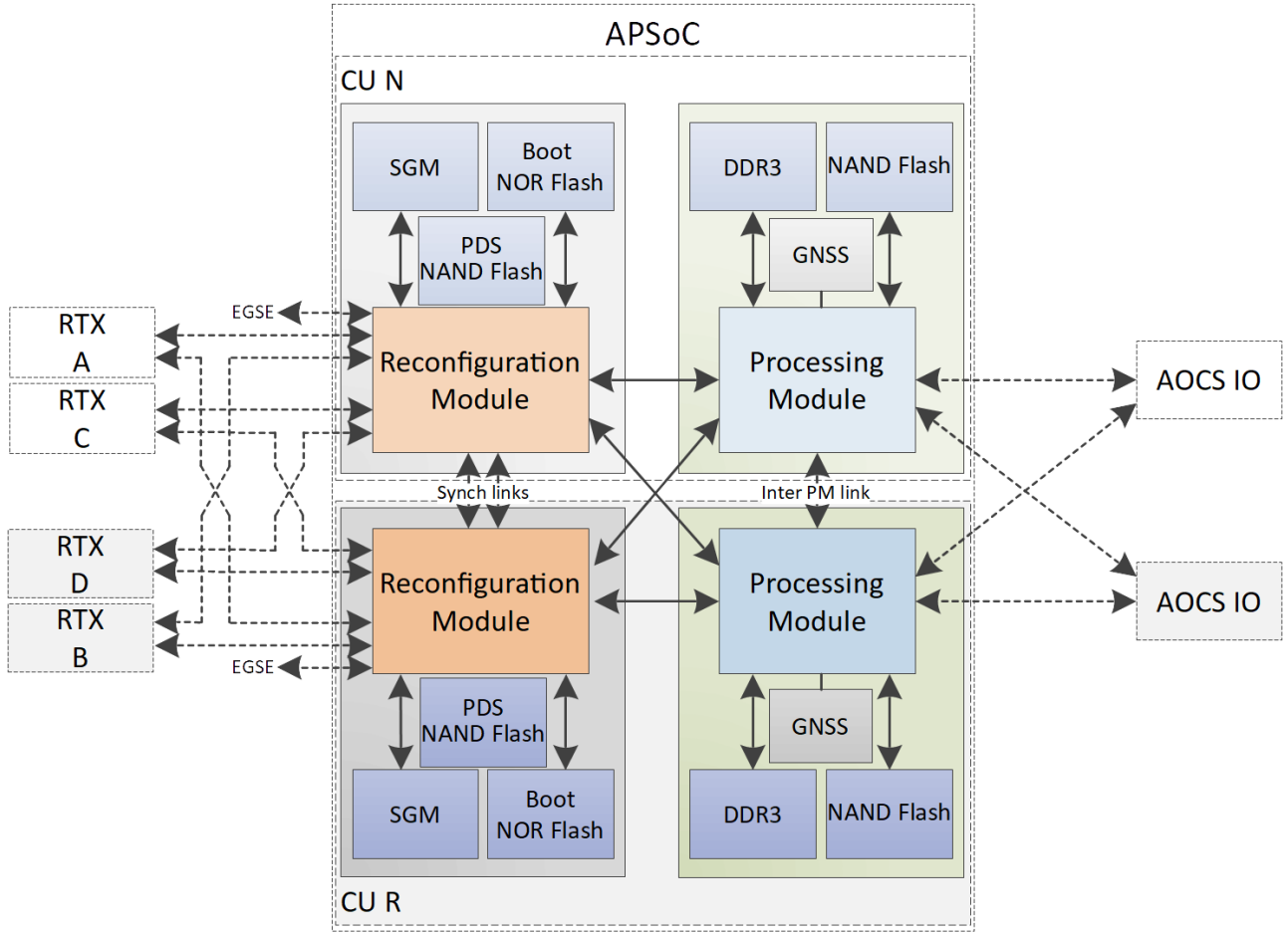
- SITAEL is developing an On-board Computer (OBC) in the framework of the ARTES Advanced Technology (AT) program, in collaboration with esc Aerospace (Czech Republic).
- The present paper describes the activity preliminary results, the key design factors, the architectural design, the mechanical design and the way foreword.
- The unit is intended to serve as the core of future platform avionics for telecom applications, with strong drive towards the use on small satellites (up to 200kg).
- The program is currently running, the presented status corresponds to the results of the PDR. CDR is about to come, before the end of the year. The final objective is the manufacturing and functional testing of a DM model.

Key design factors

- Unit specifications derived from SAVOIR Generic OBC specifications, complemented with SITAEL internal heritage.
- Strong drive on mass and volume optimization, by means of functions integration in large FPGAs and SoC.
- Architecture modularity and scalability, to make it adaptable to different mission needs, even outside of the Telecom applications.
- Based on the cPCI Serial Space, implemented with special care to size of the target platform (some of the ADHA design choices are considered, but ADHA specs are not applicable).
- Targretin mixed use of COTS and qualified components (although the first DM is completely COTS based expect for SGM, as it will be functionally tested only).
- Simple implementation, minimal use of the cPCI Serial Space concept to what is essentially needed.

Architectural design

- Two Computer Units (called **CU**), each one composed of three modules, realize the OBC. The modules are the Processing Module (**PM**), the Reconfiguration Module (**RM**) and the Power Supply Module (**PSU**).

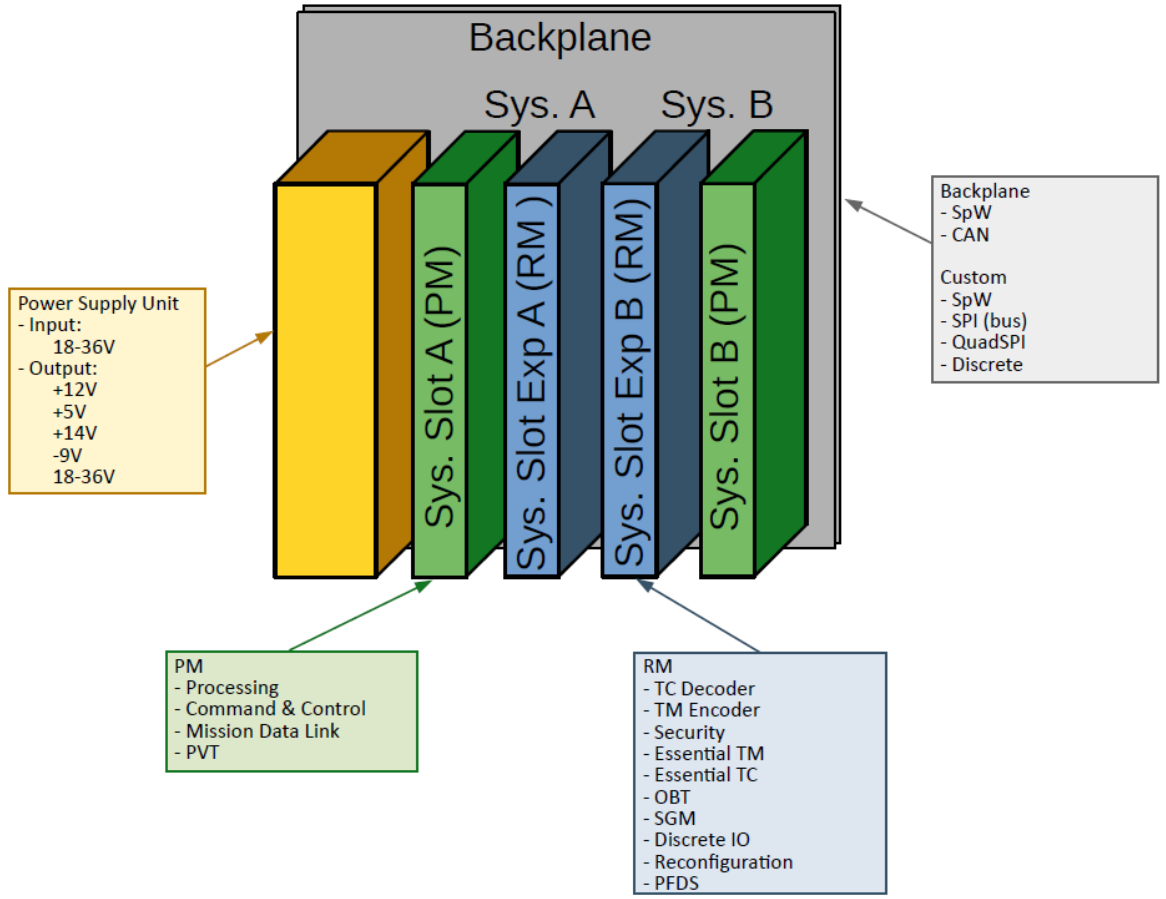


Architectural design

- The PM includes a large SoC (System-on-a-Chip) SRAM-based FPGA with its memories, and the spacecraft Command & Control and Payload links (CAN, SpW). It includes a multi-core processor (Processing function). For the DM model, a Zynq 7000 is selected.
- The RM includes a Flash FPGA with the non-volatile memories, and it is assigned with the OBC critical functions (TC Decoder, TM Encoder, Security, OBT, Essential TM, Essential TC, SGM, PFDS, Reconfiguration, Discrete IO functions). For the DM model, a Polarfire is selected.
- The PSU completes the OBC architecture with EMI filtering, isolated power conversion, power distribution and protections against over-voltages and over-currents at unit level.

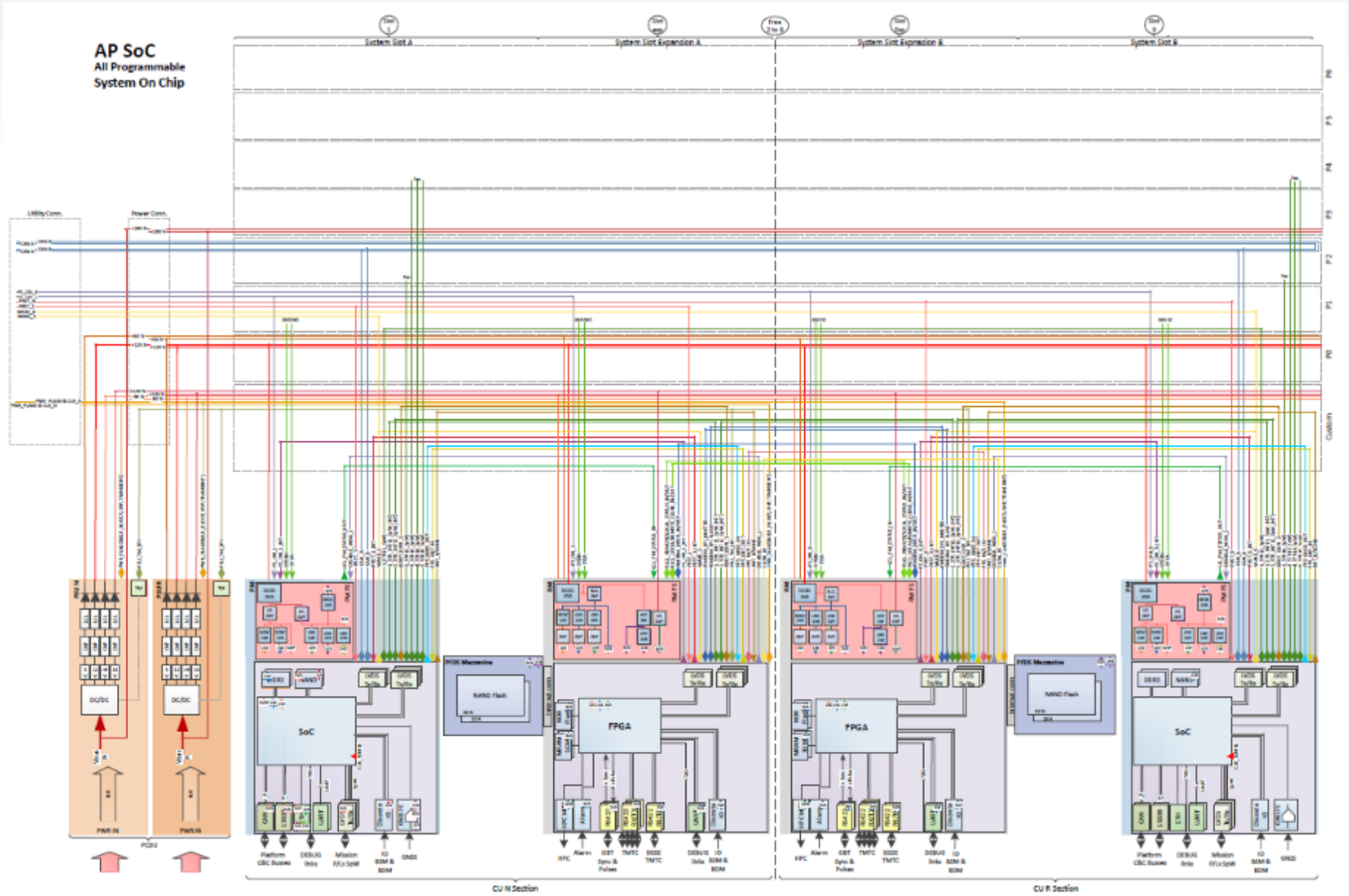
- Internal Links
  - RM to RM: Each RM is equipped with a master and a slave SPI interface towards the other RM. Each SPI interface link is implemented as 4 single ended lines. The bitrate is 1-10Mbit/s. In addition, 2 Discrete IO between RMs are implemented to be used as Heartbeat signsls.
  - PM to active RM (Direct): The PM accesses the active RM registers space by means of a SpW link, which is implementing Direct Memory Access (DMA) access to the RM Platform Data Storage (PFDS) (Low-voltage differential signaling, LVDS, 4 lines, 200Mbit/s).
  - PM to the local RM: Dedicated direct quad-SPI link implemented as 6 lines (CS + Clk + DQ[3:0]), to be used for PM boot and logic programming.
  - PM to standby RM (cross-strapped): The PM accesses the standby RM registers space by means of a SpW link, which is implementing DMA access to the RM PFDS (single ended 4 lines, 200Mbit/s).
  - PM to PM: a SpW link with Remote Memory Access Protocol (RMAP) is planned as inter-PM Link (single ended 4 lines, 200Mbit/s).

Architectural design



- The **System Slot** is assigned to the **CU**, the combination of the RM and the PM modules. From a functional point of view, they behave as a unique system slot, and the connection between them is implemented with custom connectors, leaving the cPCI backplane free for the peripherals.
- The **Peripheral Slot** is not assigned, as this role is reserved for future possible expansions.

Architectural design



cPCI Serial Space backplane use

- The PM and RM are located on two separate boards, connected by means of a backplane custom connector. The backplane power distribution follows the standard +5V and +12V but is expanded to provide redundant power distribution and unregulated power distribution +28V (with dedicated ground). In addition, the following connections from the standard are used:
  - #PS_ON signal, routed to the backplane Utility connector.
  - #WAKE signal, routed to the backplane Utility connector, and additionally used by the PM to signal the RM that the unit is alive.
  - #PRST signal, routed to the backplane Utility connector.
  - SYSEN and SYSA used for physical slot addressing.
  - CAN bus Nominal and Redundant, additionally routed to the backplane Utility connector.
  - Dual Star Serial Interconnect used as follows:
    - 1_STR to 1_STR for PM Nominal to PM Redundant data interlink (SpW).
    - From 2_STR to 5_STR implemented from each PM module as expansions for future peripheral slots (SpW).

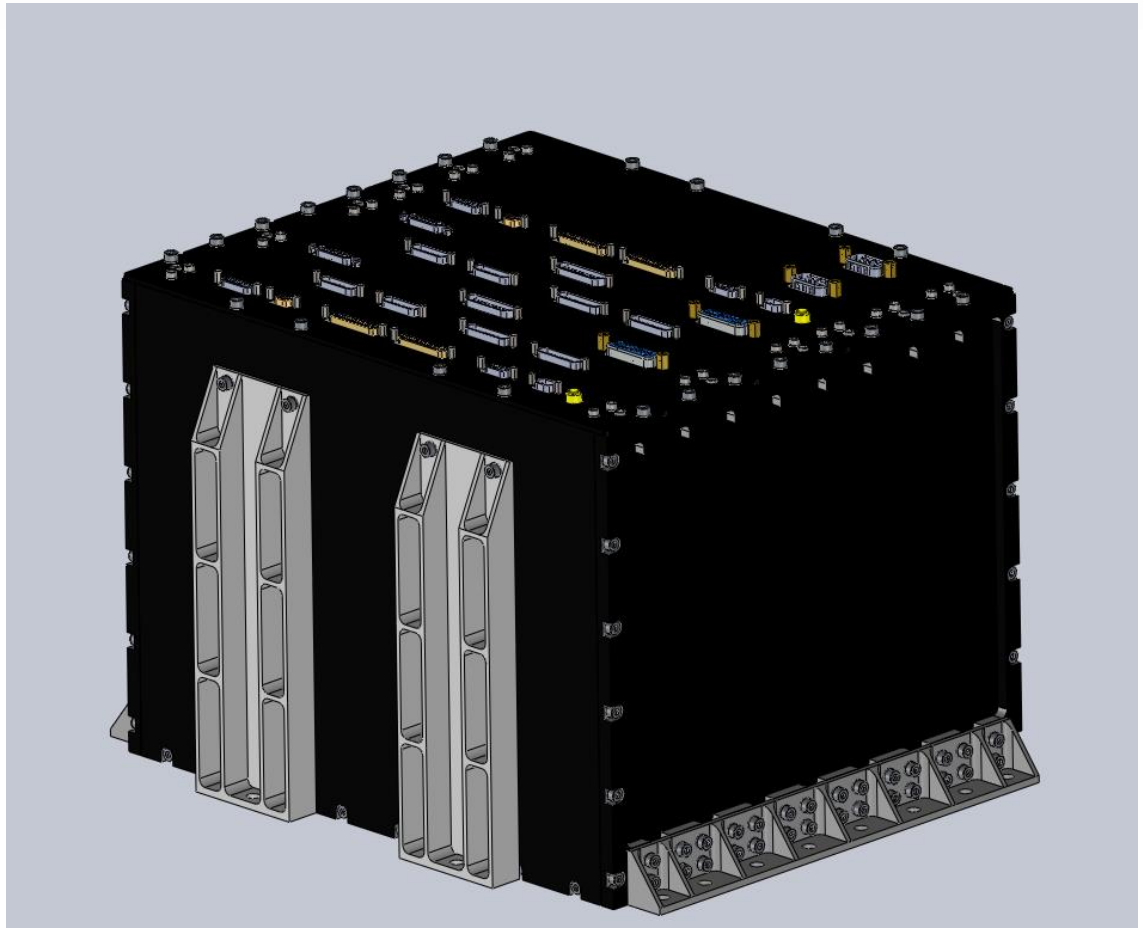
cPCI Serial Space Backplane use

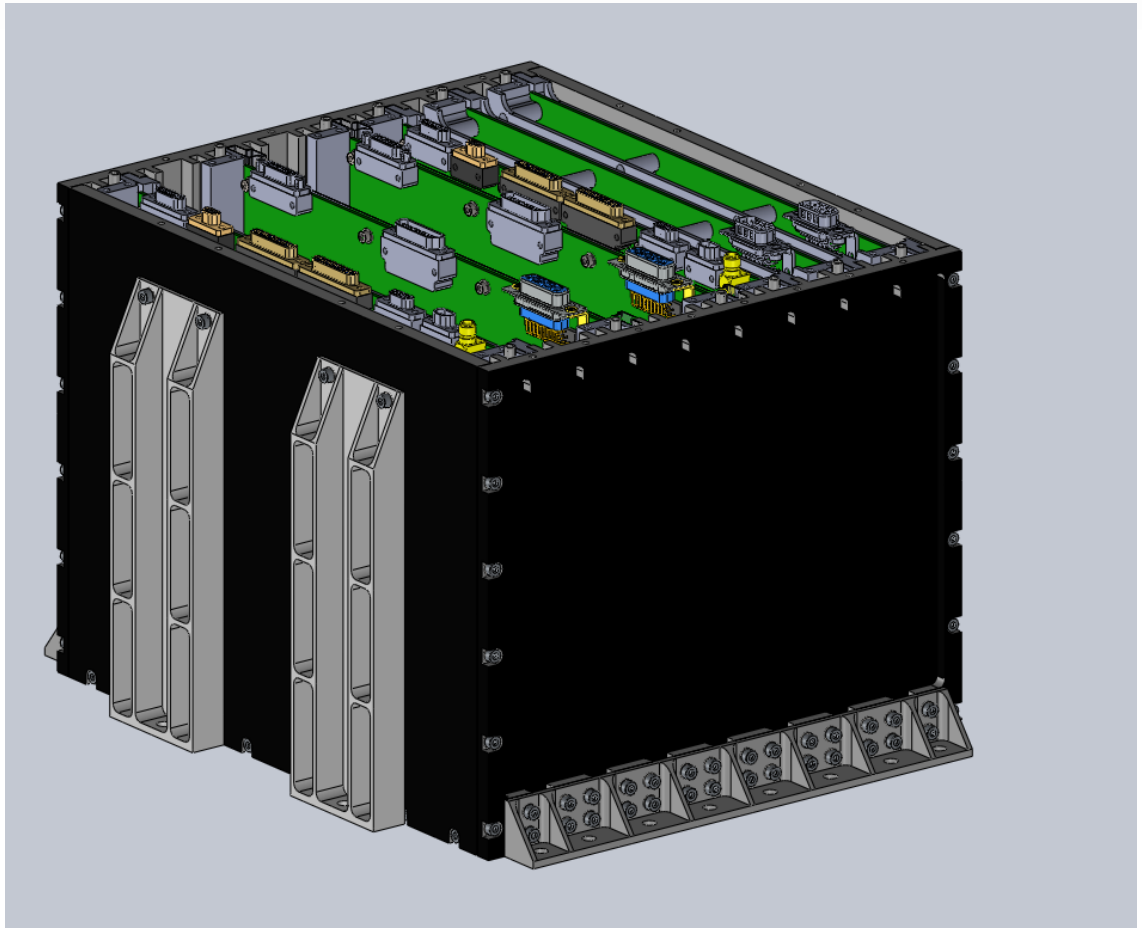
- In addition, a custom connector is implemented for:
  - Fully cross-strapped SpW between the PM and RM modules.
  - Boot Quad serial peripheral interface (QSPI) from PM to RM plus DONE line to signal successful boot operations.
  - PSU to RM SPI for PSU Telemetry acquisition (with the RM as a SPI Master).
  - PSU to RM Discrete singles to control OVC and OVV protections (cross-strapped)
  - RM to RM dual SPI.
  - RM to RM CLCW remote routing.
  - RM to PM watchdog disable signal.
  - RM to PM reset signal.
  - RM to PM PPS for Master/Slave OBT sync.
  - RM to PM PPS for Processing sync.
  - PM to RM PPS for OBT sync to GNSS.

External Interfaces (each CU)

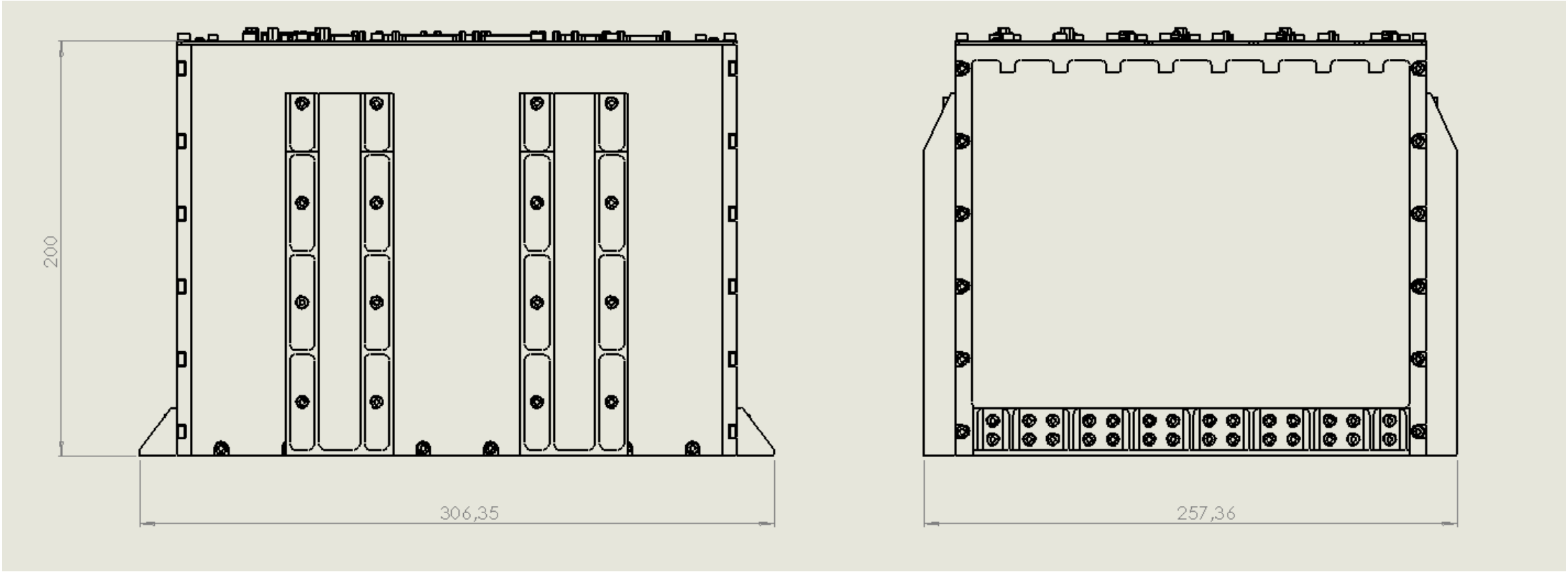
- 1 x Power Input (18-36V @ up to 80W).
- 2 x CAN bus (Nominal and Redundant) (up to 1Mbps).
- 6 x Payload Interfaces, of type SpW (up to 200Mbps).
- 8 x Discrete IO Inputs dedicated to the SoC FPGA (PMF), composed of:
  - 4 Inputs of type BSM (Contact Closure).
  - 4 Inputs of type BDM (Bi-Level Discrete Monitor).
- 1 x GNSS Signal Inputs.
- 1 x Debug Interface dedicated to the SoC FPGA (PMF), composed of:
  - JTAG.
  - 2 x Universal Asynchronous Receiver-Transmitter, UART, (TTL 8N1 115200 bps).
  - Ethernet.
- 4 x TC acquisition link, each composed of:
  - TC Data (RS422 @ 64000 bps).
  - TC Clock (RS422 @ 64000 bps).
  - TC Data Valid (RS422 active high, signals valid data after successful acquisition).
  - TC Lock Signal (RS422 active high, used to define the CLCW NoRF Flag).
- 4 x TM transmission link, each composed of:
  - TM Data (RS422 @ up to 10240 Kbps).
  - TM Clock (RS422 @ up to 10240 Kbps).
- 1 x EGSE TC Link
- 1 x EGSE TM Link
- 12 x Alarm Inputs, composed of:
  - 3 Inputs of type BSM (Contact Closure, generally used for separation straps);
  - 9 Inputs of type BDM (Bi-Level Discrete Monitor);
- 32 x HPC Outputs of type LV-HPC (HV-HPC Optional).
- 2 x OBT Synchronization Inputs (Nominal and Redundant), of type SDI (RS422).
- 8 x OBT Synchronization Outputs, of type SDI (RS422 @ 1Hz).
- 8 x Discrete IO Inputs dedicated to the Reconf. FPGA (RMF), composed of:
  - 4 Inputs of type BSM (Contact Closure).
  - 4 Inputs of type BDM (Bi-Level Discrete Monitor).
- 1 x Debug interface dedicated to the Reconf. FPGA (RMF), composed of:
  - JTAG.
  - 2 x UART (TTL 8N1 115200 bps).

Mechanical Layout





Mechanical Layout



Mechanical layout

- 6U cPCI Serial Space configuration
  - 5HP for the modules, 6HP for the power supply
  - No violation of the cPCI PCB dimensions, which are kept at minimum suggested by the standard
- 6U selected because:
  - Fitting all required connectors is problematic in the 3U standard (even in the 6U some compromises were taken)
  - Architecture implies functions redundancy concept, segregation and cross strapping which was not possible to implement with a 3U PCB.
  - Note that each module (PM and RM) implements
    - Local power conversion (POL and linear)
    - Local protection for OVC (RLCL for the RM and LCL for the PM) and OVV
- PCB already pre-placed and they fit the 6U dimension (PFDS implemented as a daughter board)

Preliminary budgets and way foreword

- Volume: 306 x 257 x 200 mm
- Mass: 12 kg (preliminary estimation, the box only is about 5kg)
- Power: PSU designed for a mean power provision of about 35W, peak power of about 80W.
- RM PFDS is 1.5 Tbit (Flash SEC DEC EDAC protected)
- RM SGM is 2 x 8 Mbit (3DPlus MRAM in N+R configuration)
- RM first-level boot memory is 3 x 256 Mbit (NOR in TMR with power down control)
- CPU is a dual core ARM Cortex-A9 at 2.5 DMIPS/MHz (lowest speed grade is about 667 MHz)
- PM volatile memory is 256 Mbit (DDR2 SDRAM SEC DEC EDAC protected)

CDR before end of 2023, first DM prototype in 2024.

Thank you