ESA EDHPC 2023
OBC-Ultra, the rad-hard NG-Ultra-based On Board Computer for future applications

5th October 2023 at Juan Les Pins

DEFENCE AND SPACE

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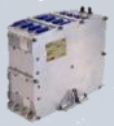
Space Electronics key figures & facts



450
France workforce

> 1200 boards /y
> 150 unit /y

150 M€
Revenues
40% export

Space Agencies

Start-up, medium & big size companies

Institutions and Defence Agencies

Satellite Operators

Governments, institutional and enterprises from multiple areas/ fields

1st

Worldwide Leader

> 60 M€ Export
Order Intake in 2022

Spacecraft Electronic Unit Supplier

Elancourt

Toulouse

Our Ambition

Be worldwide Electronics and Sensors / Actuators reference for Space

Master New Space & Conventional Space solutions from design and technologies, up to manufacturing & test processes

Pioneer and qualify space technologies for future spacecrafts, launchers & space systems

Be attractive for talents by offering key competences acquisition and efficient collective knowledge management

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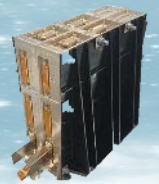
Space Electronics reliable & large unit portfolio

Electric Propulsion

Power Distribution & Regulation

Power & Propulsion Units

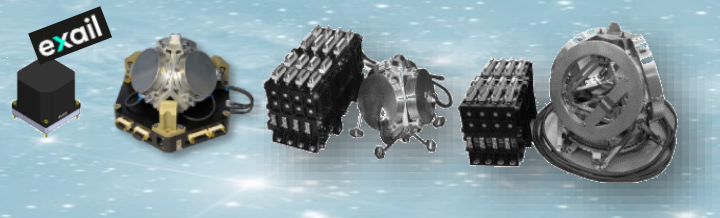
On-board Computers



Security

Payload Data Handling

Platform & Payload Processing Units



Fiber Optic Gyroscopes

Control Moment Gryroscope

Sensors & Actuators

www.airbus.com/en/products-services/space/equipment

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Summary

- Introduction
- Key points
  - A generic product for multiple applications
  - Modular Approach as a key driver
  - Main functions of the OBC-Ultra
  - Radiation Hardened
- Conclusion

Introduction

- **OBC-Ultra** is a modular **O**n **B**oard **C**omputer developed by Airbus DS
  - Strategic for European non-dependence & competitiveness
  - Based on **NG-Ultra** component from NanoXplore

- **NG-Ultra** is very **well fit for OBC** applications
  - Large reprogrammable FPGA matrix to implement OBC functions
  - Plenty of processing performance to cover different types of missions
  - High robustness to radiations

- **OBC-Ultra** benefits from **ADS experience on NG-Ultra**
  - H2020 DAHLIA & OPERA, ESA GSTP, Internal R&D MYTIKAS…

- For this OBC, Airbus DS has built a **comprehensive framework** to speed up **development time**
  - Generic VHDL libraries
  - Generic SW drivers libraries
  - FPGA Place & Route optimization scripts

An 8-year journey from chip to OBC

NG-ULTRA
component

See Poster

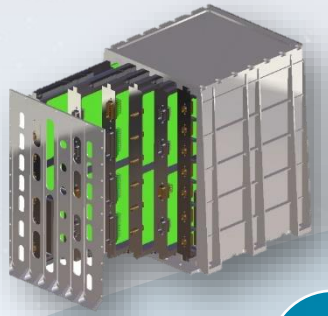
OLYMPE
processing board

See OLYMPE presentation

MYTIKAS
processing building block

See Poster

See POLLUX presentation (secondary power generation)



OBC-ULTRA
Engineering Model + Flight Model

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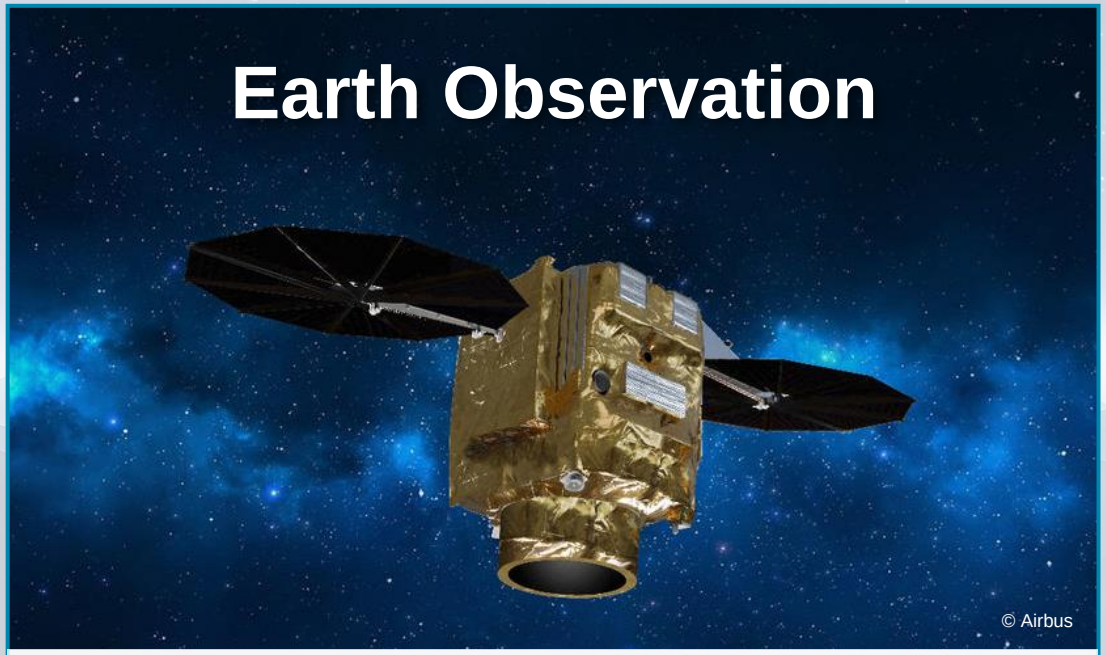
Generic product for cross business applications

Only one OBC-Ultra product to replace several previous generation of OBCs



1st version of OBC-Ultra
- EM mid 2024, followed by FM

Updated version of OBC-Ultra
- FPGA design and SW functions updates
- New boards based on OBC-Ultra modular approach

Genericity allows to reduce time to market and NREC cost

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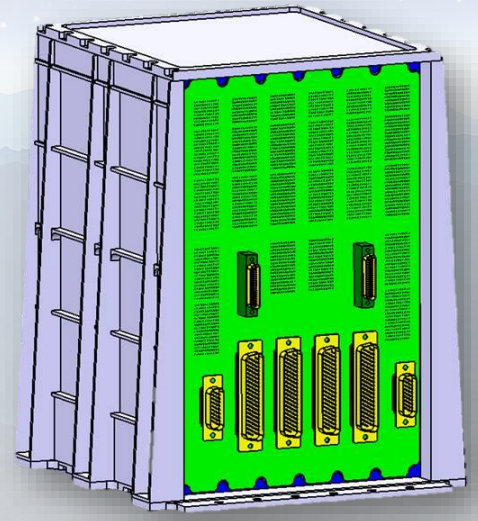
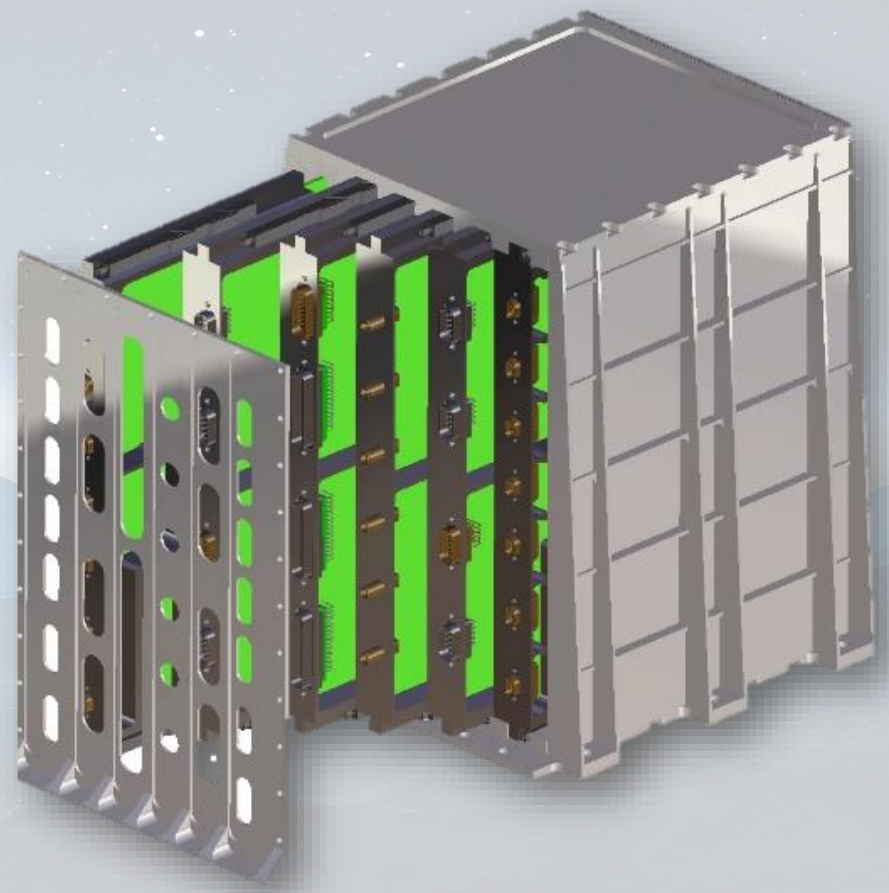
Modular Approach as a key driver

- Architecture based on a rack system, **ADHA compatibility**
- External **I/O connectors** only on front and rear sides
- Boards form factor = **VPX 6U extended** depth standard
- **Fully redounded** boards to be robust to single failure





Modularity & alignment on industrial standards for efficiency and sustainability

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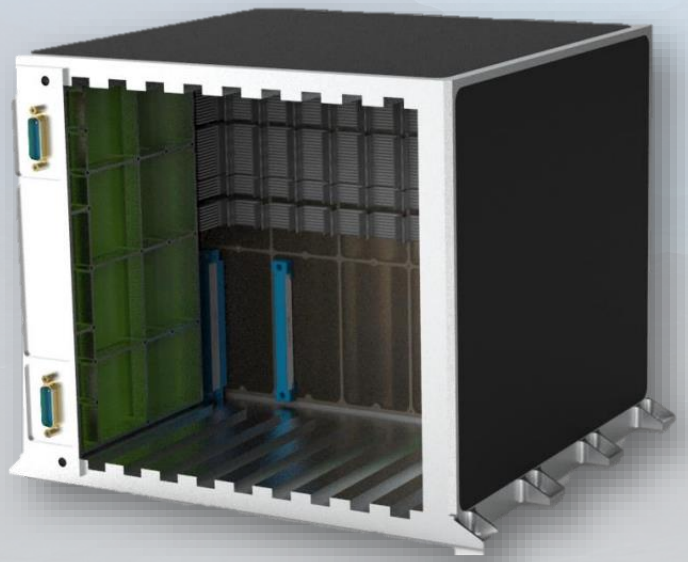
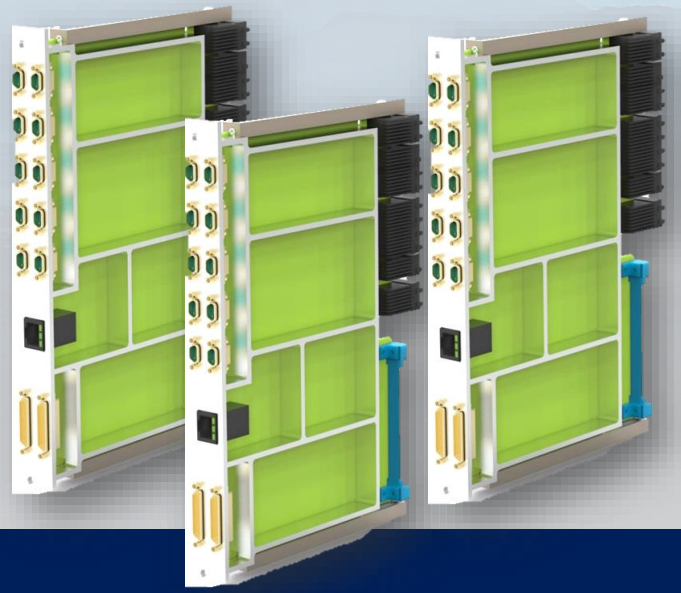
What is ADHA?

- **ESA initiative** to reduce cost and development time (consortium Airbus DS, TAS, Beyond Gravity)
- Objective in 2025 = deliver a new generation of **Platform** and **Payload Data Handling units**
  - OBC-Ultra covers the Platform Data Handling needs
- Based on standardized modules, inter-operable, inter-changeable

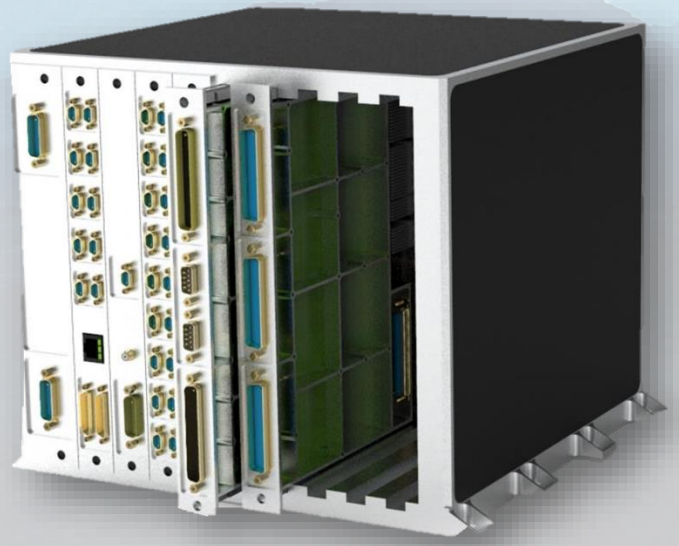
Standardized ADHA rack



Modules from different suppliers



Standardized ADHA unit



Pictures from ADCSS – ESTEC 22 October 2020

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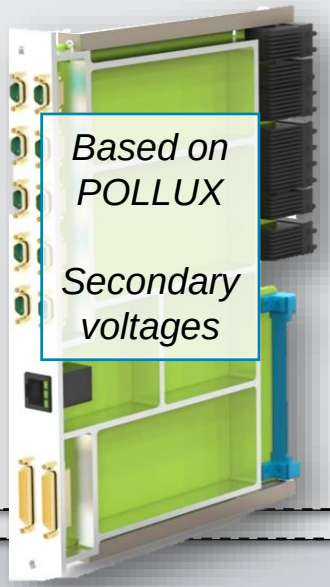
Baseline & Extended Versions

Baseline Version

Power Board



Based on POLLUX

Secondary voltages

Processing Board

Based on NG-Ultra

Functions in FPGA + SW

Companion Board

Based on Ultra-300

Functions in FPGA only

Extended Version

GNSS Board

High Perf Board

GNSS features

Telecom Board

Increase nb of TM/TC chains from 1 to 3

ADS design

The 2 additional boards can be customized to meet specific user needs

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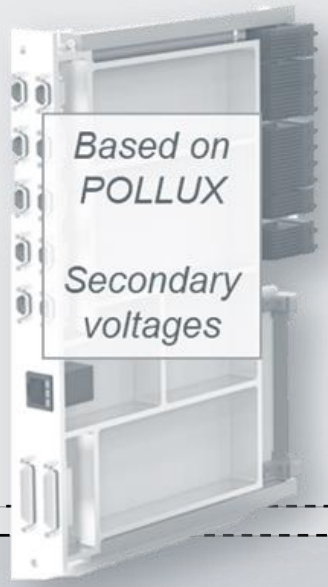
Focus on Processing board & Companion board

Baseline Version

Power Board



Processing Board

Companion Board

Extended Version

GNSS Board

Telecom Board

Unprecedented level of integration with these 2 boards designed for decades

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Processing Board

- **The OBC-Ultra implements the following SW-dependent functions typical of an OBC**
  - TM/TC chain supporting data rate up to 20Mbps + several encoding possibilities
  - Support of TM CCSDS File Delivery Protocol (CFDP)
  - Commonly used communication protocols: SPW, CAN, 1553, RS485, UART
  - On Board Time (OBT) based on ESA CUC core, temperature-insensitive through SW algorithm
- **The OBC-Ultra is based on high speed DDR4**
  - 100Gbps bandwidth
  - Optimal sharing of DDR4 access between SW and FPGA can be reached by user configuration
  - Compatible with needs of OBC increasing performances expected for missions of the next decades
  - Very high level of robustness against radiation effects
- **On a first step targeting single core ARM application, the OBC-Ultra will implement multi-core applications SW for missions with specific needs**

HW autonomous critical functions

Companion Board

- **The OBC-Ultra implements also the following HW autonomous functions typical of an OBC**
  - Reconfiguration Module
  - Essential TC Module
  - Essential TM Module (Housekeeping)
- **These 3 VHDL modules are implemented on the Ultra-300 FPGA of the Companion board**
  - No NG-Ultra boot sequence involving in its very first step the execution of the Boot Loader firmware
    ➔ No need to carry out additional FDIR analysis
  - Easiest way to ensure compliance with **SAVOIR requirements** of critical functions being SW independent

Critical functions are SW independant

OBC-Ultra Security

- **Securing end-to-end communications between ground and spacecraft is:**
  - An important matter for the OBC which manages TM/TC links
  - Strategic for security of current and future space missions

- **OBC-Ultra** is compatible with **all possible security modes** depending on final user needs**:**
  - **Internal security mode** supporting:
    - Latest Space Data Link Security (SDLS) Extended Procedures standard
    - Multi-users
  - **External security mode** for OBC-Ultra interfaced with external in band security equipment
  - **Bypass security mode** for OBC-Ultra interfaced with external out of band security equipment

The OBC-Ultra can ensure security without need of any additional crypto unit

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Processing Board

- **Implemented NVM allows the OBC-Ultra to be compatible with the following elements:**
  - Overall storage capacity increased compared to previous OBCs
  - SAVOIR (Space AVionics Open Interface aRchitecture) requirements compatibility
  - High SW flexibility with boot possible on different versions of application SW

- **Implemented NVM are:**
  - **<u>Flash NAND 64 GiB</u>**
    - Part of **Static Safe Guard Memory accessible directly by the SW** (and by the ground via SW)
    - Storage of multiple application SW images
    - Offers a highly integrated Mass Memory functionality
  - **<u>MRAM 1 MiB</u>**
    - Part of **Static Safe Guard Memory accessible directly by the ground** (without SW intervention)
    - HW parameters
  - **<u>NOR Flash 16MiB</u>**
    - NG-Ultra bitstream storage

Part of Static SGM *directly* accessible by the ground = OBC compatible with SAVOIR

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OBC-Ultra baseline version will implement 64 GiB Mass Memory

Processing Board

- **This will be achieved through:**
  - Autonomous FPGA modules able to transfer data to/from DDR4/NVM
  - Huge size capacity Flash NAND 64 GiB
  - Functionality 100% implemented on the **Processing board**
- **This functionality is typically needed by science and exploration missions:**
  - Spacecraft cannot communicate with the ground during the whole mission
  - Storage capacity needed for science data and telemetry
  - Implementation inside OBC avoids developing a dedicated computing capacity in another equipment type mass memory

No additional board or additional unit needed

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OBC-Ultra Debug functions

- **Wide range of SW debug possibilities**
  - Debug tools of the SoC environment (UART, JTAG), accessible on closed equipment
  - Real-time Trace, via HSSL protocol Aurora IP from NanoXplore, compatible with Lauterbach debug and trace probe
  - Design For Test (DFT) features to ease testbench and SW developments (possible to use standard interface instead of the very specific CADU interface)

- **FPGA debug through UART interface,** accessible on closed equipment
  - Able to perform read/write accesses on all FPGA registers (for control/command)

- **Equipment debug through high speed Ethernet link 100 Mbps,** accessible on closed equipment **:**
  - Able to perform DDR4 patch/dump

The OBC-Ultra has been designed to offer debug at SW, FPGA & Equipment level

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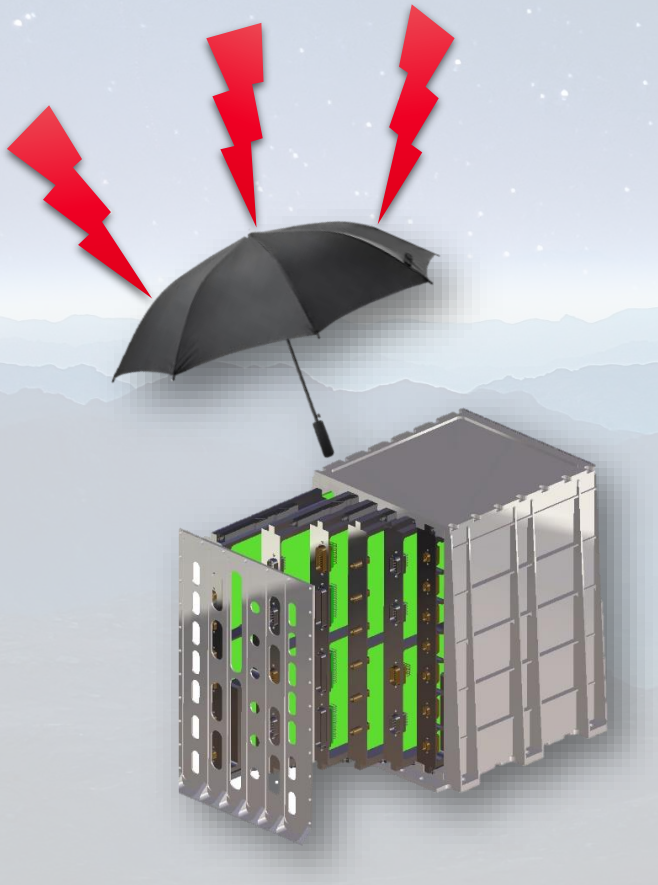
OBC-Ultra is a Rad-Hard equipment

OBC-Ultra radiation hardening considered at all levels: components, design, architecture



- **<u>Components</u> selection**
  - NG-Ultra and Ultra-300 from NanoXplore:
    - Natively rad-hard (STMicro 28nmFDSOI technology)
    - Internal FPGA SRAM configuration memory protected by Integrity Check
  - Other components **mainly in class CQ1** for the first version (OBC-Ultra version EOS)

- **<u>Design</u> techniques for high level of robustness against SEU/SEFI**
  - All NVM managed in triplication mode
  - DDR4 memories protected by strong Reed Solomon error correcting code + scrubbing
  - Internal RAM blocks of FPGA protected by error correcting code + scrubbing

- **<u>Architecture</u> definition**
  - with each board doubled for full redundancy

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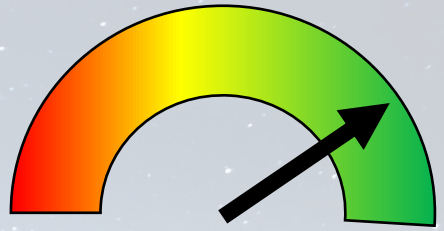
OBC-Ultra Conclusion (1/2)

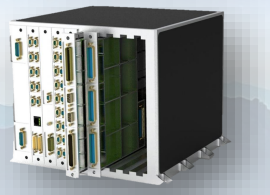
Increased performances compared to previous generations of OBC

- Overall data rate increased
- Number of interfaces increased
- SW performances way higher allowing to target new kind of applications
- Wider range of debug features



+ Data Handling Modularity

- ADHA standard
- Easily customizable for future needs
- Reduction of time to market and NREC cost



+ European strategic non-dependence

- NG-Ultra component
- Ultra-300 component

+ Rad Hard at all levels

- Components selection, Design techniques, Architecture definition

Compatible with Earth observation, Telecom & Navigation, Science & Exploration

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Conclusion (2/2)

OBC-Ultra offers all typical OBC features

- High Performance Processing
- Ground-board TM/TC
- Wide range of standard communication protocols
- Architecture compatible with SAVOIR OBC requirements

+ Flexibility on the recurrent cost

- Design offers scalability on EEE component class quality
- Compatible with telecom constellations

+ Additional features beyond classical OBC perimeter without any additional board

- Internal security module upgraded to the latest standard version
- Mass Memory capacity

Compatible with Earth observation, Telecom & Navigation, Science & Exploration

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Thank you

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