In-Orbit Artificial Intelligence and Machine Learning for Space Applications : Versal Space Reference Design - First Design-In Experiences

Dr. Rajan Bedi
CEO Spacechips
rajan@spacechipsllc.com

The Global Space-Electronics Company

ELEKTRA 2016 WINNER
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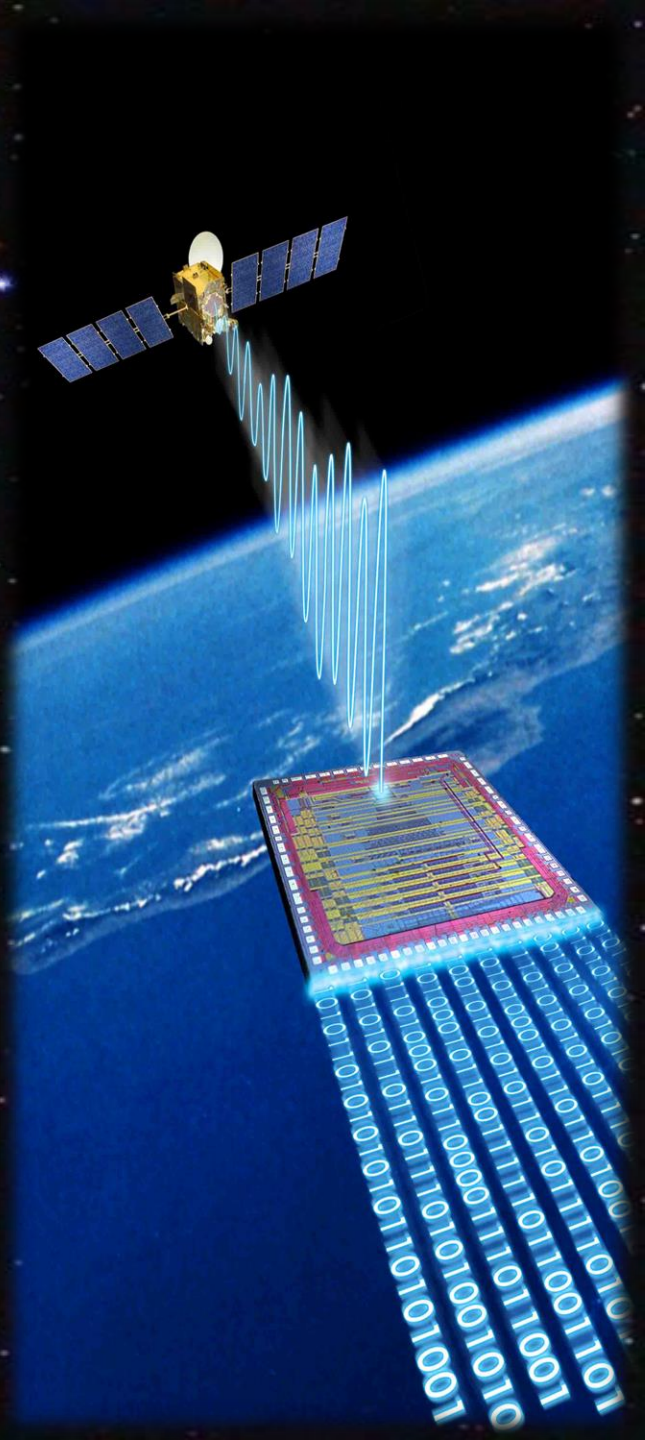
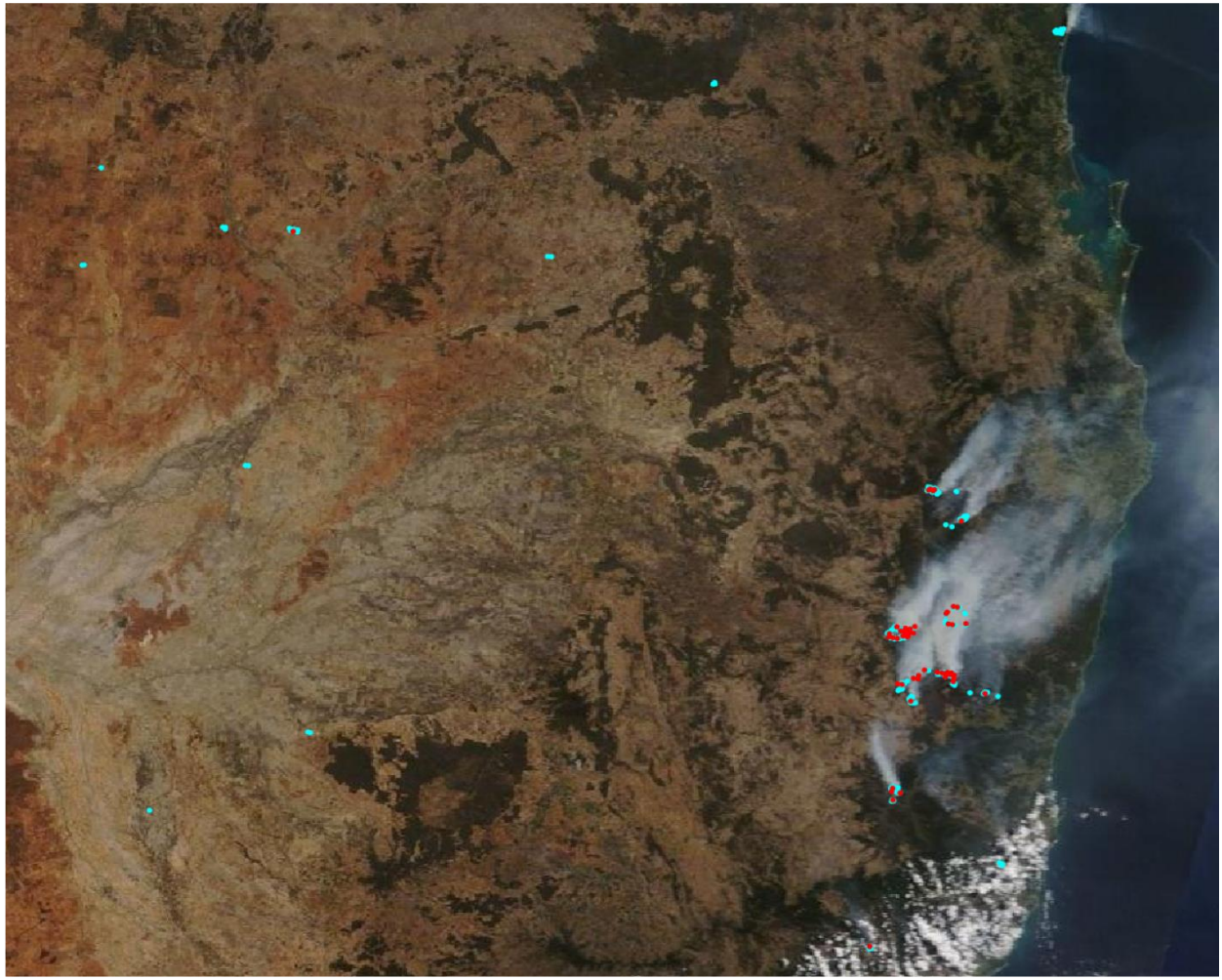
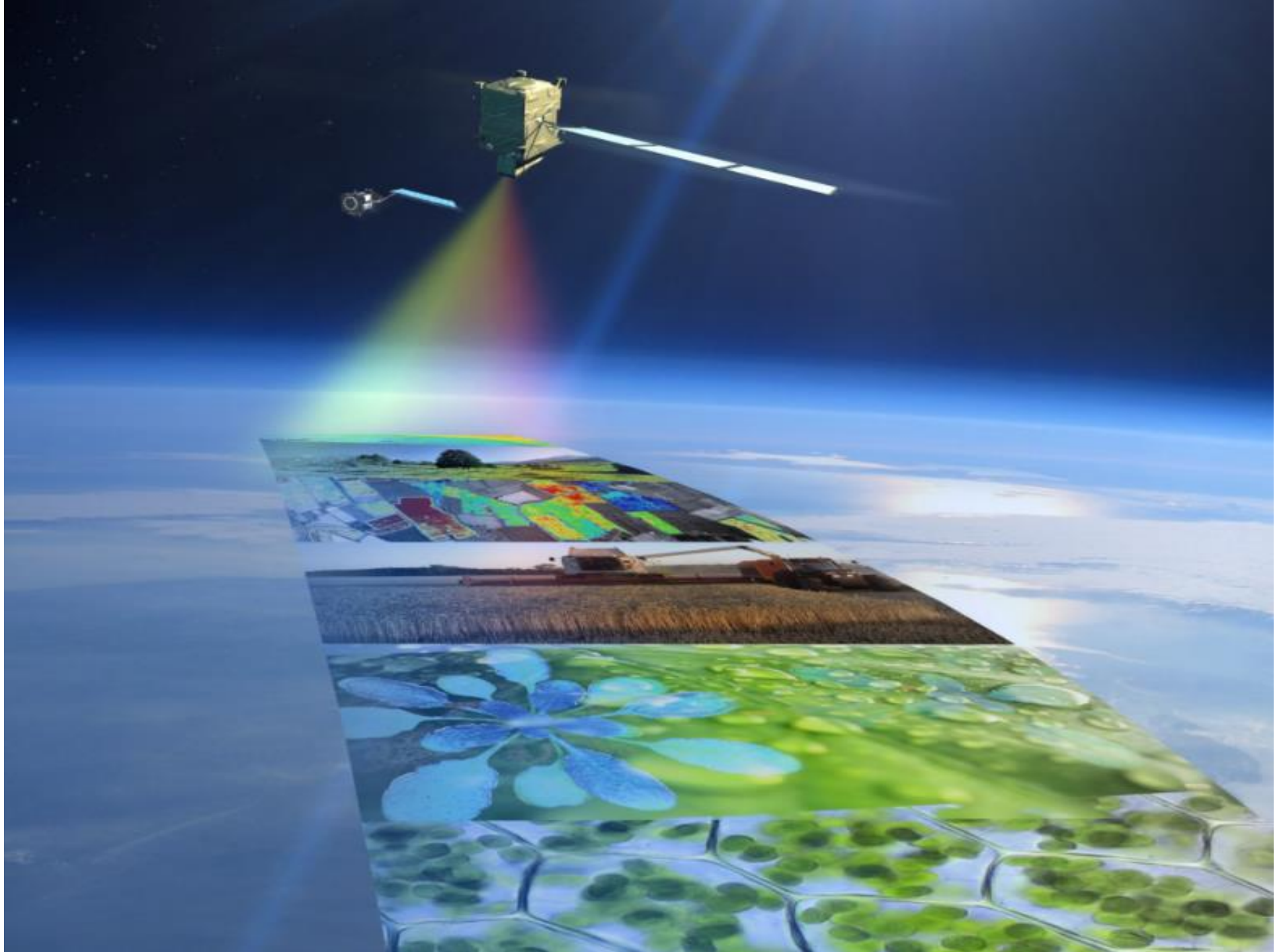
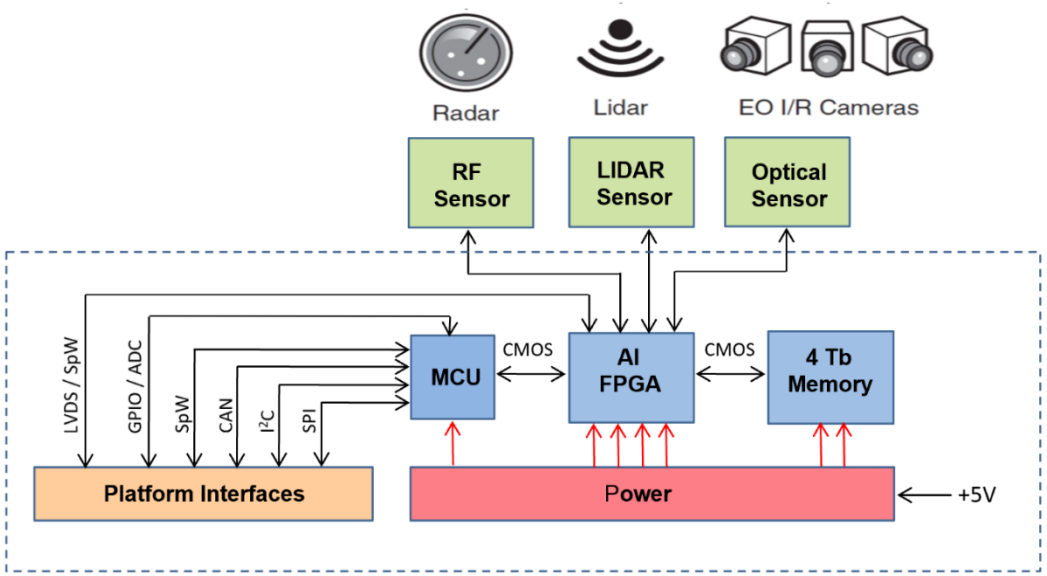
Winner of European Start-Up of 2017 and European High-Reliability Product of 2016, 17 & 18

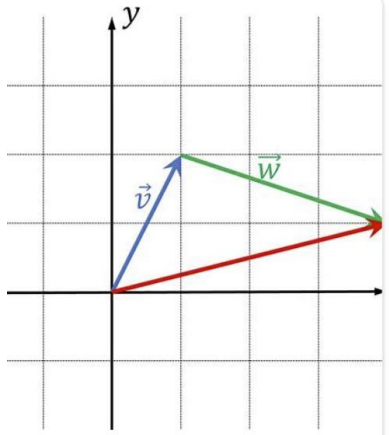


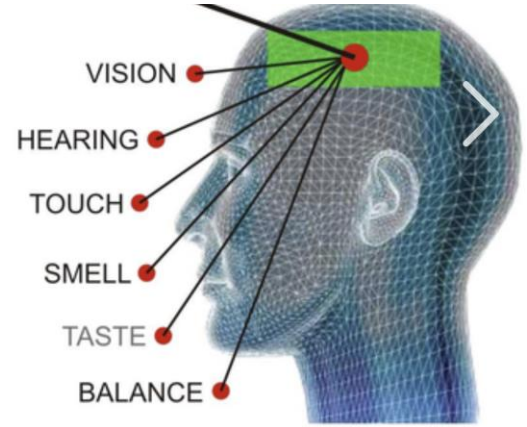


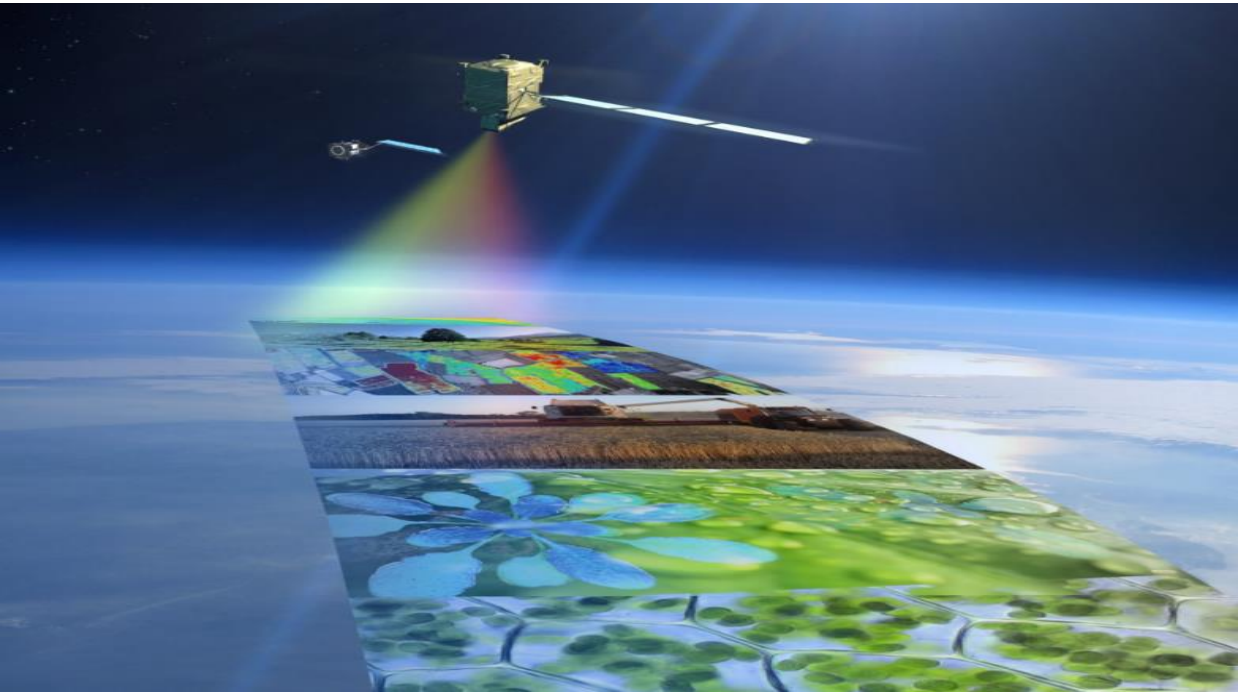


	DDR3 16Gb x 16	NAND 256Gb x 16
Number of Devices	64	4
Minimum Real Estate (mm^3)	152,320	16,796
Power Dissipation (static/dynamic)	17W / 17W	13.2mW / 5.2W
Approximate Cost ($)	650k	30k
Storage Rate, 16-bit bus (Mbytes/s)	2,667	100
Total Byte Writes (TBW)	Unlimited	7530 TB

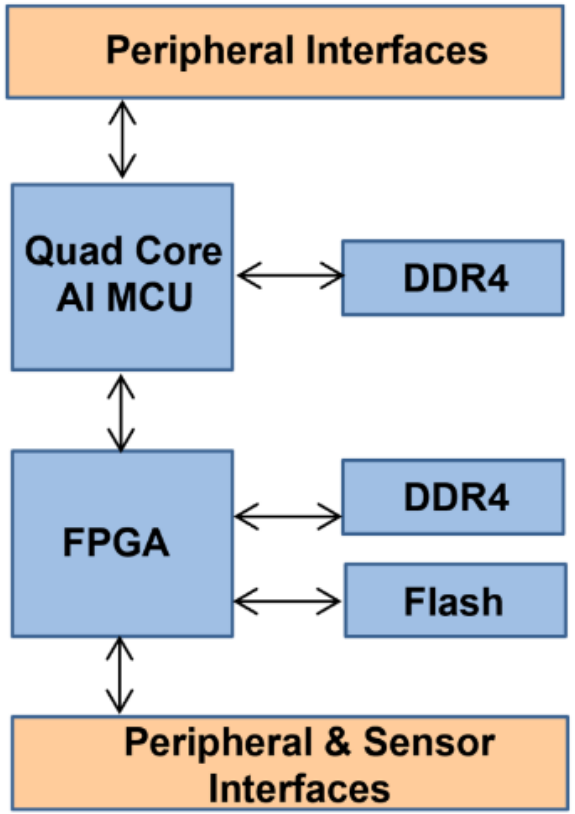








Spacechips Edge 1 : AI-Enabled Edge-Based OBC

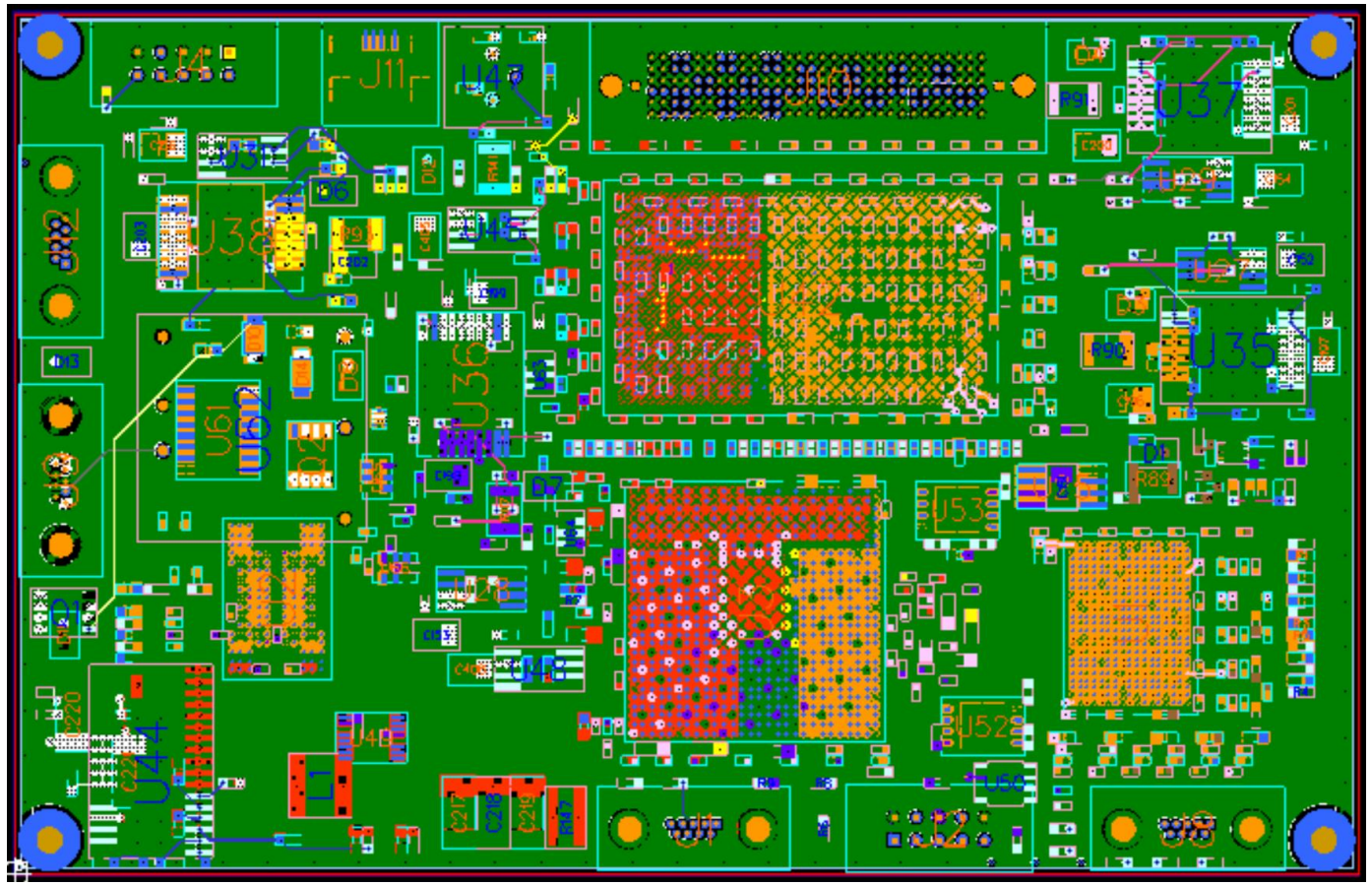


- *Each Cortex-A72 core offers a performance of 4.72 DMIPS/MHz and with four cores running at 1.8 GHz, the resultant horsepower is 34,000 DMIPS or greater than 45,000 CoreMarks®.*
- *Each core contains a SIMD vector processing unit, NEON, processing at 56.6 GFLOPS at 1.8 GHz.*
- *8 GB of DDR4 SDRAM and 1 to 4 Tb of NAND flash memory*
- *LVCMOS I/O, LVDS and 5 & 10 Gbps high-speed serial links*
- *Scalable performance, 1 to 4 MCU cores and/or FPGA.*
- *Scalable system power consumption ranges from 6.5 to 20 W dependant on clock frequency, no. of cores and I/O rate.*

Spacechips Edge 1 : AI-Enabled Edge-Based OBP

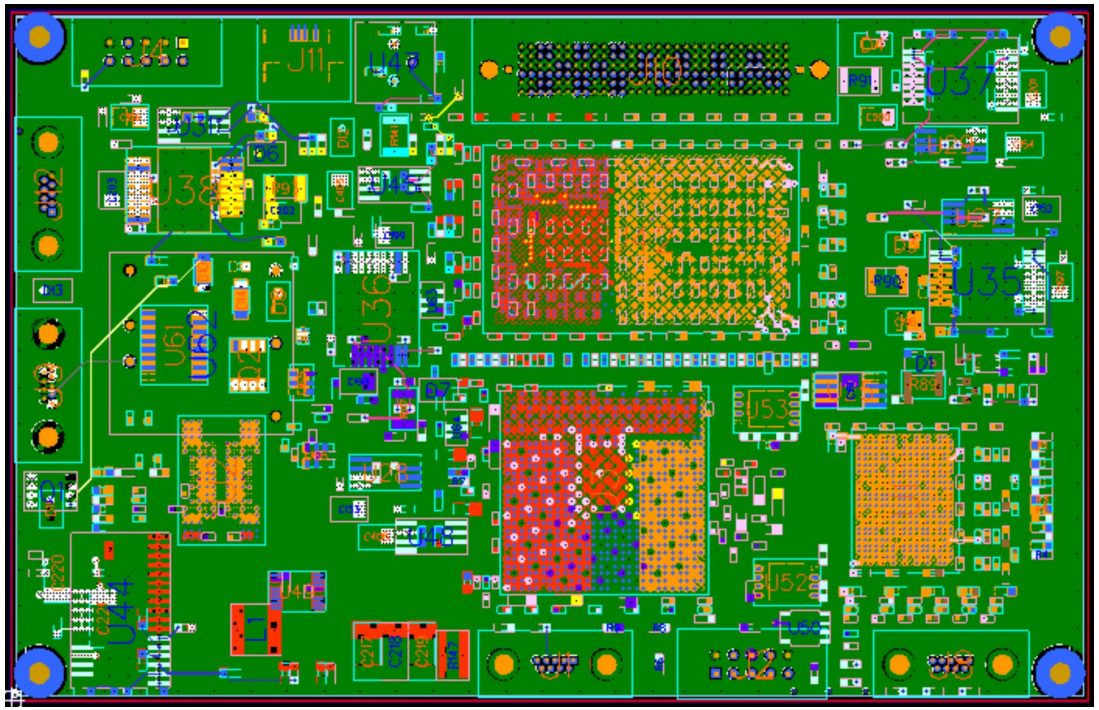
149 mm

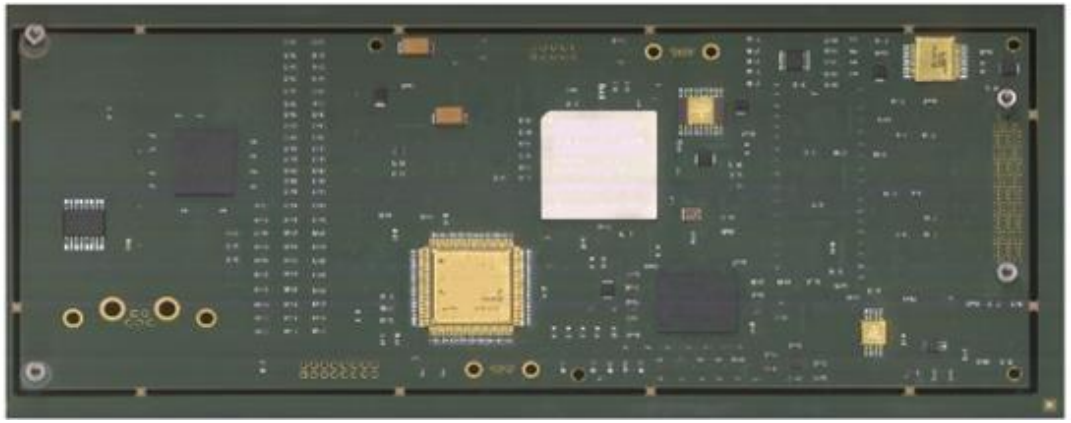
95.8 mm



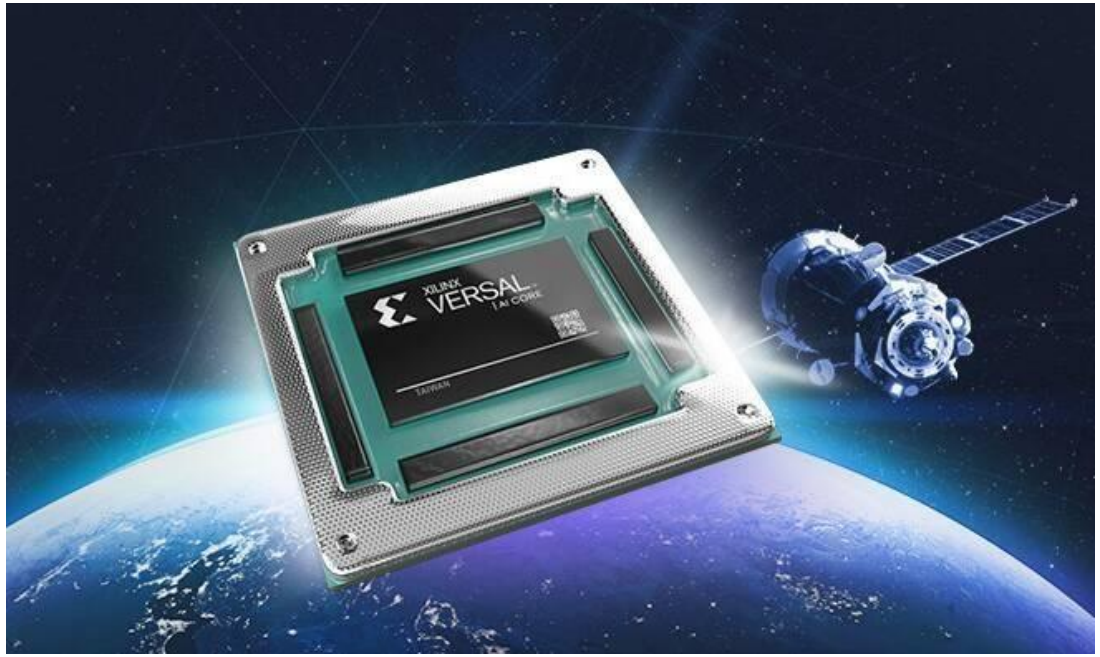
Moving the data centre to the origin of the raw data!

Bespoke OBP Integrating Sensor Drive Voltages



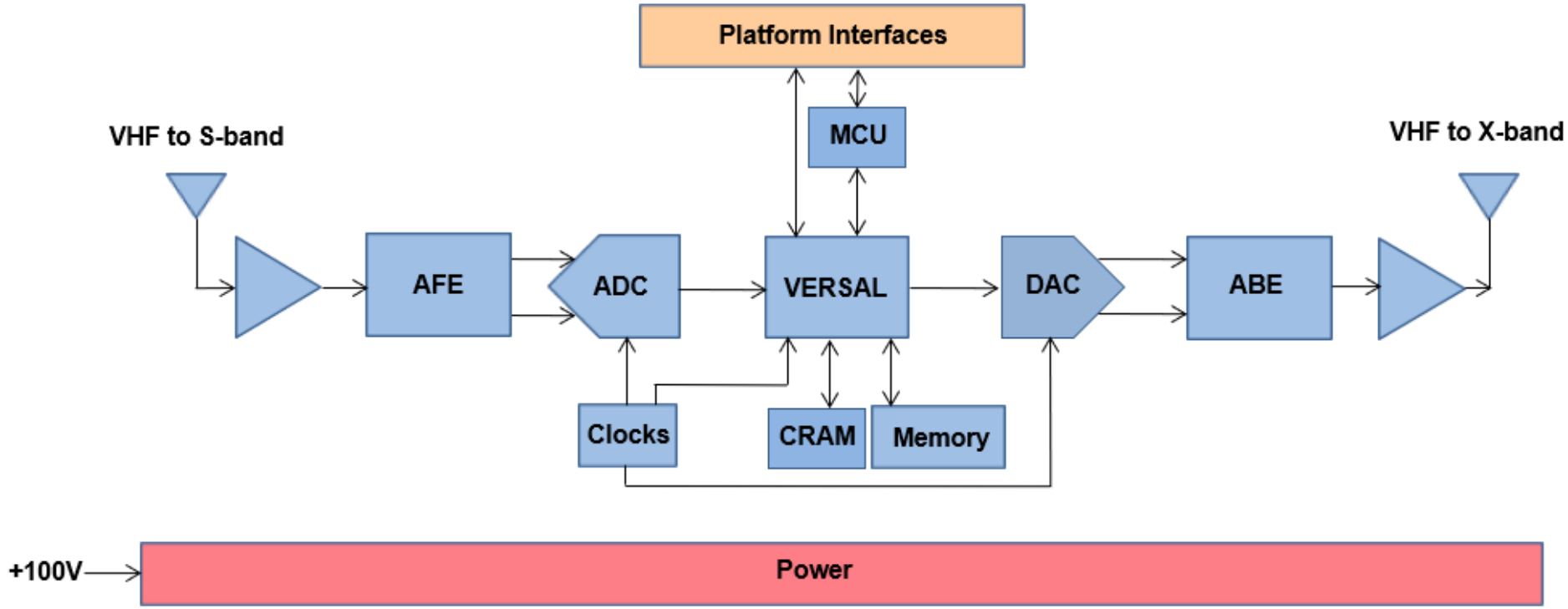


Spacechips' Versal Space Reference Design



- *AMD/Xilinx's Versal ACAP represents a timely and synergistic to enable in-orbit AI and ML.*
- *Spacechips is bringing-to-market an EM Versal Space Reference Design (XCVC1902-1MSEVSVA2197) later this year to allow you to prototype and de-risk in-orbit AI and ML.*
- *Populated with EM-grade versions of space-grade parts!*
- *The XCVC1902 is part of the AI Core Series (133 TOPs) and contains 400 AI engines, 1,968 DSP engines, 1,968,400 logic cells 899,840 LUTs and 1,968k logic cells.*
- *Spacechips is bringing-to-orbit a flight-qualified version next year which you can launch to implement AI and ML in-orbit.*
- *Populated with space-qualified components, delivered with EICD, an Instruction Manual and functional HDL to prove operation of the signal-chain blocks – no application code!*

Spacechips' Versal Space Reference Design

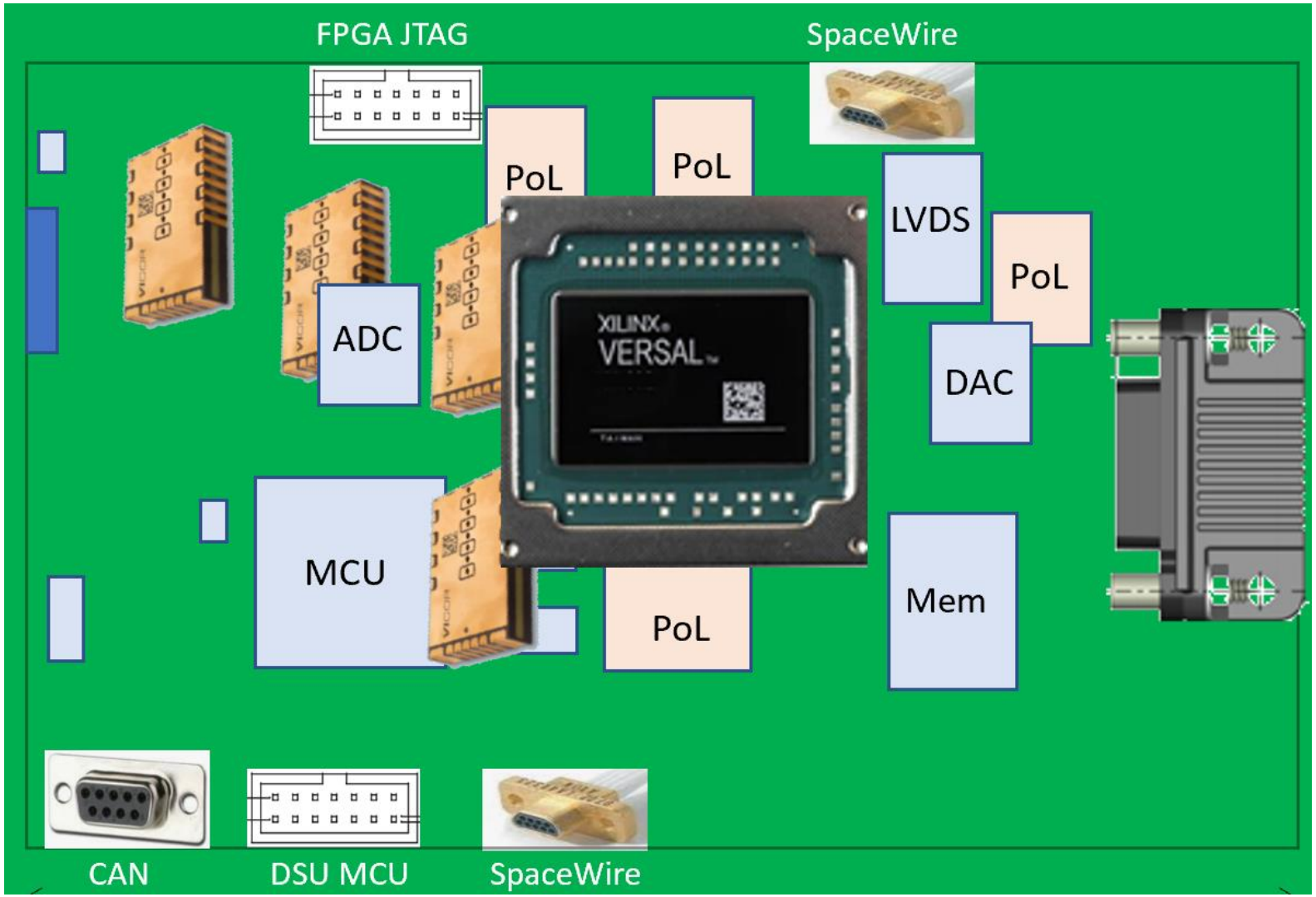


Representative transponder that allows RF traffic to be input, digitised, processed and intelligent analytics extracted in real-time.

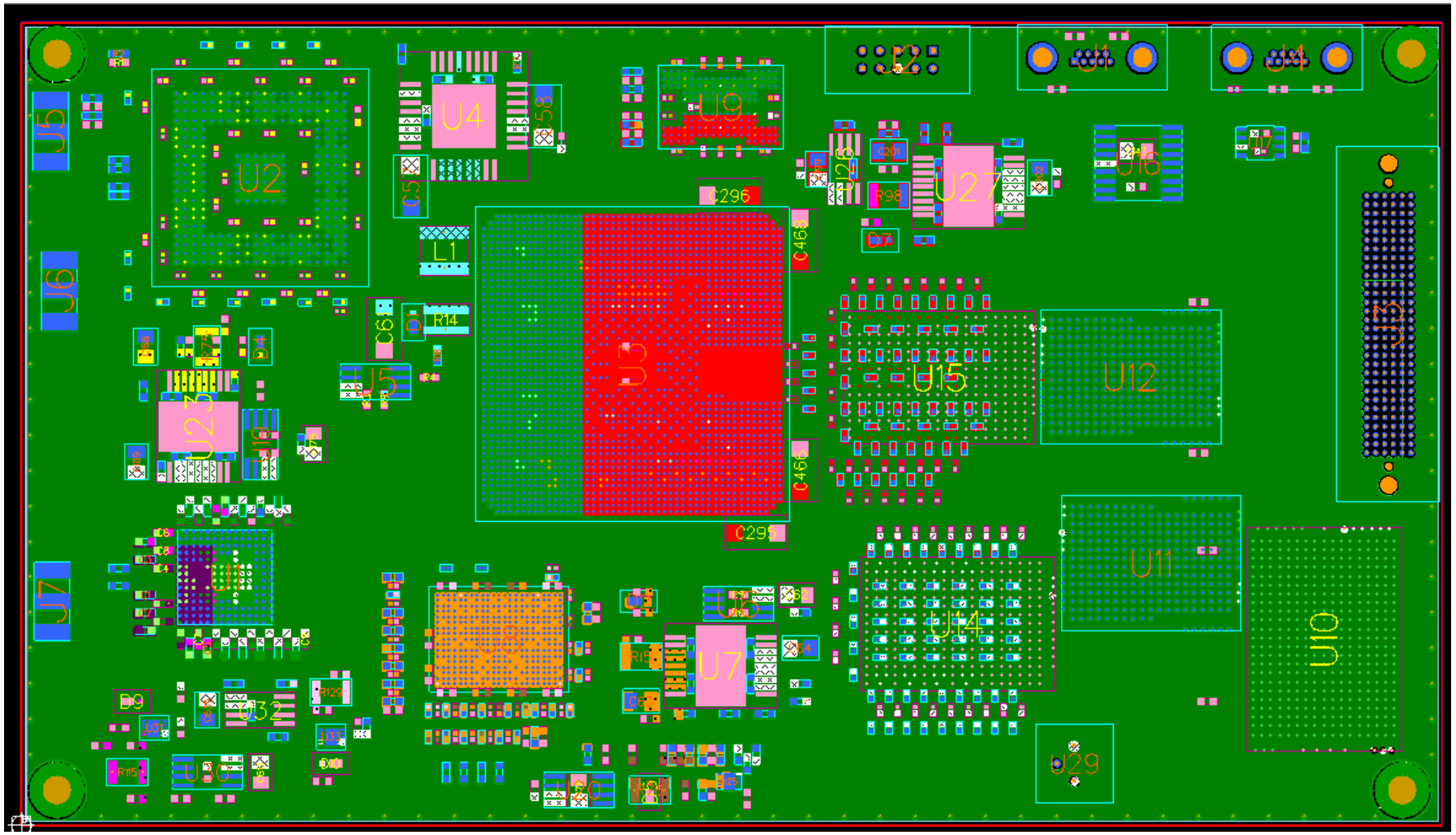
Data can be stored using fast DDR4 SDRAM or fast, 1 Tb NAND flash memory (DDR3-speed) and exported to external sub-systems using a variety of space-industry interfaces such as SpaceWire, SpaceFibre, SPI, CAN & 32.75 Gbps HSSLs.

1Tb of CRAM, scrubbing options supported as well as access to SMAP!

Concept Floorplan : XCVC1902-1MSEVSVA2197



Actual Floorplan : XCVC1902-1MSEVSVA2197



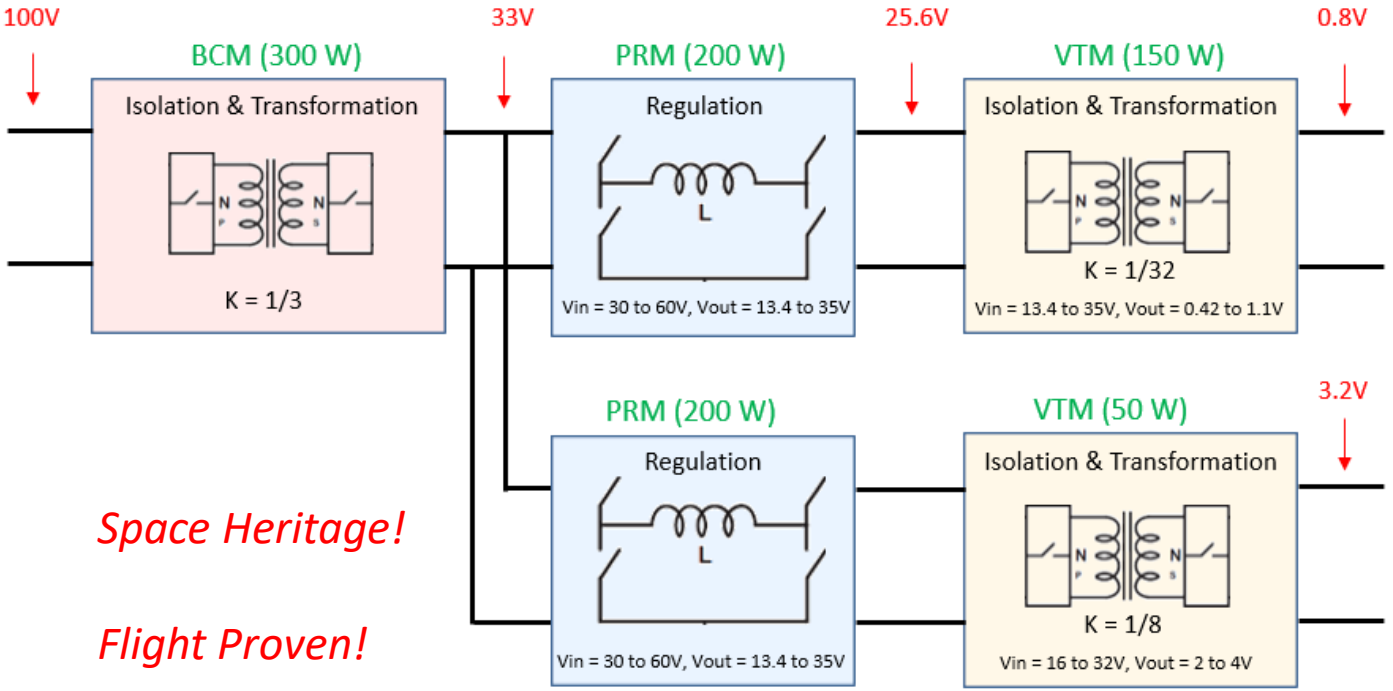
Versal Power Distribution

Domain/ Sequence no.	Rail Name	Rails	Voltage	DC Spec.	AC Spec.	Current (A)	Power (W)	Step	Comment
LPD/1 PL/1 PMC/1 System/1	PS_IO (Digital)	VCCO_500/1/2/3, VCCO_HDIO, VCCO_XPIO	1.8V – 3.3V (HDIO/PSIO) 1.8V – 3.3V (VCCO_50X) 1V – 1.5V (XPIO)	±1%	±5% (XPIO) (HDIO/PSIO/XPIO)*	0.100 - 3	10	100%	*1.8V, 2.5V at ±5%, and 3.3V at +3/–5% VCCO supplies can be combined if using same Voltage VCCOs must be powered on first in relevant domain
System/2	0V80_SOC _IO (Digital)	VCC_SOC, VCC_IO	0.8V	±1%	±17mV	3.5	3	33%	
PMC/2	0V80_PMC (Digital)	VCC_PMC	0.8V	±1%	±17mV	0.350	0.3	33%	0.88V for PS Overdrive
System/3	1V5_VCCAUX (Digital)	VCCAUX	1.5V	±1%	±2%	4.2	6.3	33%	
LPD/2	0V80_PSLP (Digital)	VCC_PSLP	0.8V	±1%	±17mV	0.300	.2	33%	0.88V for PS Overdrive
FPD/1	0V80_PSFP (Digital)	VCC_PSFP	0.8V	±1%	±17mV	1.5	1.2	70%	0.88V for PS Overdrive
PL/2	0V80_RAM (Digital)	VCCINT, VCC_RAM	0.8V	±1%	±17mV	135	108	33%	200A/us Slew Rate
PMC/3	1V5 (Digital)	VCCAUX_SMON, VCCAUX_PMC	1.5V	±1%	±2%	0.350	.5	100%	
PL/3	0V88 (Analog)	GTAVCC	0.88V	±2%	10mVpp	1.7	1.5	70%	Ripple is steady state, total tolerance is +/-3%. Ripple at FPGA pins, see UG578
PL/4	1V5 (Analog)	GTAVCCAUX	1.5V	±2%	10mVpp	0.100	.2	70%	Ripple is steady state, total tolerance is +/-3%. Ripple at FPGA pins, see UG578
PL/5	1V2 (Analog)	GTAVTT	1.2V	±2%	10mVpp	2.8	3.3	70%	Ripple is steady state, total tolerance is +/-3%. Ripple at FPGA pins, see UG578

When the XCVC1902-1MSEVSVA2197 is fully implemented, its 0.8 V core voltage will draw around 140 A with a total device dissipation of 130 W.
57% of the overall power is consumed by the AI engines, 13% by logic, 10% by the high-speed transceivers, 10% by clocking and PLLs
5% by processors and the remainder by memory and interfaces


GND
VIN
PVIN
GND
GND
VOUT

Factorised Power Architecture

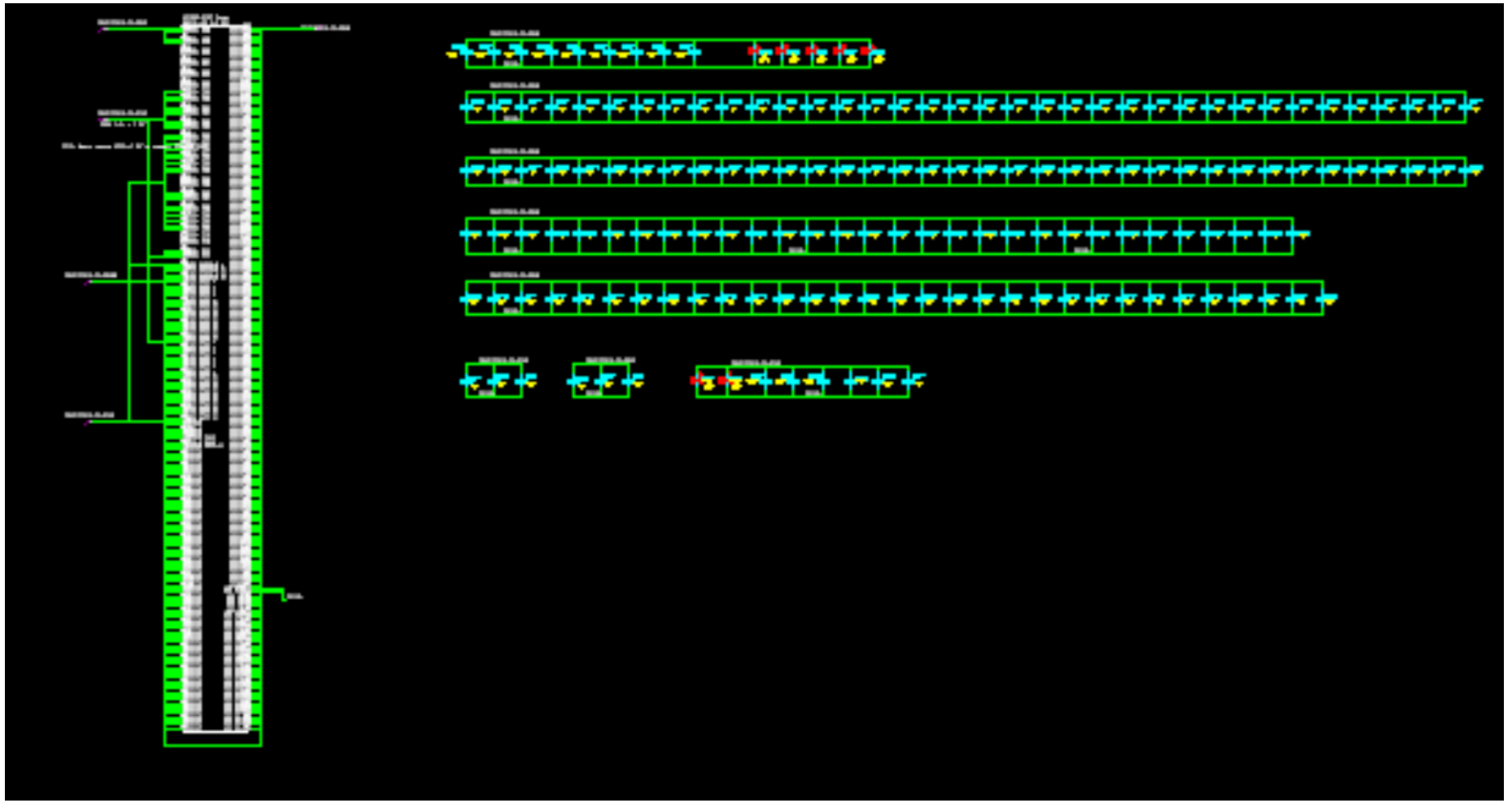


The FPA consists of voltage regulation followed by transformation: first, a buck-boost topology is used to generate a high-voltage intermediate rail from an external source, which is significantly higher than the lower legacy buses typically input to POLs, e.g. a 48 V output bus requires four times less current than a 12V intermediate bus for the same power (P=VI) and PDN losses are the square of the current ($P=I^2R$), which reduces by sixteen.

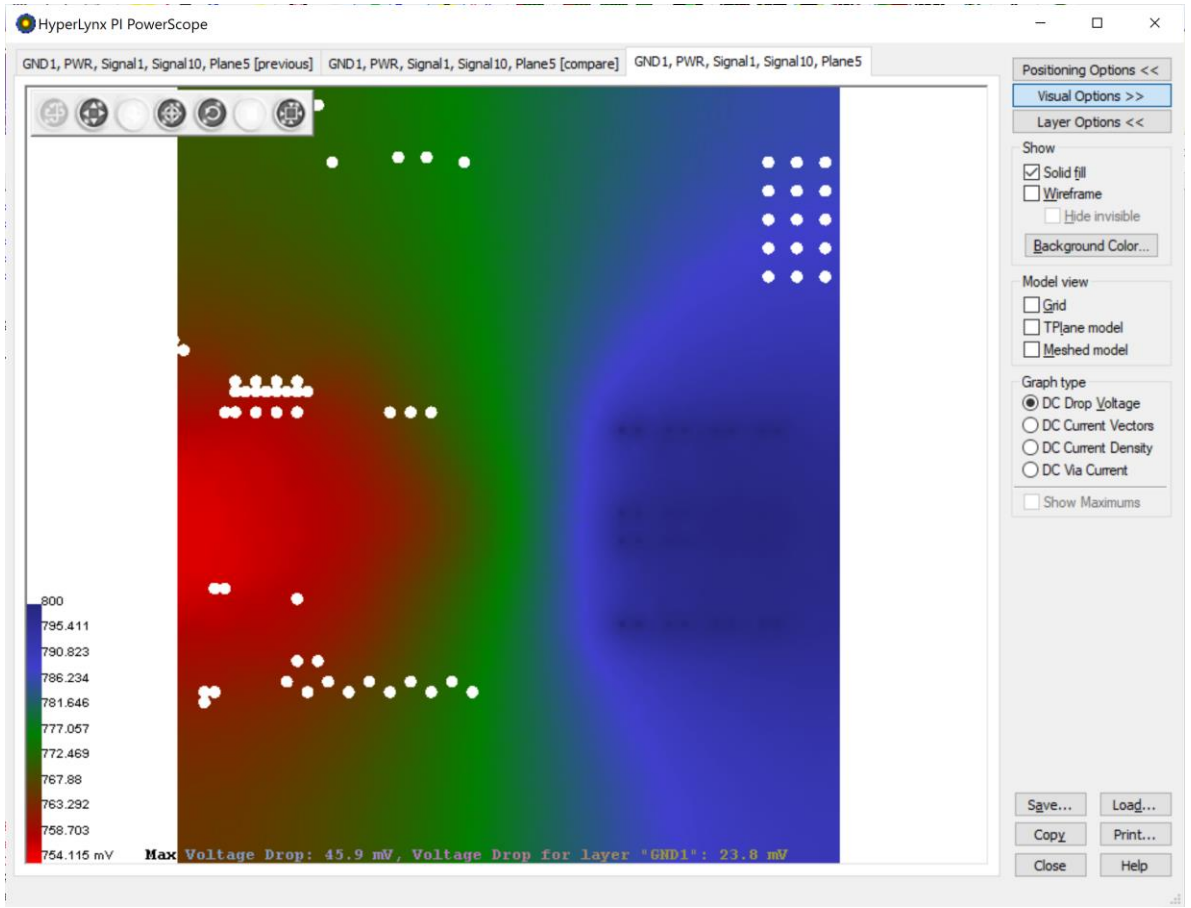
The PRM generates a regulated 'factorized bus' from an unregulated input followed by the VTM, which transforms (steps-down K=1/32) the high 'factorized bus', 25.6 V to the desired core voltage of 0.8V

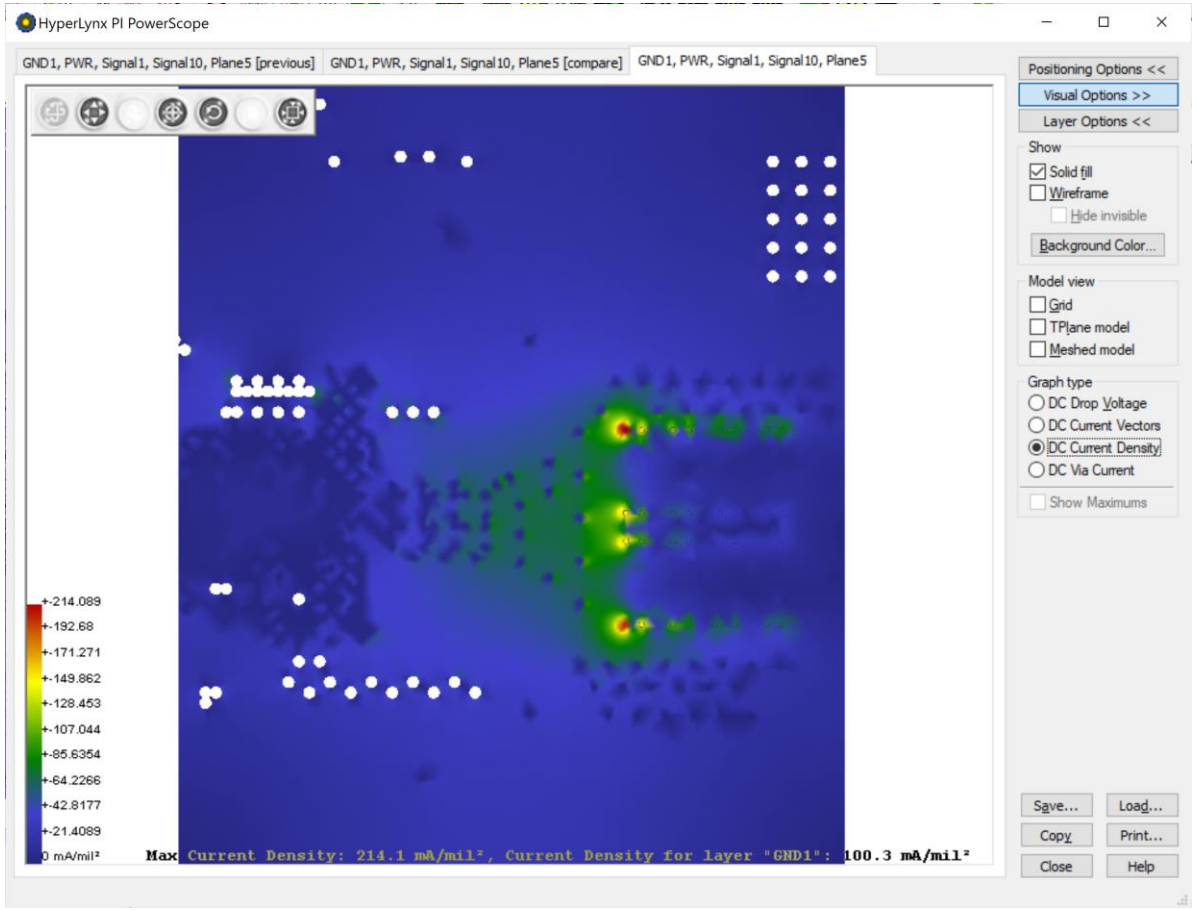
[DC-DCs meet power-distribution needs of NewSpace applications - EDN]

2% Ripple = 17 mV, PDN Ztarget ~ 200 uΩ



Sufficient Copper CSA to minimise I^2R Drop





Conclusion

- *For high-definition SAR video, the raw computing performance of the Spacechips' Edge 1 OBP together with its fast, memory interface and small form-factor makes it suitable for extracting real-time insights from Earth-Observation imaging data. DDR4 rates up to 2.1 GHz avoid traditional I/O bottlenecks.*

- *For real-time situational awareness, e.g., for identification of friend or foe or space-debris collision avoidance, Spacechips' Versal Reference Design is able to fuse and process Tbps of data from multiple sensors with low latency in real-time to deliver ASIC-class, in-orbit AI & ML system-level performance.*

- *For object classification, AI inference and autonomous decision making to enable feature identification or re-configurable, cognitive transponders based on real-time traffic needs, Spacechips' Versal Reference Design would result in the most efficient vector-compute solution compared to traditional FPGAs or MCUs.*

- *Spacechips' Edge 1 OBP will deliver in-orbit AI and ML at lower power dissipation and less financial cost.*

Conclusion

- *Spacechips is bringing to market a range of smart OBCs and transponders which enable in-orbit AI and ML offering performances from 56.6 GFLOPS to ~200 TOPS.*

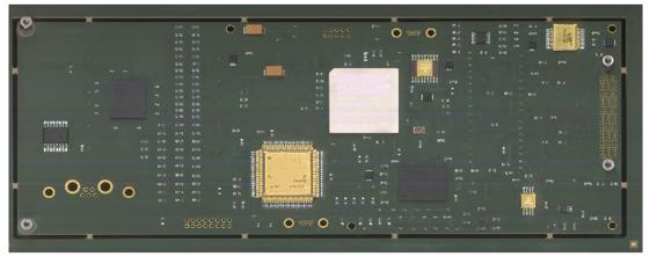
- *Spacechips is bringing-to-market EM and FM Versal Space Reference Designs (XCVC1902-1MSEVSVA2197) later this year to allow you to prototype and de-risk in-orbit AI and ML (133 TOPs).*

- *Spacechips is bringing-to-orbit a space-qualified Versal Space Reference Designs next year to allow you to implement Ai and ML in-orbit.*

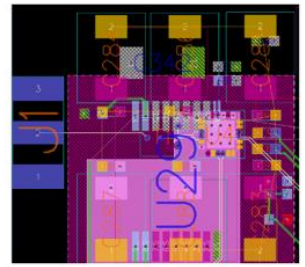
- *Orders for the XCVC1902-1MSEVSVA2197 EM Versal Space Reference Design currently being taken – EM-grade parts, includes an EICD, an Instruction Manual and functional HDL to prove operation of the signal-chain blocks – no application code!* *Next year we will also offer a 28V version!*

- *In 2024, Spacechips will bring-to-market lower-power EM and FM versions of the Versal Space Reference Design baselining the smaller XCVE2302-1MLISFVA784 ACAP (45 TOPs, 34 AI, 150k LUTs, 324 DSP, 329k logic cells)*

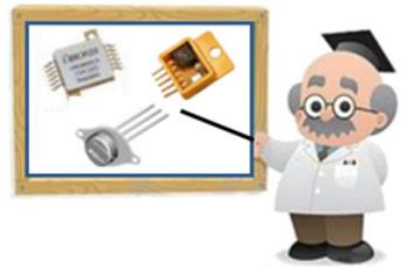
- *Products*



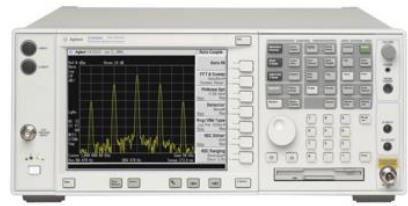
- *Design-Consultancy Services*



- *Training Services*

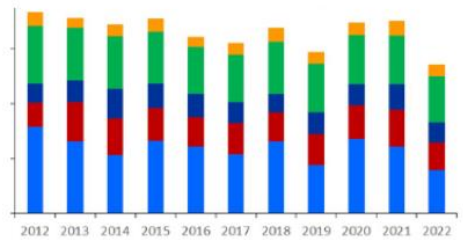


- *Testing Services*



- *Technical-Marketing Services*

- *Business-Intelligence*



Dr. Rajan Bedi
CEO Spacechips
rajan@spacechipsllc.com

http://out-of-this-world-design.info/
https://www.linkedin.com/in/drrajanbedi/

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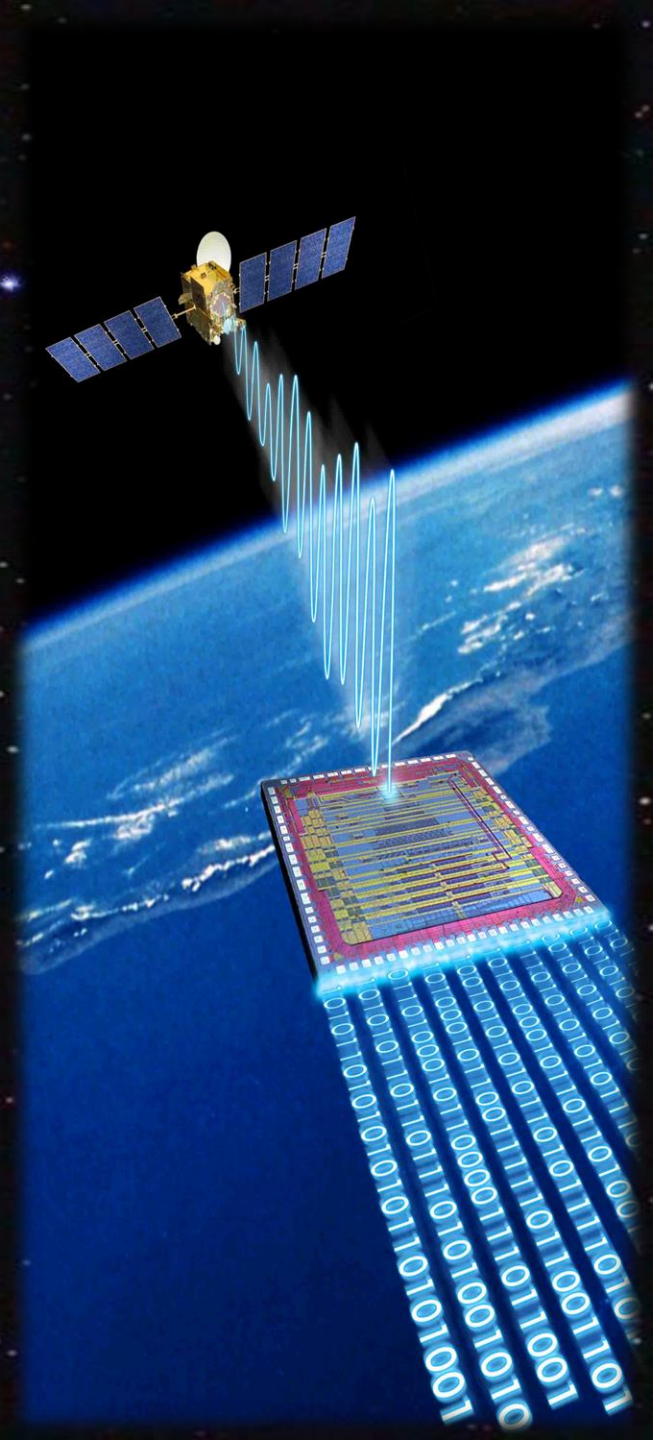

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