EDHPC 2023
European Data Handling & Data Processing Conference for Space

The Universal Processing Module
A Standardized Electronics for Next Generation Radar Processing

DEFENCE AND SPACE

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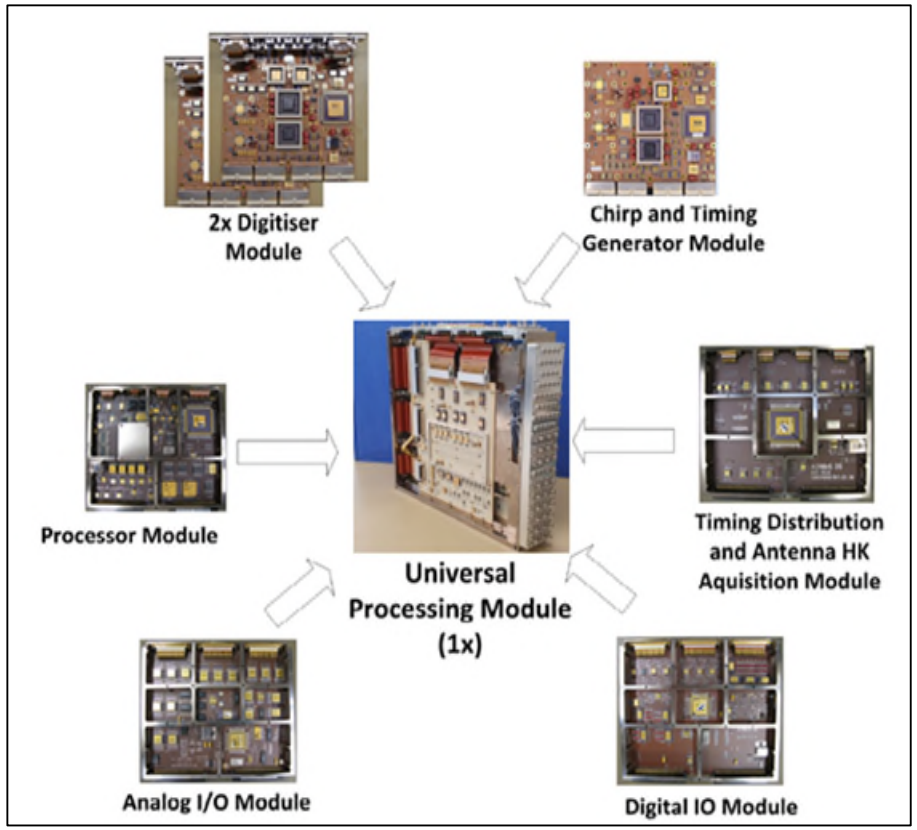
Agenda

- Introduction
- Architecture
- Novelties in Architecture
    - Multi Channel Rx Synchronisation
- Novelties in Technology
- Exemplary Target Applications
- Customization
- Development Status and Outlook

Introduction

- The Universal Processing Module is a single module that contains all functions and interfaces required for on-board Radar data conversion and processing together with the instrument control functionality. Reduction of mass by the factor of 2 to 3 and power by more than 50% compared to previous generations
- Establishes a standardized H/W platform suitable for most Radar missions within the next 5 to 10 years
- Customization is enabled by assembly configurations, IO adaptions and mission specific firmware
- The standardization is driven from the growing complexity and cost of specific hardware development and the need for faster realization times of space born radar missions
- Replaces more than four heritage data conversion and processing product lines



Merge of traditional Radar Backend Modules within a single UPM

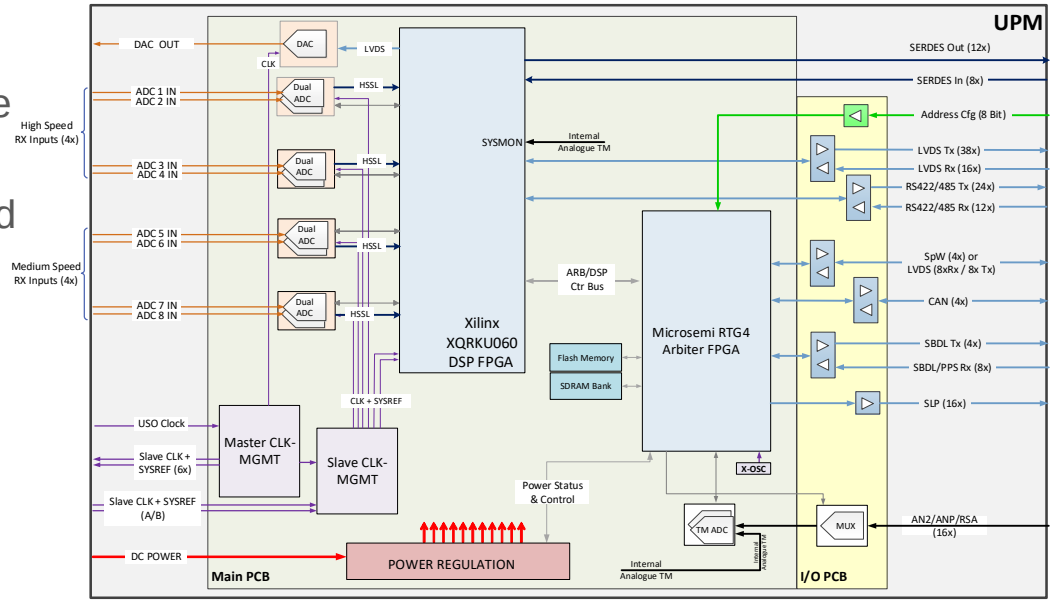
UPM Architecture
Electrical Interfaces and Functional Blocks

- The processing core is provided by the most powerful FPGA available in space grade. The Xilinx XQRKU060.
  In orbit re-programmability and multi-image hosting are supported

- A radiation hard RTG4 FPGA for configuration and radiation hardening of the XQRKU060. In addition non real-time critical functions and the option to implement the Instrument Control function by an embedded ICU are provided

- 4 Dual Channel ADC with up to C-Band sampling capability which support
  - up to 8 Rx channels with 0.5 GHz signal bandwidth
  - up to 4 Rx channels with 1.6 GHz signal bandwidth
  - Up to 2 Rx channels with 3.2 GHz signal bandwidth

- 1 DAC with up to C-Band output capability and up to 1.6 GHz signal bandwidth
- Internal clock synthesis from USO clock to sample clock
- External interfaces are matched to state-of-the-art Radar instrument needs, future needs are anticipated



UPM Functional Block Diagram

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UPM Architecture
Mechanical Design

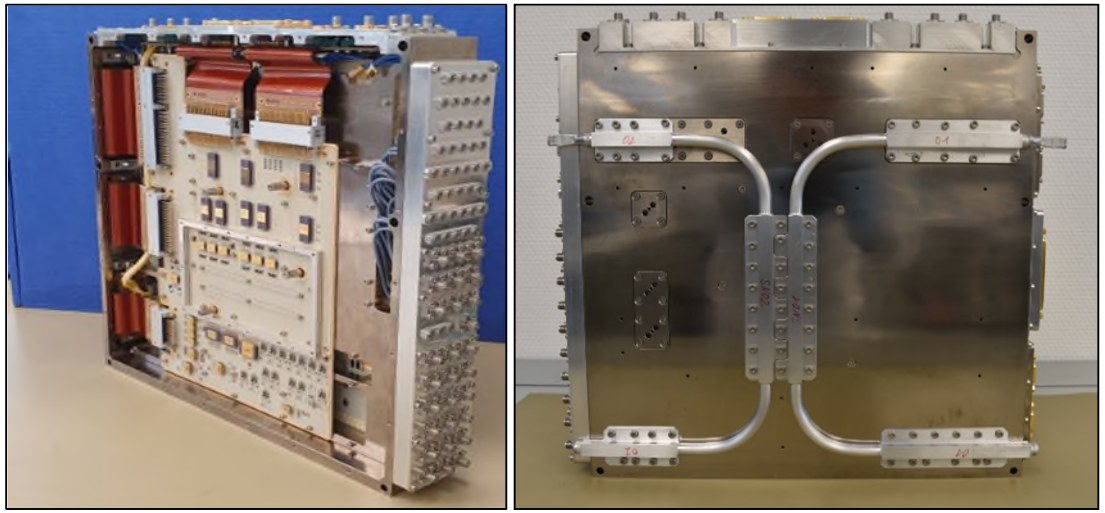
- The UPM is a single module with an independently EMC sealed enclosure

- It contains
  - The main PCB that contains all performance critical circuits
  - A mezzanine I/O PCB with standard interface circuitry
  - Flex-Rigid adapter PCB to provide mission specific IO connector configurations
  - Internal coax harness for RF signals and clocks

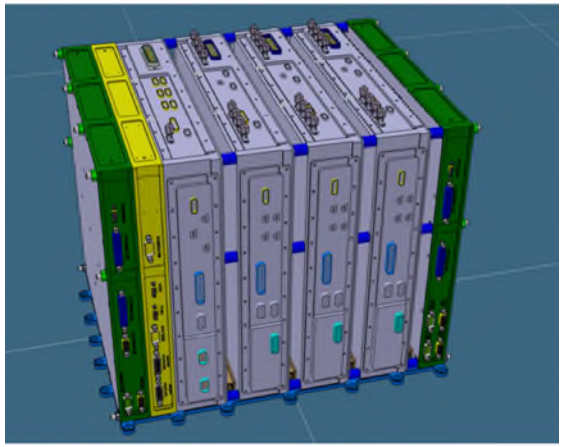
- The chassis and connection to the PCB is highly optimized for thermal performance. Heat Pipes can be optionally externally attached.

- High-Dissipating EEE are top-lid cooled

- Up to 60W steady state or 120W peak dissipation are supported
- Multiple modules can be stacked together with matched power conversion modules to a box configuration



UPM Mechanical Design with optional Heat Pipes
(Back Cover not shown)

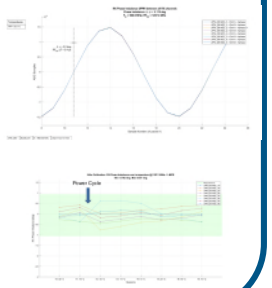


Exemplary Box Configuration

Novelties in Architecture

Multi-RX Channel Fine-Sync Capability

- Prerequisite for on board digital beamforming
- Fine sync below one picosecond capability
- Excellent stability over temperature with <1.5° drifts in L-band
- SCORE implemented for ROSE-L



Cognitive SAR Ready

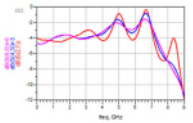
- Very large amount of configurable real-time processing resources
- On-board S/W host capability
- In-orbit update and add-on of functions supported
- Access to all instrument related data and telemetry

All-in-One Radar Backend

- Replacement of multiple heritage product lines
- All major digital backend functions combined
- Scale able on module and system level

Broadband RF Design

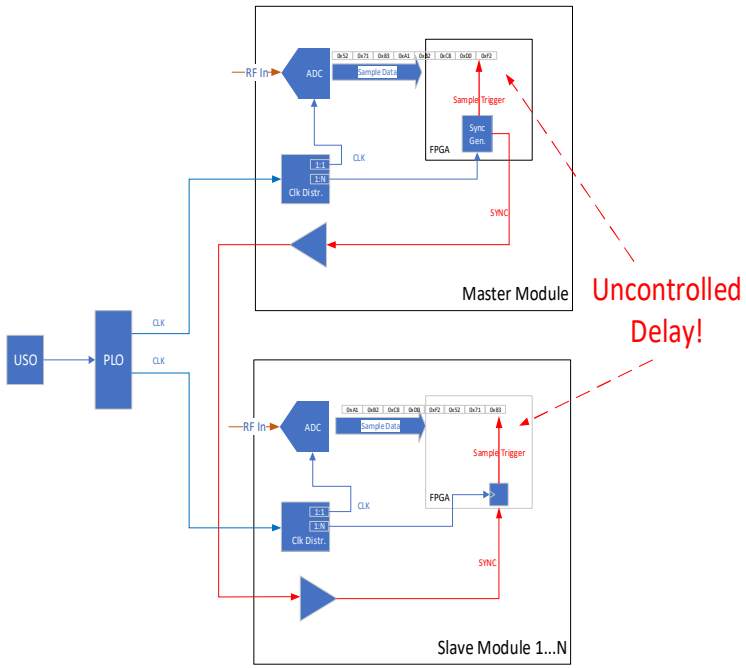
- Analogue input BW from close DC to C-Band
- Direct sampling
- Rx/Tx bandwidth of 1.5 GHz and more



In-Orbit Reconfiguration

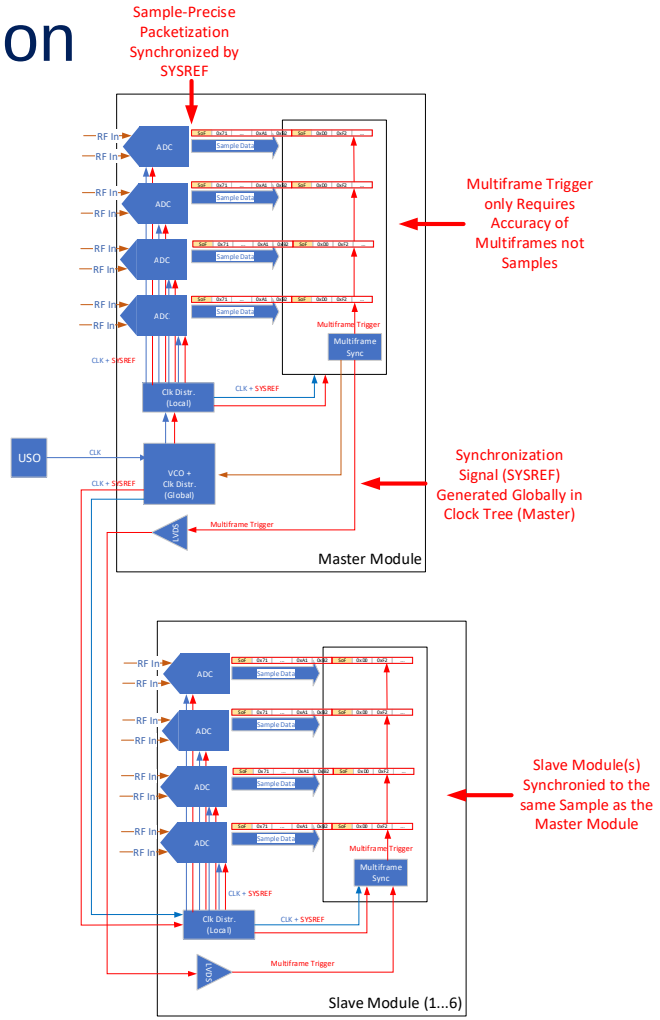
- DSP FPGA reconfigurable in space
- Multi-image host capability
- swap between images supported

Rx Multi-Channel Synchronisation



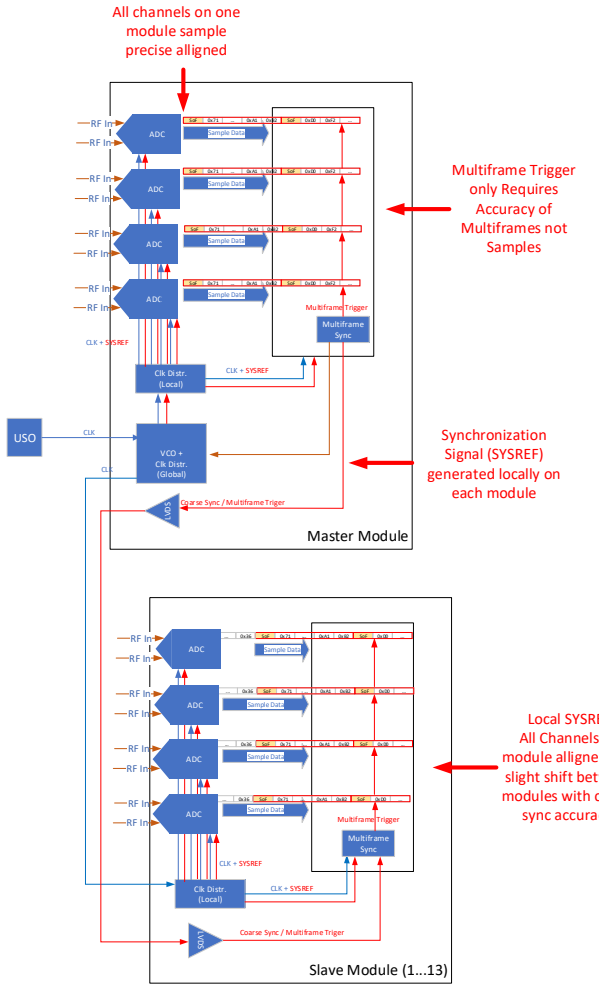
Traditional Systems

- ADC free running and coarse sync'd by LVDS or similar
- Channel sync. limited by sync link accuracy and drifts and clock divider ambiguities (multiple samples)



UPM Global Sync

- All channels even between multiple modules sync'd to sub-sample level
- Supported for up to 7 modules / up to 56 Rx channels



UPM Local Sync

- Modules internally fine sync'd (8x Rx), coarse sync between modules
- Supported for up to 14 modules

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Novelties in Technology - Highlights

Latest Generation of Space-Grade EEE

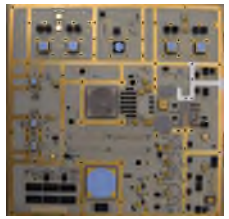
- Latest generation of space grade FPGA, ADC, DAC, clocking and power solutions
- Development started at the time the parts were announced to have them in-time ready for flight

GaN Based Power Supply

- Use for core supply of XQRKU060 FPGA
- >30A output capability at highest precision and efficiency
- Highest load step performance

Advanced Thermal Solutions

- Application of new interfiller materials qualified for space
- Top-lid cooling of EEE
- Up to 40W of DSP FPGA dissipation supported
- External heat pipes supported



High Speed Broadband PCB

- Qualification of Megtron 7N for space use
- Outperforms previous generation of HDI materials with performance close to RF substrates
- High RF performance with state-of-the-art HDI stack-up combined

MEGTRON7

Exemplary Target Applications

Multi Channel Rx missions with digital beamforming

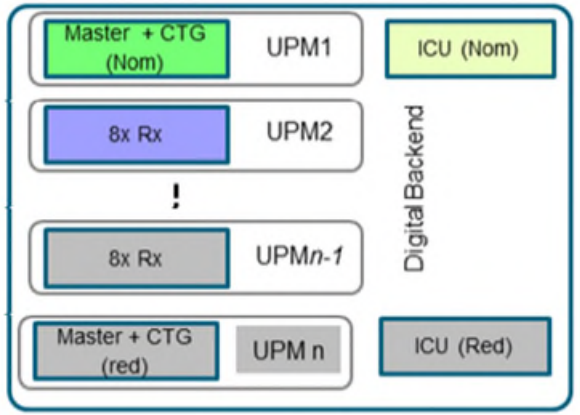
- Up to 14 UPM can be operated in a synchronous master-slave configuration
- Each UPM supports up to 8x Rx channels for implementation of advanced on board processing such as Scan on Receive (SCORE)
- A shared digitizer (slave) array is controlled by cold redundant CTG (master)

High Performance Missions

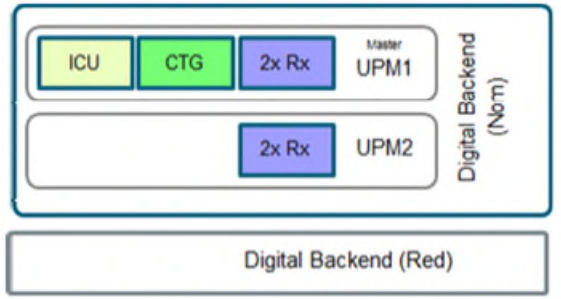
- Compact backend with one combined CTG/digitizer and an additional slave digitiser. ICU merged into CTG
- 4 to 8 Rx channels with > 1 GHz bandwidth each can be implemented (depending from the processing need)
- Cold redundancy recommended for small assemblies

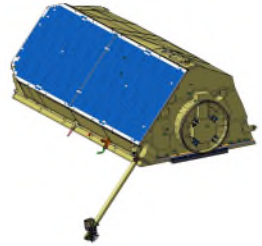
Low Cost / Low Mass Missions

- Single module digital backend for cost or mass sensitive applications
- Redundancy is optionally implemented by a second module

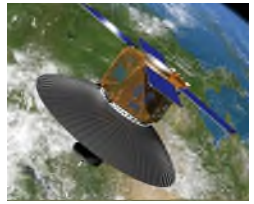


Multi Rx DBE Configuration





High Performance 4-Channel Application



Compact SAR Application

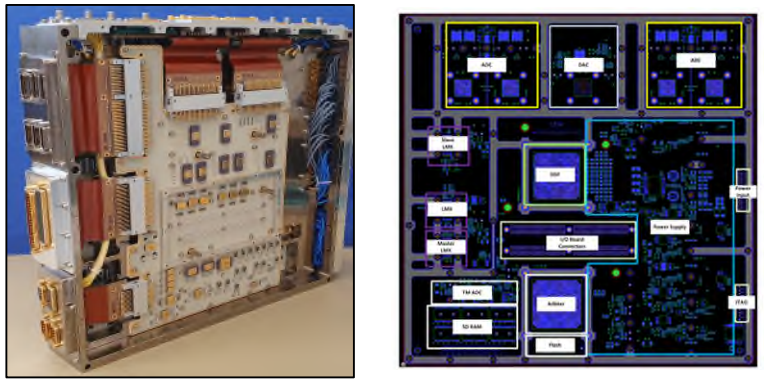
Module Level Customization

The following customization options are provided:

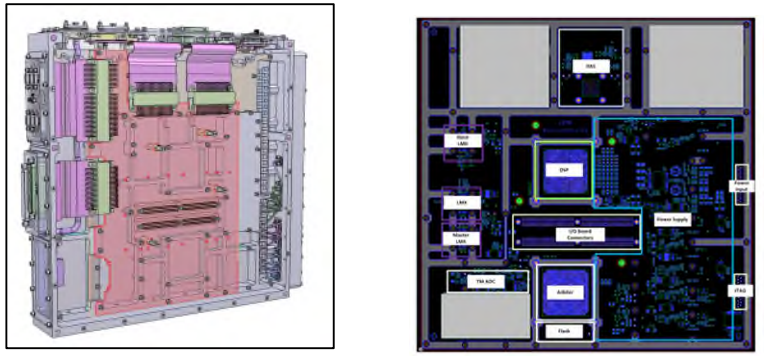
- Specific DSP FPGA firmware matched to the needs of the target missions
- PCB assembly options with only the key components populated that are required for the function/role of a respective UPM
- Interface customization by:
  - Assembly configuration of external connectors and internal clock/RF harness
  - Adaption of flex-rigid IO adapter PCB

All these modification do not impact the overall design baseline, critical PCB and hence the hardware qualification status.

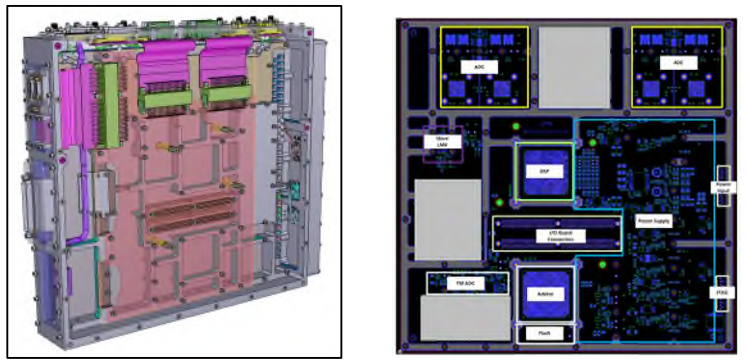
This is an enabler for avoiding schedule and cost of development and hardware qualification ➔ EM to PFM for target missions



Full Design Mechanical and PCB Assembly Configuration



CTG Only Mechanical and PCB Assembly Configuration



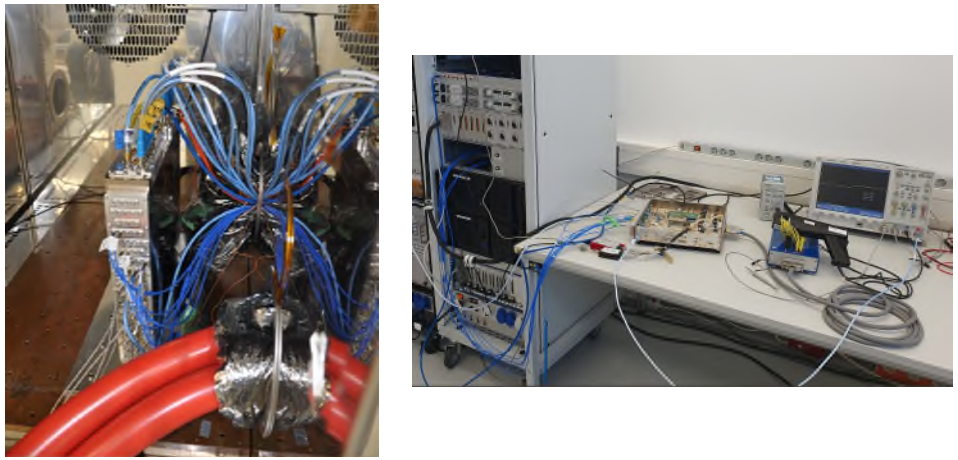
Digitizer Only Mechanical and PCB Assembly Configuration

Development Status and Outlook

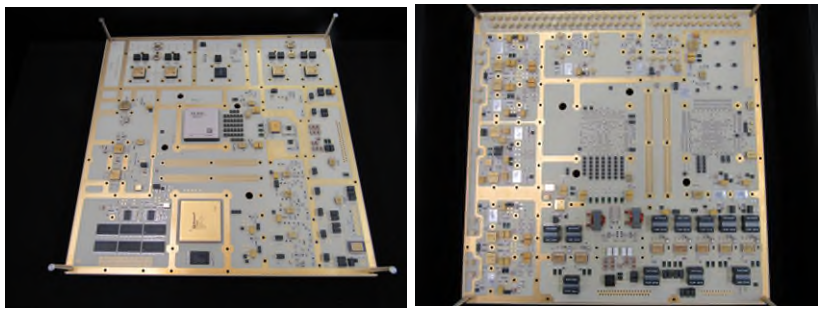
- EM+ built and successfully tested to **TRL6** in 2022
- EQM production is ongoing at the time of presentation with the full EQM built available in 2023.
- Hardware qualification to TRL7 will be performed in a box configuration consisting of two UPM EQM modules and one matched Power Supply EQM module
- ROSE-L FM module production is planned for 2024

The development is supported by a co-funded GSTP activity with the main focus on the generic approach and background technology development. Airbus would like to thank ESA and DLR for support.

UPM is concepted to be able to accommodate future possible design evolutions in case system needs arise or to incorporate future technology evolutions.



UPM EM+ under test



UPM EM+ Main PCB

Thank you

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