GR716: LEON3 mixed-signal rad-hard microcontroller

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PUBLIC

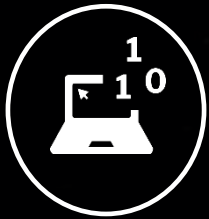A world leader in embedded computer systems for harsh environments

Experts in fault-tolerant computing

We provide a full ecosystem to support hardware and software design for:
- Standard components
- Semi-custom FPGA
- Full custom ASIC

Based on SPARC and RISC-V architectures

GR716:
Rad-hard Microcontroller

GR716A and GR716B - LEON3FT Microcontroller

Baseline features

- Single-core LEON3 SPARC V8 processor, Rad-hard, Fault Tolerant

- LEON-REX extension with 16-bit instructions: improved code density

- 2x Real Time Accelerators

- Support for many different standard interfaces (SpaceWire, Ethernet, CAN, MIL-STD-1553, SPI, I2C, and more)

- 192 KiB on-chip RAM

- FPGA Supervisor

- On chip DACs, ADCs, LDO and PLL – SWaP-C improves

- LEON Technology – re-use of Development and Software ecosystem.

- Can replace FPGA implementations – SWaP-C improves

Applications

- Satellite supervision, monitoring and control

- Sensor bus control

- Distributed multi-interface communication nodes

- Propulsion system control

- Motor control

- Radiation environment monitoring

SPARC
Compliant
SCD V8

FRONTGRADE
Gaisler

GR716A

LEON3FT
Microcontroller

LEON

GR716A and GR716B - LEON3FT Microcontroller

Specification

Part no.	Processor core	Clock freq. (MHz)	DMIPS/core	TID krad (Si)	SEL LET (MeV-cm^2/mg)	Power cons.	Package	Temp. range	Qualification status	Availability	Development board
GR716A	Single-core LEON3FT	50	>70	100 (analog) 300 (functional)	> 118	< 200mW at room temperature	132-Pin Ceramic Quad Flat Pack	-55°C / +110°C (case)	• Qualification tests as per PCA defined by ESCC Basic Specification No. 2567000 • Screening tests as per ESCC 9000	Flight parts available	GR716 SW Eval. Board GR716 HW engineering Board
GR716B	Single-core LEON3FT + 2x RTA	100	>140	100 (analog) 300 (functional) **TBC**	> 118 (TBC)	< 250mW at 40 °C (TBC)	132-Pin Ceramic Quad Flat Pack	-55°C / +125°C (case)	• In development	Prototypes in Q2 2024*	GR716 interface dev. Board

Complete software toolchains and debugger are available

- Released new GR716A datasheet in November 2022
- Released first GR716B datasheet in December 2022
- App Note about GR716A vs GR716B
- GR716A and GR716B are pin compatible as long as the same resources are used. However, the exchange requires software recompile

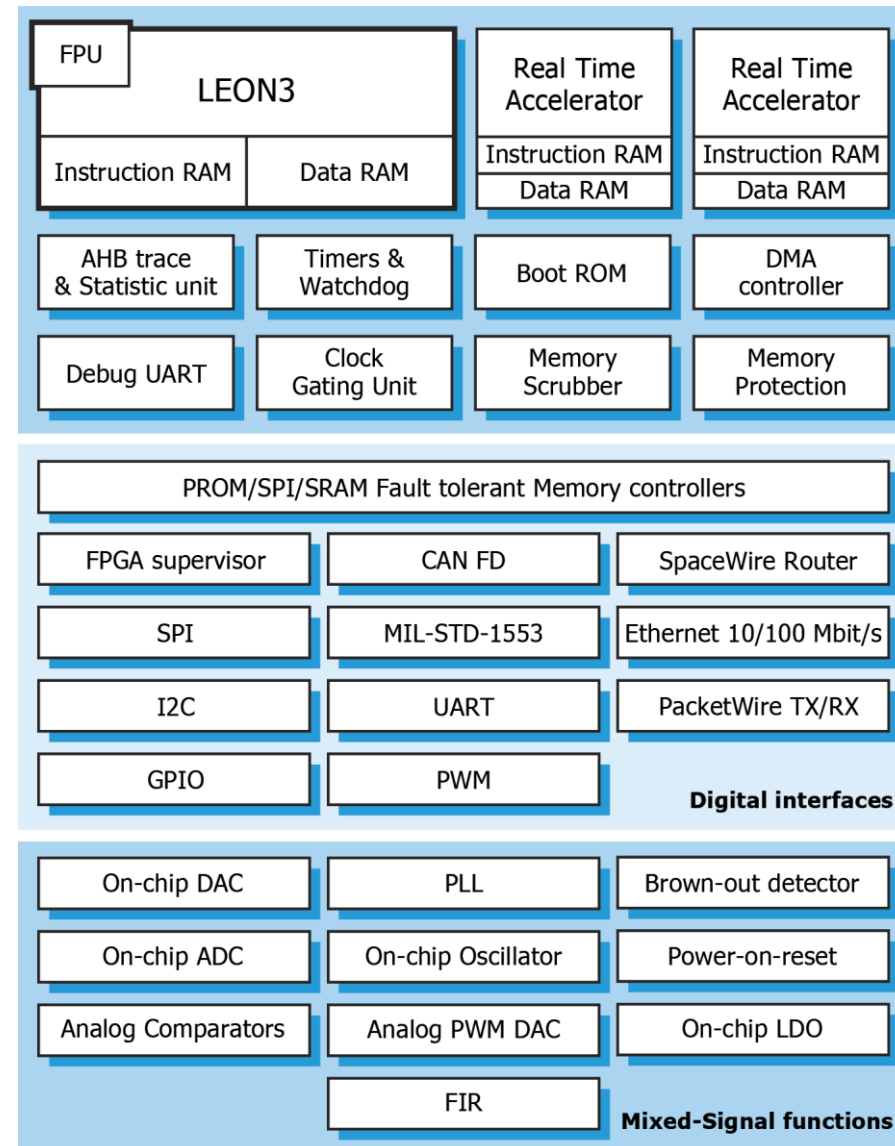*Subject to change without notice

GR716B - LEON3FT Microcontroller Enhanced Product

Features

- LEON3FT - Fault-tolerant SPARC V8 32-bit processor, 100 MHz.
  - LEON-REX – extension with 16-bit instructions: improved code density
  - High-Performance Floating Point Unit
  - 192 KiB on-chip RAM with EDAC
  - Deterministic software execution: Multiple non-intrusive buses, fixed interrupt latency, cache-less architecture...
- 2x RTA (Real Time Accelerators) - allowing complex real-time functions to be implemented independlty from the main LEON3 processor
- External EDAC memory: 8-bit PROM/SRAM, SPI (4 Byte address)
- External FPGA supervisor for programming and scrubbing Xilinx Virtex5, Kintex UltraScale
- Enhanced DMA controller with support for 'if-else' statements
- 4x ADC 11/14 bit resolution , 500 /80 ksps , 8 differential or 16 single-ended channels per ADC
- 4x DAC : 12bit 20 Msps
- 8x DAC 24bit PWM @ 25MHz
- 20x Analogue comparator: 20ns (60ns SET-hard)
- Integrated PLL, 3.3V single supply, Power-on-Reset and Brown-out-detection

Interfaces

- 10/100 Mbps Ethernet
- SpaceWire Router (2 external ports) with time distribution support, 200 Mbps max bitrate
- LVDS with extended common-mode, Cold-Spare and Fail-Safe support
- MIL-STD-1553B interface
- CAN-FD controller interface with CANopen support for remote boot
- Programmable Enhanced PWM with analog/digital voltage control loop support
- UARTs, I^{2}C, SPI with SPI-for-Space protocols, Timers, Watchdog, mixed GPIO

Block diagram:

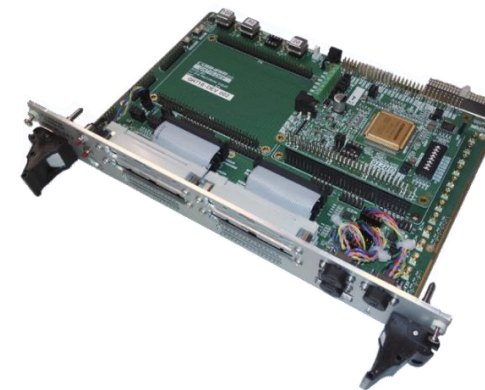| FPU	LEON3	Real Time Accelerator	Real Time Accelerator
	Instruction RAM / Data RAM	Instruction RAM / Data RAM	Instruction RAM / Data RAM
AHB trace & Statistic unit	Timers & Watchdog	Boot ROM	DMA controller
Debug UART	Clock Gating Unit	Memory Scrubber	Memory Protection

PROM/SPI/SRAM Fault tolerant Memory controllers

FPGA supervisor	CAN FD	SpaceWire Router
SPI	MIL-STD-1553	Ethernet 10/100 Mbit/s
I2C	UART	PacketWire TX/RX
GPIO	PWM	**Digital interfaces**

On-chip DAC	PLL	Brown-out detector
On-chip ADC	On-chip Oscillator	Power-on-reset
Analog Comparators	Analog PWM DAC	On-chip LDO
	FIR	**Mixed-Signal functions**

GR716 Boards

GR716-MINI

- Size: 37.5% of a credit card
- SPI Flash & SRAM memories
- Available for free-of-charge loans

GR716-BOARD-Daughter

**GR-CPCI-GR716-DEV
Interface Board**

- 8 cm x 10 cm format
- Stackable pin headers for I/O interfaces

- CPCI 6U format
- Facilitates access to all the I/O and memory interfaces

GR716: Software Support

BCC2 bare metal cross-compiler:
- GNU GCC
- LLVM CLANG
- GNU Binutils (assembler, Linker)
- BSP
- Drivers for IO peripherals
- Supports Real Time Accelerators

GRMON3 Debugger:
- Non-intrusive debug environment
- GUI support with C/C++ source level debugging
- TCL-based scripting framework shared with TSIM3

GRM3N
debugging made easy

Zephyr RTOS:
- BSP
- Drivers for IO peripherals
- Cross-compilation toolchain

TSIM3 Instruction-level simulator:
- Accurate behavior and timing
- TCL-based scripting framework shared with GRMON3
- GR716 I/O modelling

TSIM3
Instruction-level simulator

GR716A & GR716B: Functionalities Comparison

GR716B: Real Time Accelerator (RTA)

An RTA includes:

- LEON3FT processor with 2 register windows and support for 32bit multiplier and accumulator
- Separate timer possible to synchronize with main system timer
- Local interrupt controller
- RTA Task Manager - task scheduling and interrupt time stamp functionality
- Each RTA is isolated from the main GR716B processor ensuring timing independence

Key takeaways:

- An RTA can execute software in parallel with the main LEON3FT
- The RTA Task Manager (RTM) can initiate an RTA task routine following real-time events when the sequencer is idle.
- An RTA can access 16KiB of tightly coupled memory protected by EDAC to ensure single cycle instruction execution.
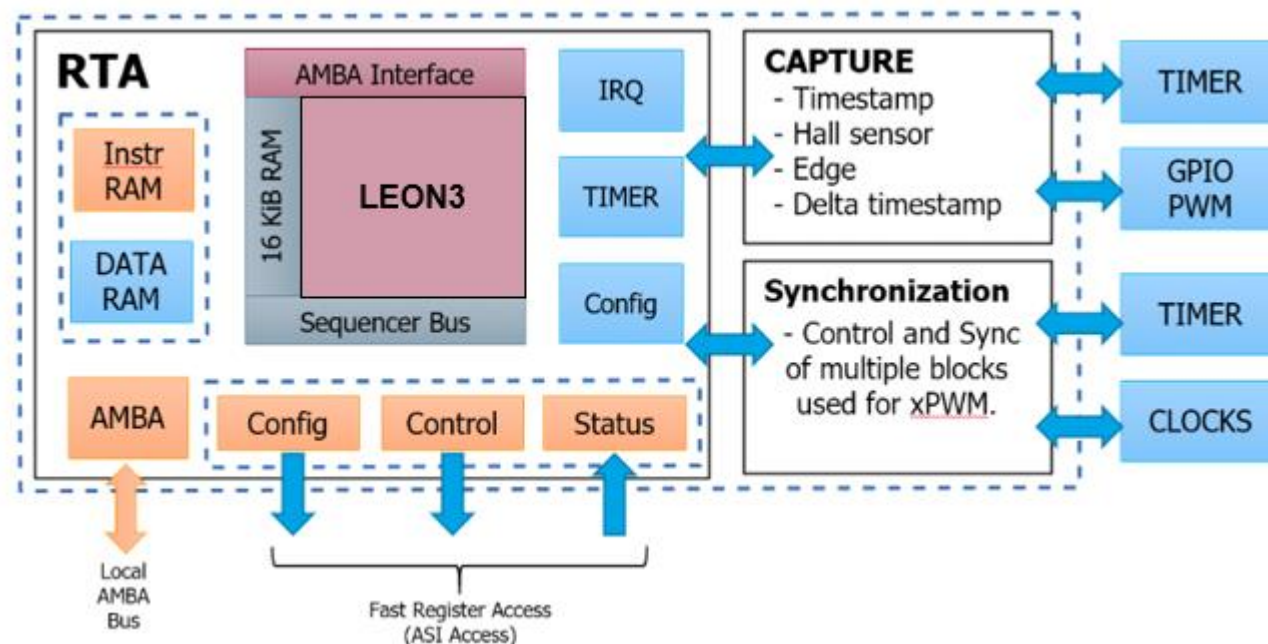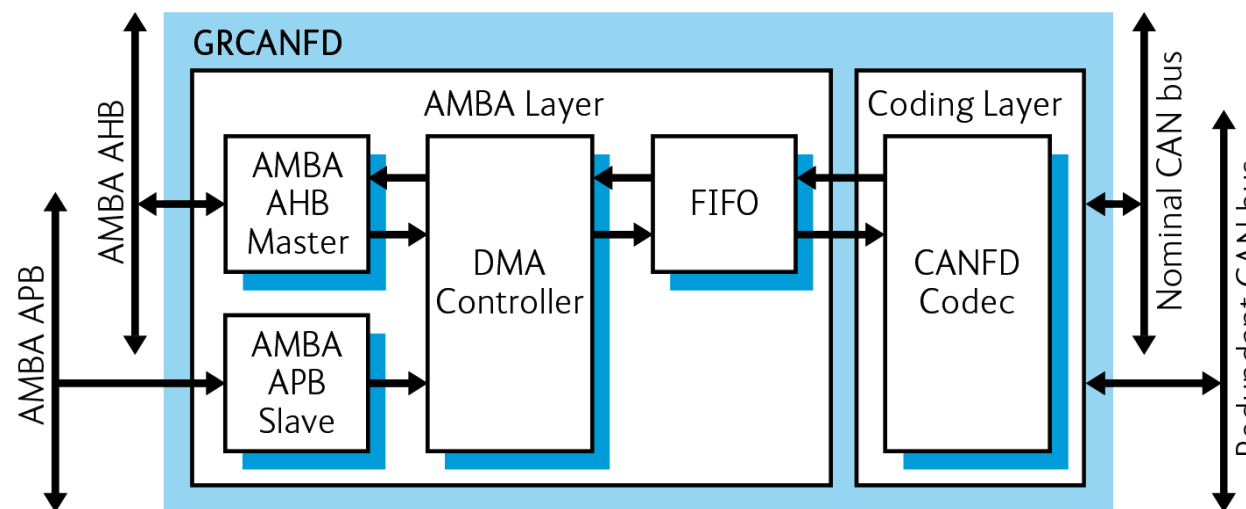
CAN controllers

GR716A
- 2x CAN 2.0 controllers each with access to nominal and redundant CAN bus
- Max bit rate: 1 Mbps

GR716B
- 1x CANFD controller with access to nominal and redundant CAN bus
- Supports CANOpen ECSS-E-ST-50-15C, Minimal Set Protocol
- Max bit rate: 8 Mbps

GR716B CANOpen functionalities:

- Answer PDO commands
  - Provide R/W access to on chip-bus
  - Enables processor boot via CAN
- Handle Heartbeat commands
  - If nominal bus is dead, switch automatically to redundant
- Handle SYNC commands
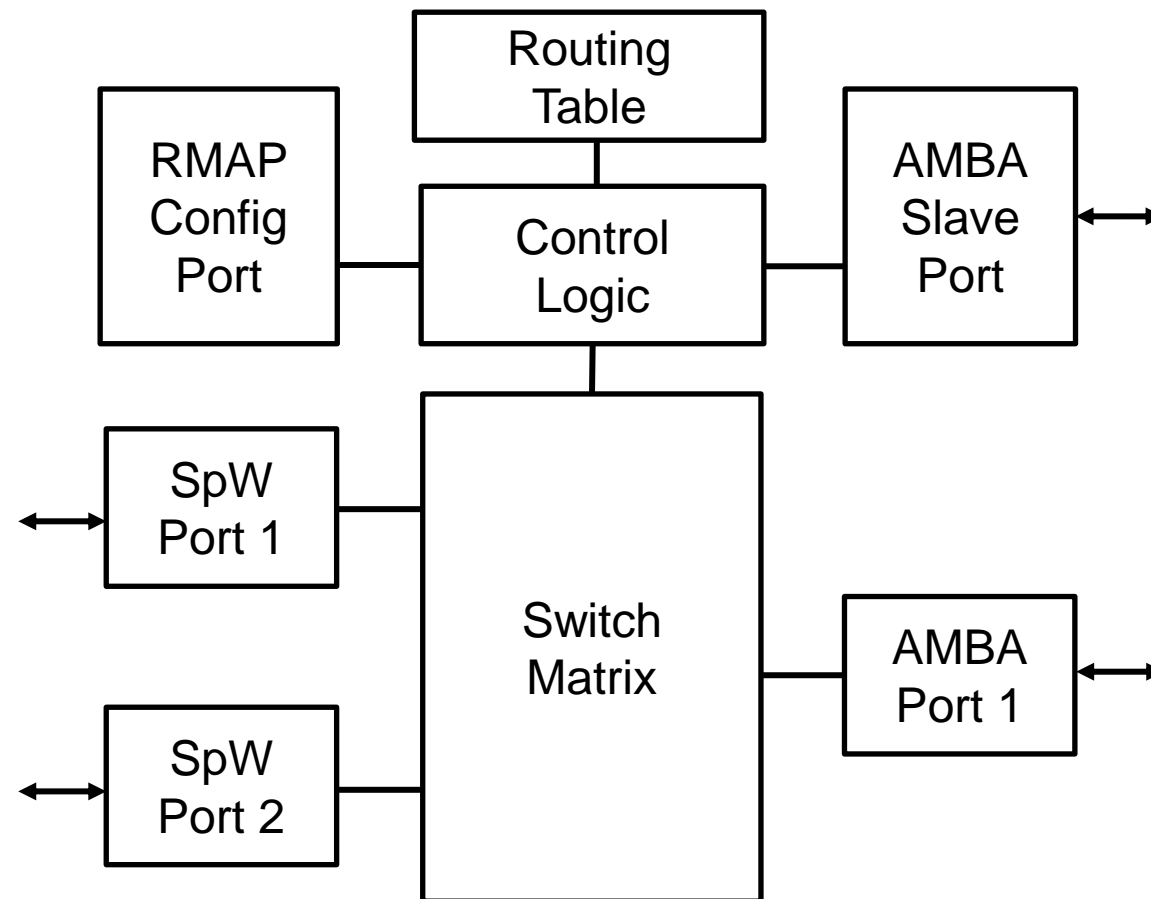 - Synchronize the slave nodes in a CAN bus

GR716A
- SpaceWire controller
- RMAP and time distribution support
- On-chip LVDS or CMOS interface

GR716B
- 2-port SpaceWire Router
- RMAP and Time Distribution Protocol support
- On-chip LVDS interface with cold-spare, fail-safe and extended common mode support

GR716B: FPGA Supervisor

The FPGA supervisor (GRSCRUB) is responsible for programming and scrubbing FPGA's configuration memory in order to prevent the accumulation of radiation-induced errors.

Baseline features

- Access target FPGA through the SelectMap (SMAP) interface

- FPGA programming

- Mapping of FPGA frame addresses

- Blind and readback scrubbing allows trade between speed and detection capability

- SEFI detection of the SelectMap interface of the target FPGA

  - allows restoring SMAP functionality after a SEFI

- Targets: Xilinx Kintex UltraScale and Virtex-5 FPGAs

- Periodic scrubbing with configurable delay between runs
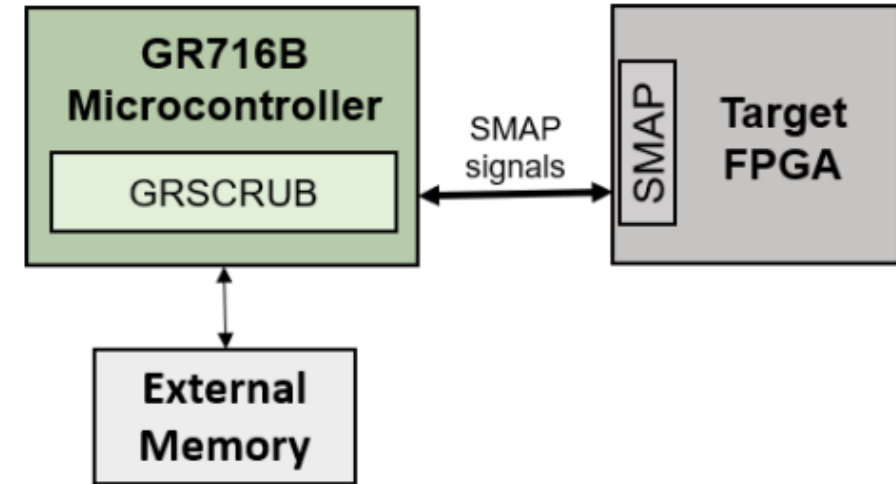
SEE testing
Validated by two proton test campaigns demonstrating that GRSCRUB considerably increases the radiation resilience of the Xilinx Kintex Ultrascale XCKU060

Availability
GRSCRUB is also available as an IP core part of the GRLIB VHDL Library

GRSCRUB validation under SEE testing

TEST SETUP

- **Protons testing:**
  - XCKU060 board: DUT SoC design based on NOEL-V processor with fault tolerance (FT). Design both with and without Triple Module Redundancy (TMR) was tested
  - Virtex5 board: SoC with GRSCRUB for programming and scrubbing the XCKU060.
- **GRSCRUB configuration for the setup:**
  - SelectMap frequency: 25 MHz
  - Data bus width: 8 bits
  - Full readback and SelectMap integrity check period: 6.7s

RESULTS

- **No need for FPGA reprogramming while using GRSCRUB during the test campaign**
  - SEFIs recovered using SoC reset only
- **GRSCRUB greatly improves the system's reliability:**
  - GRSCRUB reduces **10x** the error susceptibility compared to an unprotected SoC (FT)
  - The error susceptibility is reduced **81x** by combining the GRSCRUB with a triplicated SoC with distributed TMR (FT+TMR)

Orbital SEFI MTTF (Years)		
Orbit	FT	FT + DTMR
LEO	7.10	45.7
GEO	4.7	30.5

Analog Cores

Low Dropout Regulator (LDO)
- Enables Single 3.3V supply
- Can also supply other 1.8V loads on PCB

Power-on-Reset
Brownout Detection
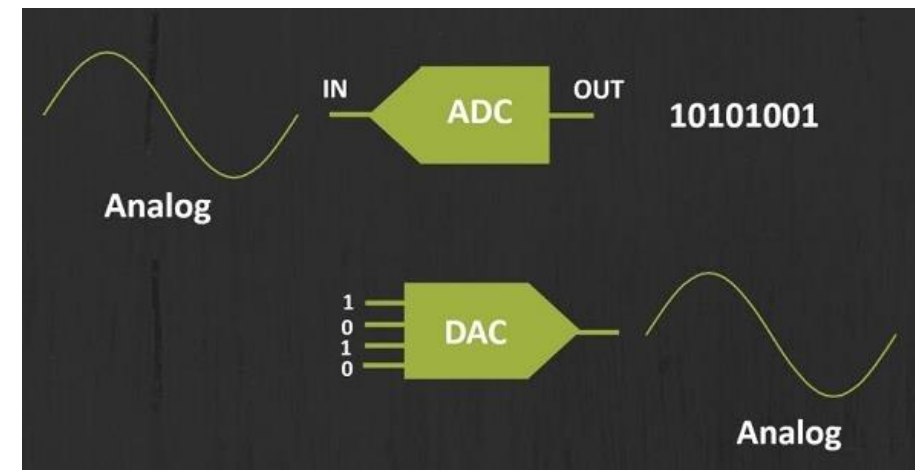## Temperature Sensor
PLL

ADC
- GR716A
    - 2x ADC 11bits resolution @ 200ksps
    - 4 Differential or 8 single-ended channels
- GR716B
    - 4x ADC 11bits/14bits @ 500Ksps
    - 8 differential or 16 single-ended channels

DAC
- GR716A
    - 12bit @ 3Msps analog DAC, 4 channels
- GR716B
    - 12bit @ 3Msps analog DAC, 4 channels
    - 24bit @ 25Msps PWM DAC, 8 channels

GR716B-only:
- Fast Analog Comparators
    - 20 channels, 25ns, 7 programmable internal comparison levels or external connection
- FIR filter
    - 8 channels, 25Msps, 27 binary programmable taps
    - Noise filtering for latch-up detection and other precise applications

- 4 independent DC/DC converters in peak-current control mode, or more in voltage control mode.
- Peak-current control mode, including overcurrent detection.
- Leading edge blanking (LEB) and max duty-cycle turn-off.
- 4 BLDC motors in PWM control mode, or 4 permanent magnet synchronous motors (PMSM), or 6 micro stepper motors
- Up to 4 analog channels with simultaneous sampling time point for optimum motor regulation.
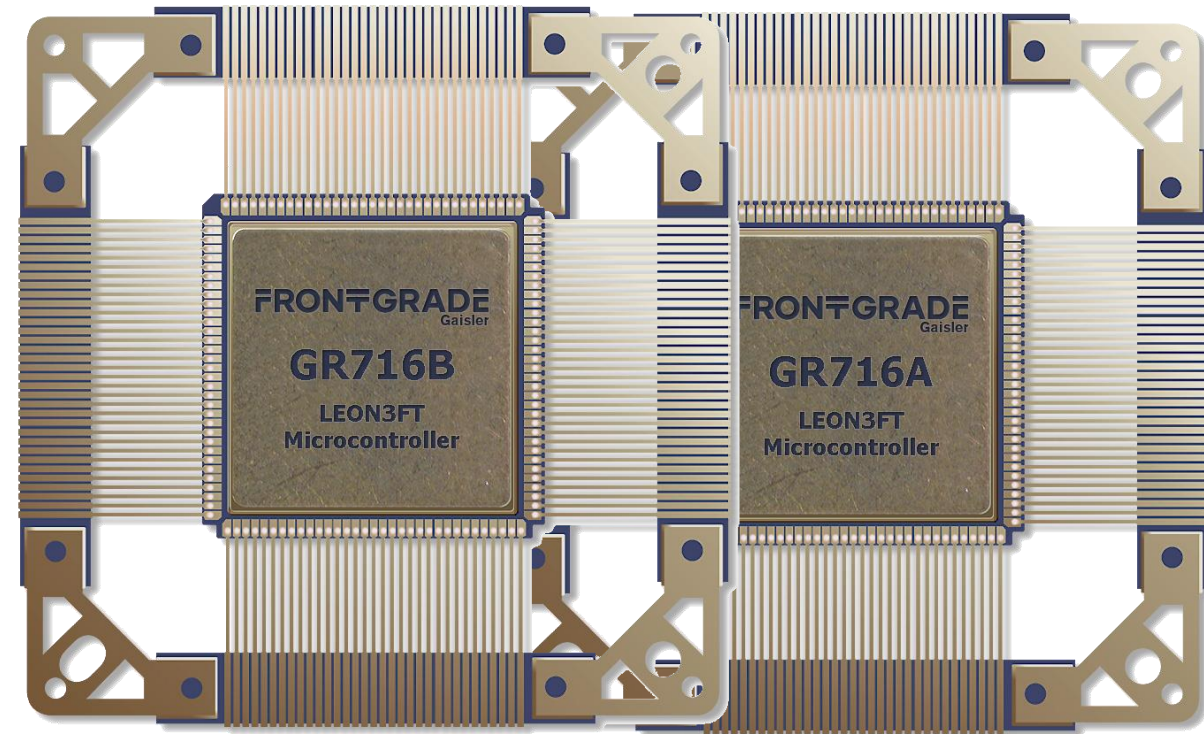
DC/DC Application: Step-Down Converter
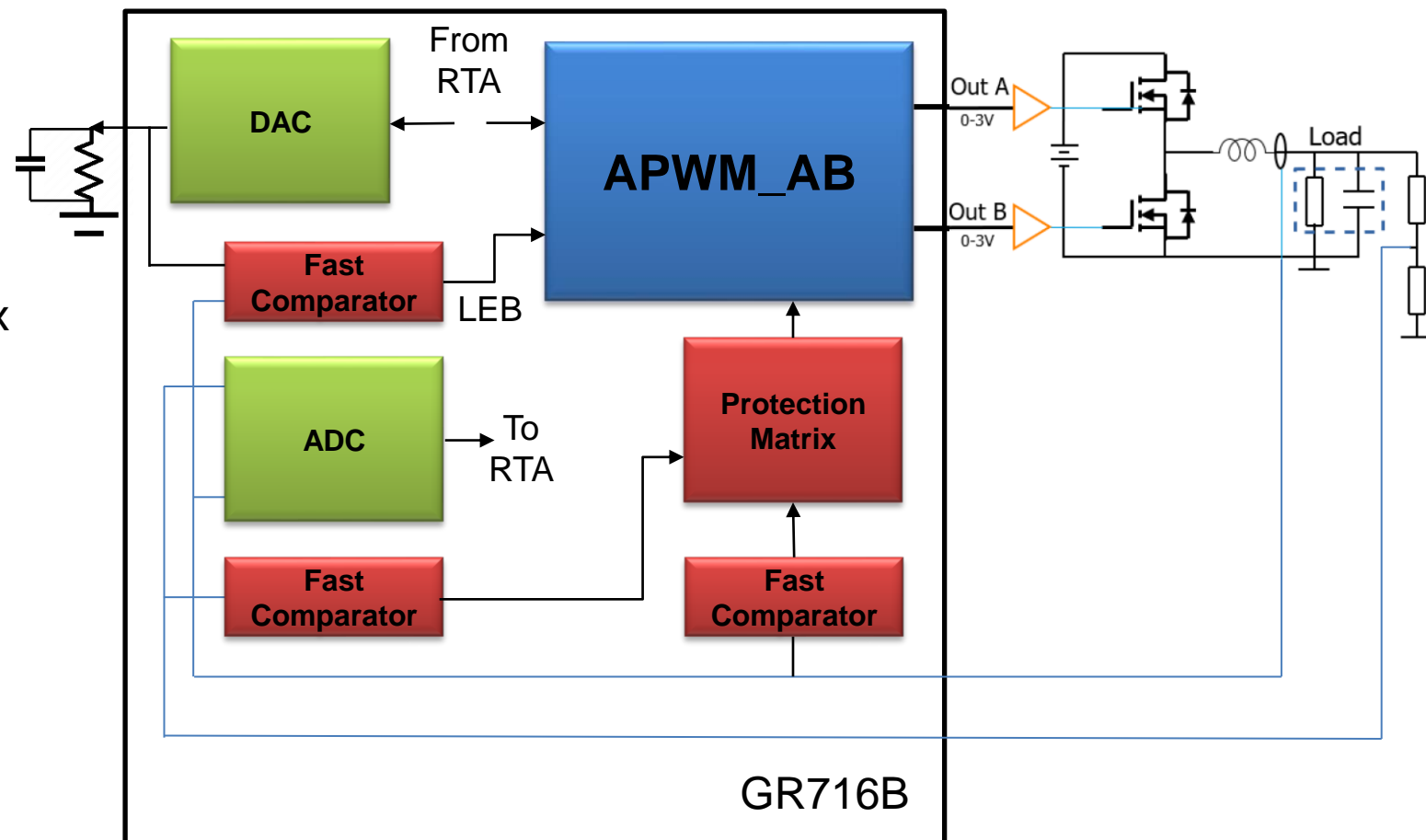
Conclusions

The GR716:

- LEON3FT Radiation-hardened microcontroller
- Includes support for mixed-signal functions
- Enables the usage of COTS FPGAs in space applications
- Has a wide range of interfaces, making it ideal for satellite supervision, monitoring and control
- Can support switching power and motor control applications
- GR716A flight parts available
- GR716B prototypes Q2 2024

Thank you for your attention!