FRONTGRADE Gaisler

GR765: SPARC and RISC-V Multiprocessor System-on-Chip

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2023-10-06

Agenda

01 Background: GR740

02 GR765 – next generation SoC

03 Test chip samples

04 Software

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GR740

LEON4FT Quad-core SoC

GR740 - Quad-Core LEON4FT Processor

Value proposition

- High performance, wide range of interfaces
- SPARC V8 compliant, **Rad**iation-hard and Fault Tolerant
- Designed as ESA's Next Generation Microprocessor, NGMP
- LEON Technology – re-use of Development and Software ecosystem
- Low risk, off-the-shelf product, QML Q/V
- Excellent performance/watt ratio
  - Very low power, < 3 W (core typical)
  - Performance 1700 DMIPS (1000 MIPS)

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	CHECKED BY Phu H. Nguyen			
	APPROVED BY Muhammad A. Akbar	MICROCIRCUIT, PROCESSOR, DIGITAL, CMOS, RADIATION HARDENED, QUAD CORE LEON4 SPARC V8 PROCESSOR, MONOLITHIC SILICON		
	DRAWING APPROVAL DATE 22-04-18			
	REVISION LEVEL	SIZE A	CAGE CODE 67268	**5962-21204**
		SHEET	1 OF 51	

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GR740 - Quad-Core LEON4FT Processor

What can be improved?

- **Higher-pin** count package enabling more interfaces simultaneously
  - No sacrifices needed
- Customers require:
  - Higher performance memory interface **(DDR3/4)**
  - **NAND Flash** memory controller for storage
  - **High Speed Serial Links**
  - Higher **processing performance**
- SBCs based on the GR740 typically require a **companion FPGA** to provide flexibility for custom interfaces and processing

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GR765

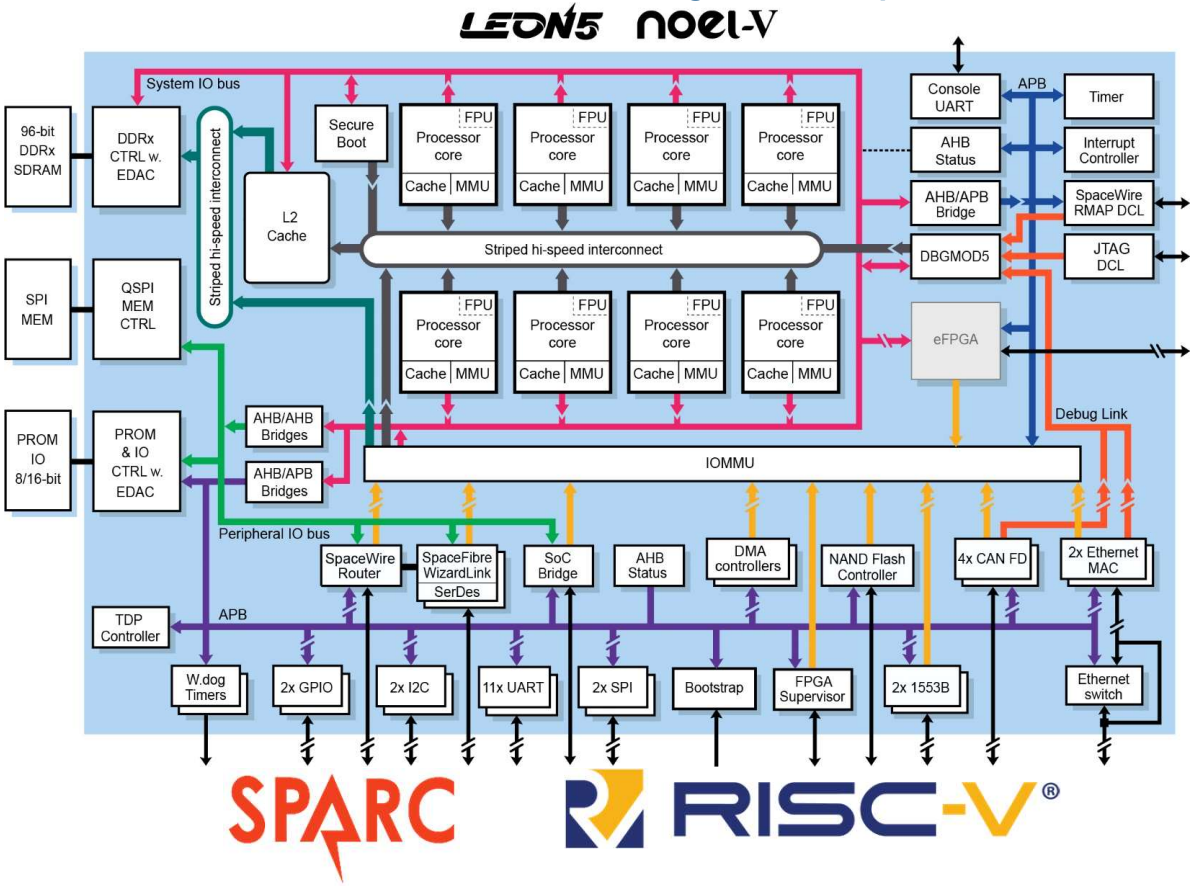
Next-Generation SoC

GR765 – Octa-Core Processor

Baseline Features

- Fault-tolerant **octa-core** architecture
  - **LEON5FT SPARC V8 or NOEL-V RV64GCH**
  - Dedicated FPU and MMU, 64 KiB per core L1 cache, connected via multi-port interconnect
- **1 GHz processor frequency - 26k DMIPS**
- 2+ MiB L2 cache, **512-bit** cache line, 4-ways
- **DMA controllers**
- **DDR2/3/4** interface with dual x8 device correction capability
- 8/16-bit PROM/IO interface
- **(Q)SPI and NAND** memory controller interfaces
- **Secure Element**, providing Secure (authenticated) boot (TBD)
- **eFPGA** ~30k LUT (TBD)
- High-pin count – **LGA1752** package allows reduction of pin sharing
- Target technology: **STM 28nm FDSOI**

In development
No guarantee of product launch



Instruction Set Architectures

Why RISC-V?

- Hardware and software potential for future space applications: A new class of processors requires a modern architecture
- Enabling new technologies by standardization
  - Hypervisor support
  - Vector extension, …
- Growing base of 3rd party ecosystem:
  - Toolsets
  - Libraries, engines etc.
- Attractive to talent entering the space domain
- Influx of know-how by talent entering the space domain

Why SPARC?

- Existing base of space proven HW and SW designs
- Mature ecosystem for today's space applications, e.g. qualified OS
- Accumulated development know-how in the industry
- Software backward compatible with existing LEON devices

GR765 provides RISC-V and SPARC

- Both architectures are needed by the industry
- Faster time-to-market for RISC-V while continuing SPARC – ease transition between the two architectures
- Minimal silicon overhead - sharing of resources on chip. User selects CPU (LEON5FT or NOEL-VFT), device cannot operate with both at the same time.

LEON5 – SPARC Processor

- **32-bit SPARC V8 processor** core
- **Multi-core support** (AMP & SMP)
- **Improved performance** over LEON3 & LEON4
  - In-order dual-issue pipeline
- **Improved fault tolerance (FT) from SEUs**
- **Improved FPU**: Floating Point Unit with denormalized number support
- **Leverage existing software:** maintain binary compatibility with LEON3 and LEON4

Performance:

- Coremark* : 4.52 CoreMark/MHz
  (-O3,-funroll-all-loops -finline-functions -finline-limit=1000)

* Results generated using BCC 2.0.7 toolchain

NOEL-V – RISC-V Processor

- **RISC-V processor core**
- 64-bit (RV64I) implementation in GR765
- Superscalar – in order pipeline
- Leverages RISC-V software and tool support in the commercial domain together with same level of software support provided by Gaisler as for the LEON line of processors

GR765 feature set:

- RISC-V **RV64GCH**
- Can run complex **OS**
- **OS-A** Embedded RISC-V platform specification
  - Set of features and default configurations that assures compatibility with rich-OS platforms

Performance:

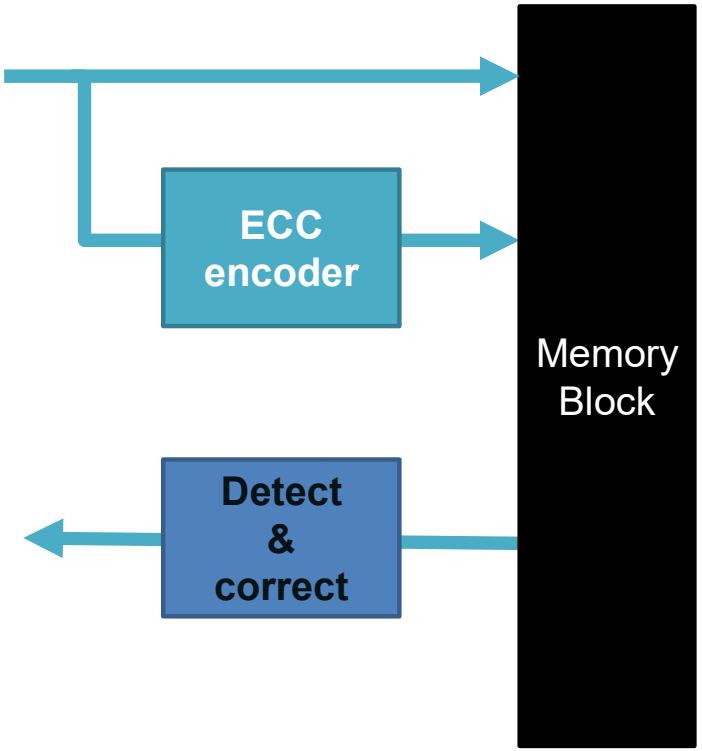
- Comparable to ARM Cortex A53
- CoreMark*/MHz: 4.41**

* GCC9.3.0 20200312 (RTEMS 5, RSB 5 (c53866c98fb2), Newlib 7947581
-g -march=rv64ima -mabi=lp64 -B /gsl/data/products/noelv/rtems-noel-1.0.3//kernel/riscv-rtems5/noel64ima/lib --specs bsp_specs -qrtems -lrtemsdefaultconfig -O2 -funroll-all-loops -funswitch-loops -fgcse-after-reload -fpredictive-commoning -mtune=sifive-7-series -finline-functions -fipa-cp-clone -falign-functions=8 -falign-loops=8 -falign-jumps=8 --param max-inline-insns-auto=20

** Using "#define ee_u32 int32_t" in core_portme.h, as is common for 64 bit RISC-V.

NOEL-V & LEON5 Fault tolerance overview

- No need for lock-step or redundant CPUs
- **Protection of memory blocks** (in caches & register file) using error correcting codes
- Protected with a full **SECDED** code with custom scheme:
  - Transparent single event correction
  - Guaranteed detection also of 3-bit and 4-bit adjacent bit errors
- **Hardware scrubber** built into the processor to avoid error build-up
  - Automatic scrubbing routines, minimized overhead
- **Error counters and diagnostic interfaces**
  - Monitor and inject errors



LEON5 & NOEL-V IP availability

- LEON5 and NOEL-V are available as part of the **GRLIB IP library**
- FPGA bitstreams for evaluation boards of multiple vendors (Xilinx, Lattice, Microchip,…)
- Debug monitor and software toolchains (Bare-C, RTEMS, Linux, …) are also freely available

www.gaisler.com

NOEL-ARTYA7

LEON-PF

NOEL-PF

LEON-XCKU

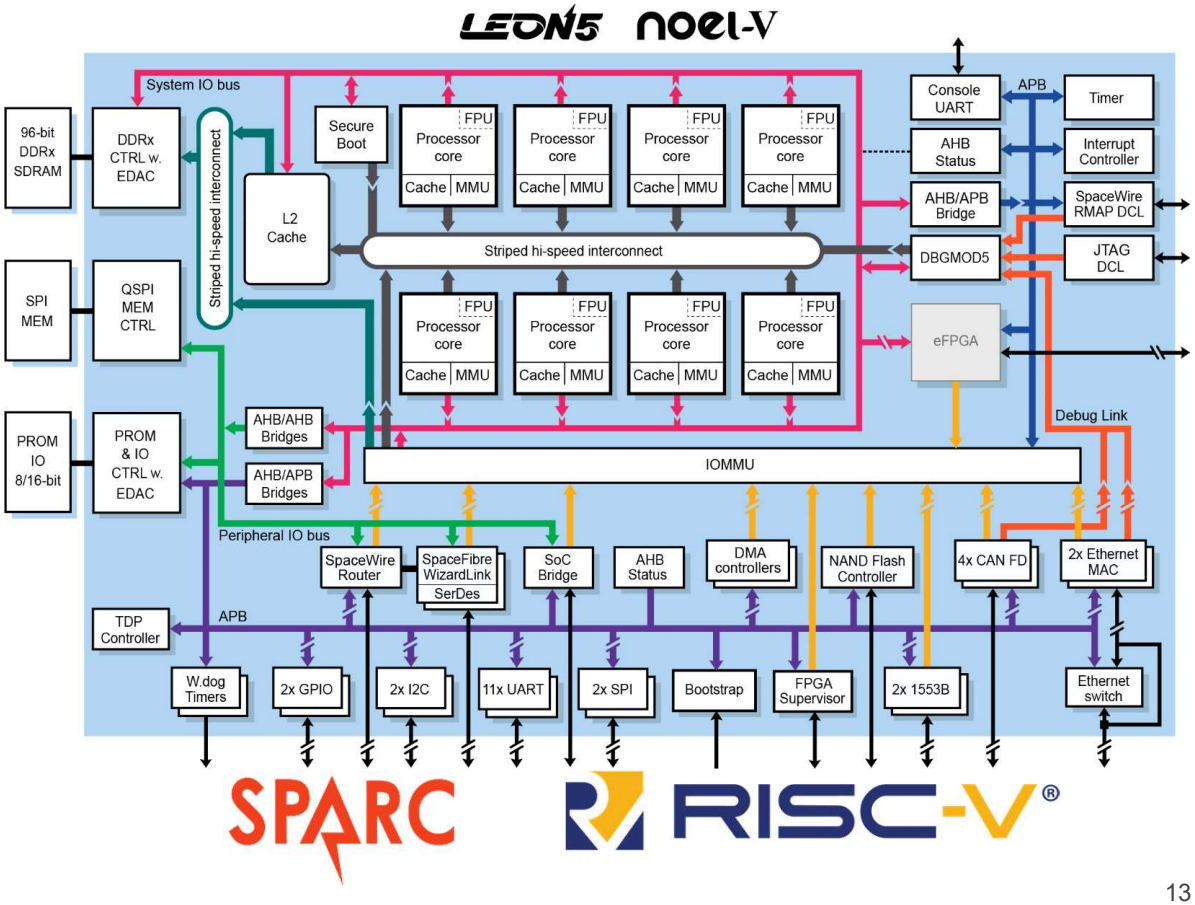
NOEL-XCKU

GR765 – Performance, Fault-Tolerance, and TSP

In development
No guarantee of product launch

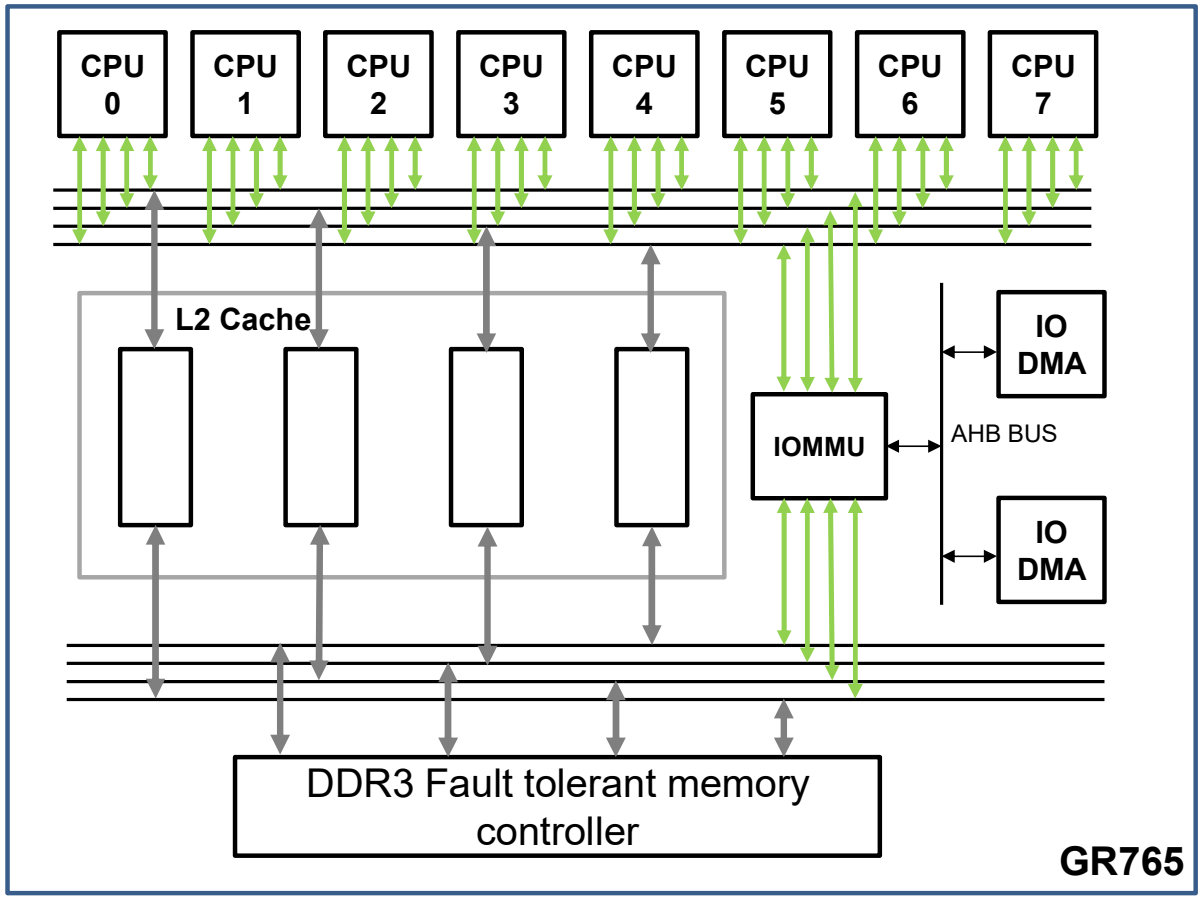
Improvements

- Higher performance and improved power consumption.
- **Fault-tolerance:** Processor L1 protected with a full SECDED code with custom scheme: Deliver correct data locally without causing memory access. Hardware scrubbers within processor pipeline, L1, L2 and DRAM controller.
- **Timing isolation features:** processors can use a subset of the multiple connections to Level-2 cache and memory controller.
- **Improved functional separation features**



GR765 – Improved interconnect

- **Striped interconnect**:
  - 4x AHB 2.0 buses
  - All cores connected to all stripes
  - Support for larger physical address space, up to 48-bits
- **Encoding to stripe based on (configurable) bits in physical address**
  - Default setting: map stripes to cache lines
    - line 0 -> stripe 0, line 1 -> stripe 1, …
  - Encoding to stripe address space in L1 cache backend
  - Achieve isolation by changing a stripe selection bit to a higher logical address bit
    - separate stripes 0-1 from 2-3
  - Consistent addressing from L1 backend to DDR controller
- **Fully isolated L2 cache pipelines dedicated to each stripe**

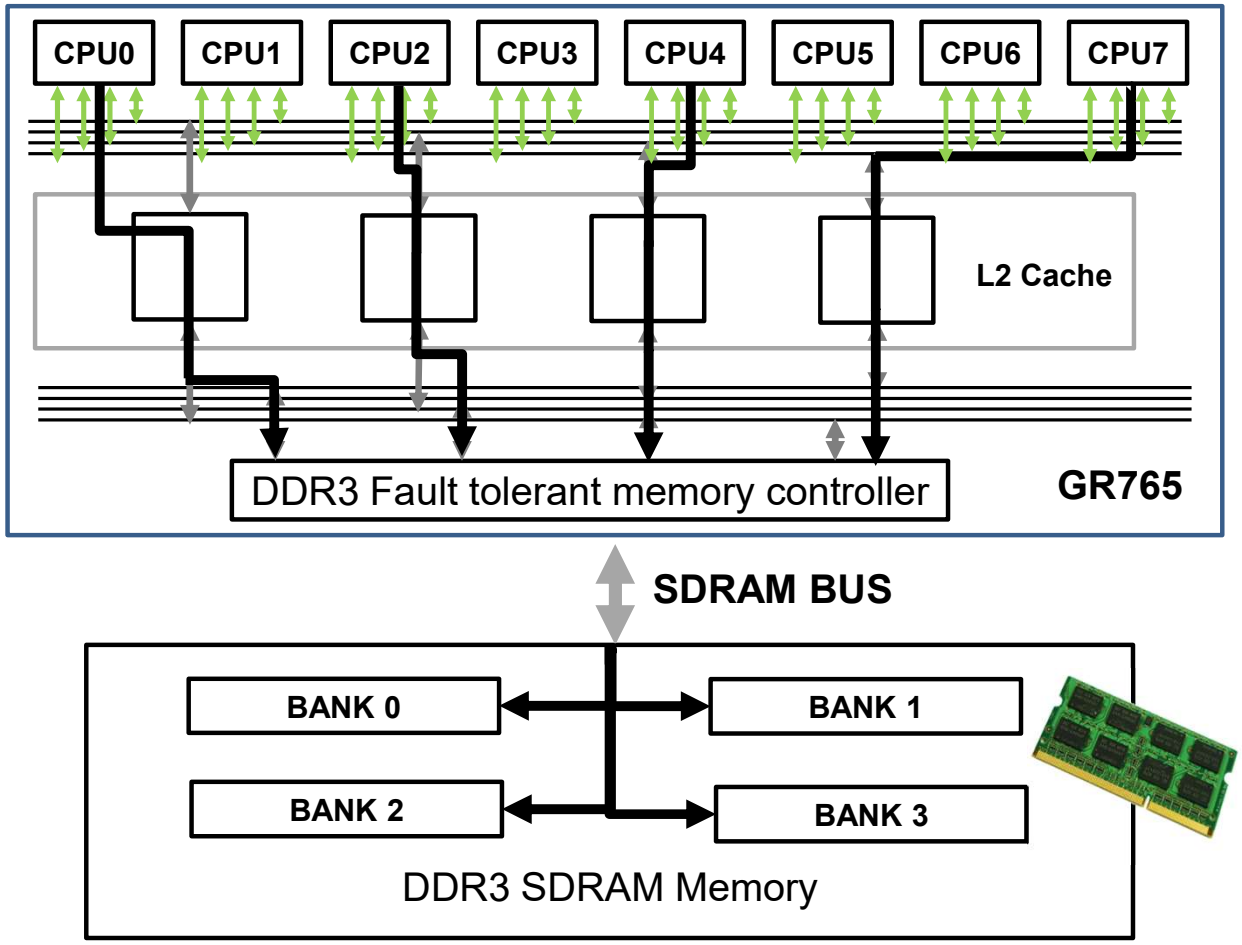


GR765 – Improved interconnect

The striped interconnect allows for concurrent accesses to different memory banks

- Minimizing interference
- Improving performance
- Maintaining L1 cache coherency

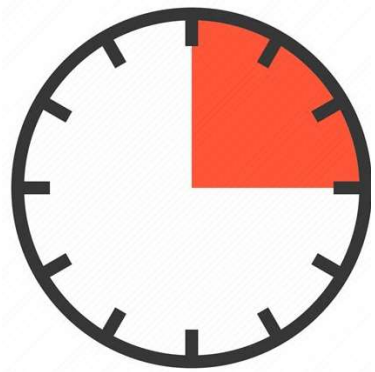
An L2 cache hit causes absolutely no interference!



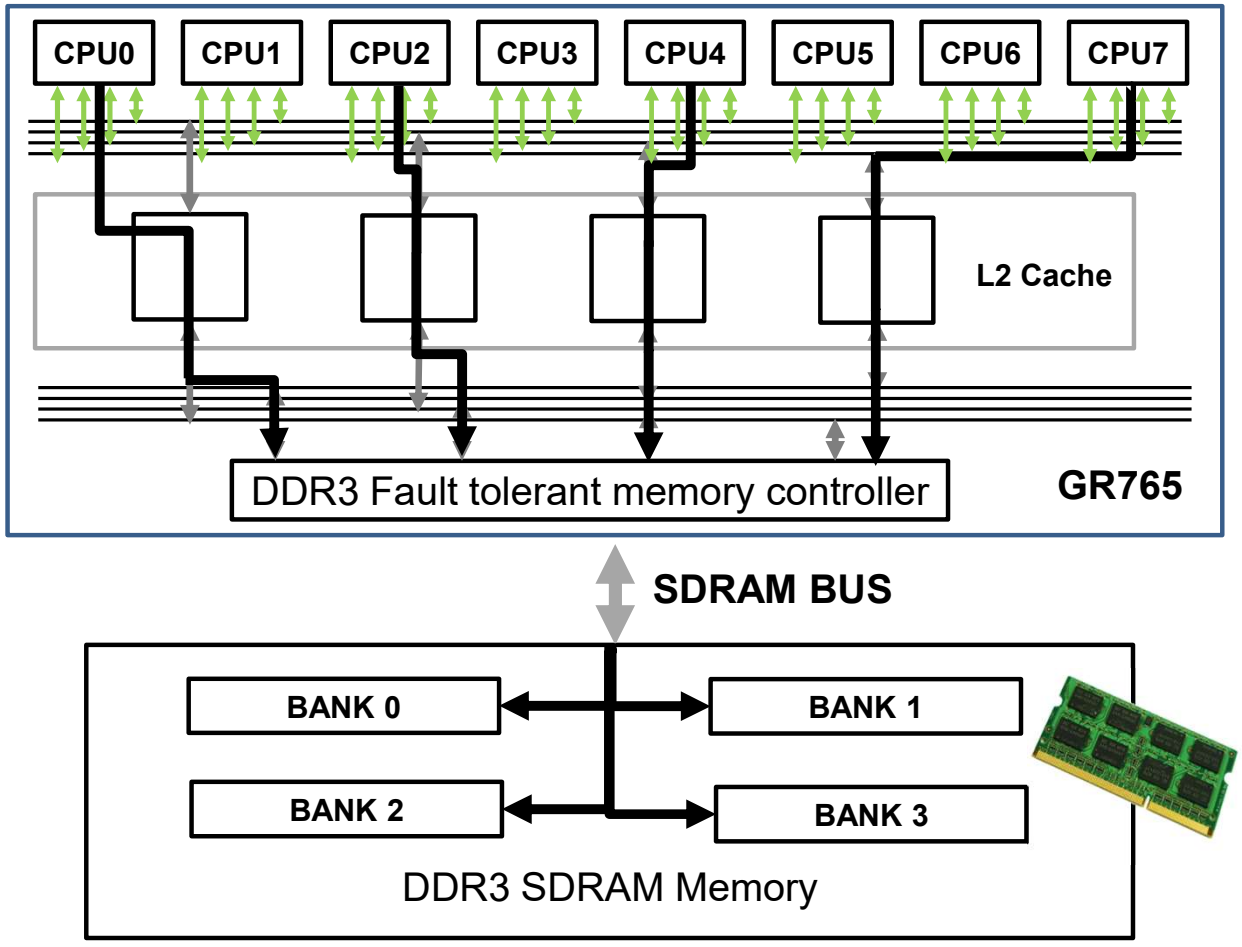
GR765 – Improved interconnect

Time-slotted mode:

- Accesses to each memory bank are only allowed 1/4 of the time
- Zero interference between the stripes
- Performance cost



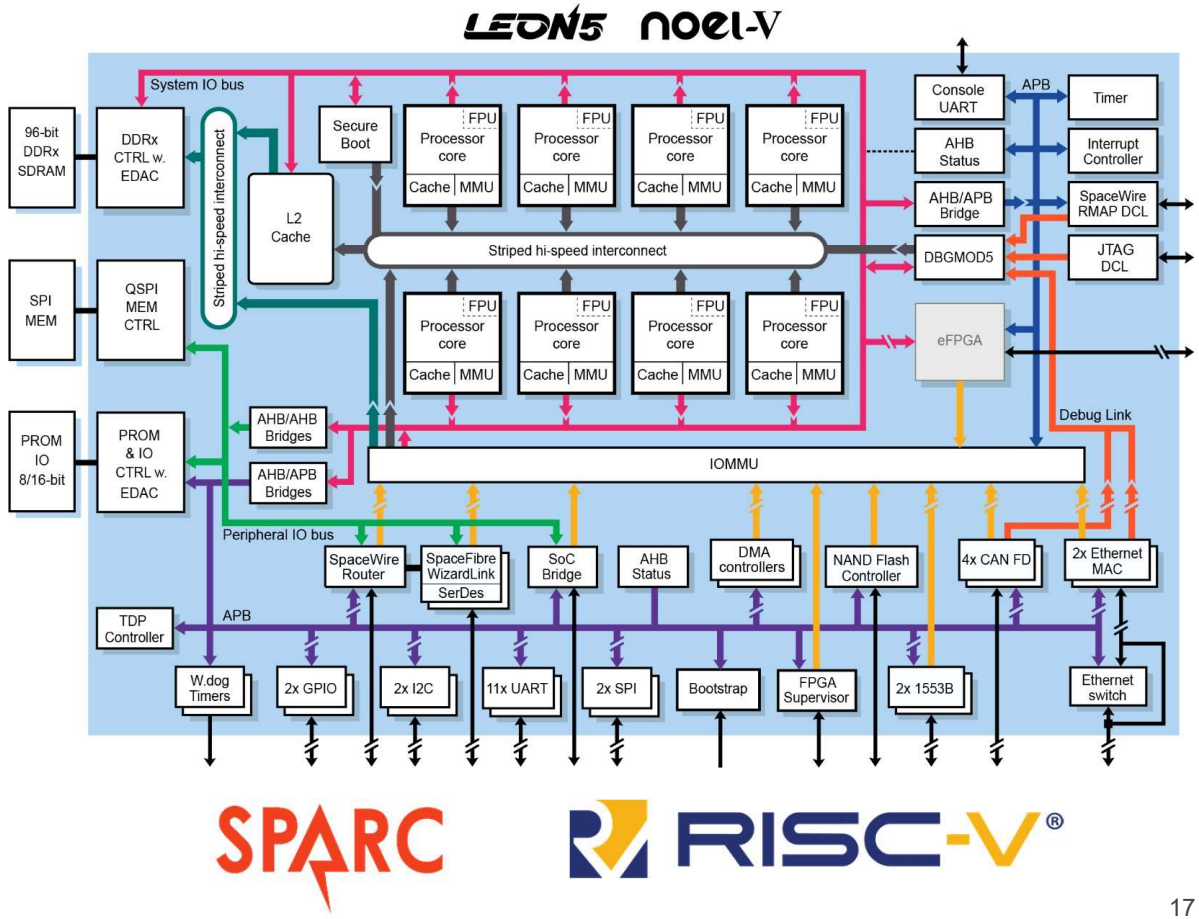
- …under development



GR765 – Functional separation

- **NOEL-V H extension + AIA + IOPMP/MMU**
  - Allows to group IO units together with guest VMs and to separate VMs+IO from each other.
  - Allows for HW distribution of interrupts to guests in hypervisor.
- **Same IOMMU implementation** for both SPARC and RISC-V modes
- **LEON5FT hypervisor mode** (in development)
- Evaluating use of an **additional layer of protection** (in addition to processor/IO MMU and PMP) to limit which devices are allowed to access memory-mapped interfaces.
- Additional layer may be necessary in at least LEON5 mode – and will in that case also be available in RISC-V mode.

In development
No guarantee of product launch

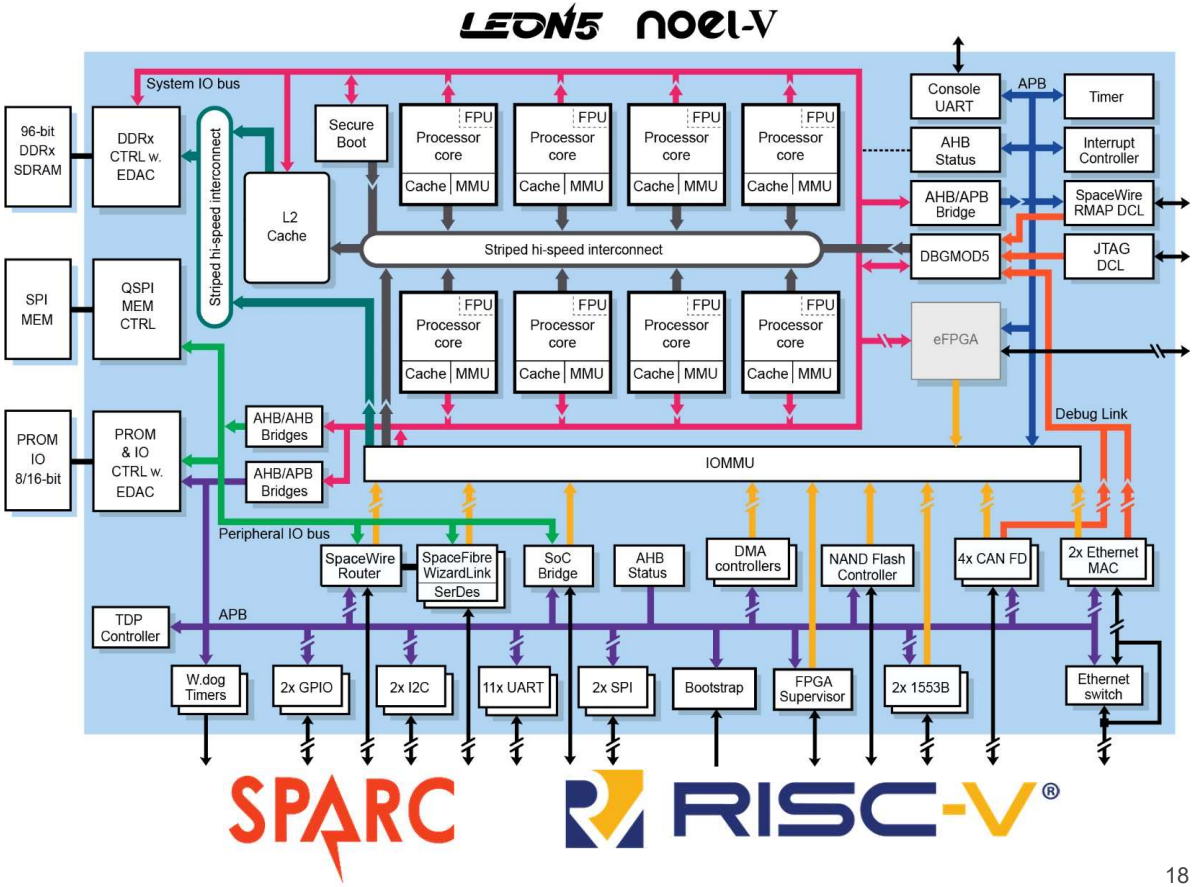


GR765 – Interfaces

Interfaces – SPARC and RISC-V mode

- **SpaceFibre x8 lanes 6.25 Gbit/s + WizardLink support**
- **12-port** SpaceWire router with +4 internal ports
- 2x 10/100/1000 Mbit Ethernet **w. TTEthernet capable switch**
- **2x** MIL-STD-1553B
- **4x CAN FD**
- **2x I2C interface, 12** x UART, **2x** SPI controller
- **SoC Bridge interface**
- **FPGA Supervisor interface**
- Timers & Watchdog, GPIO ports
- Debug links:
  - Dedicated: JTAG and SpaceWire
  - CAN, SpFi, Ethernet

In development
No guarantee of product launch

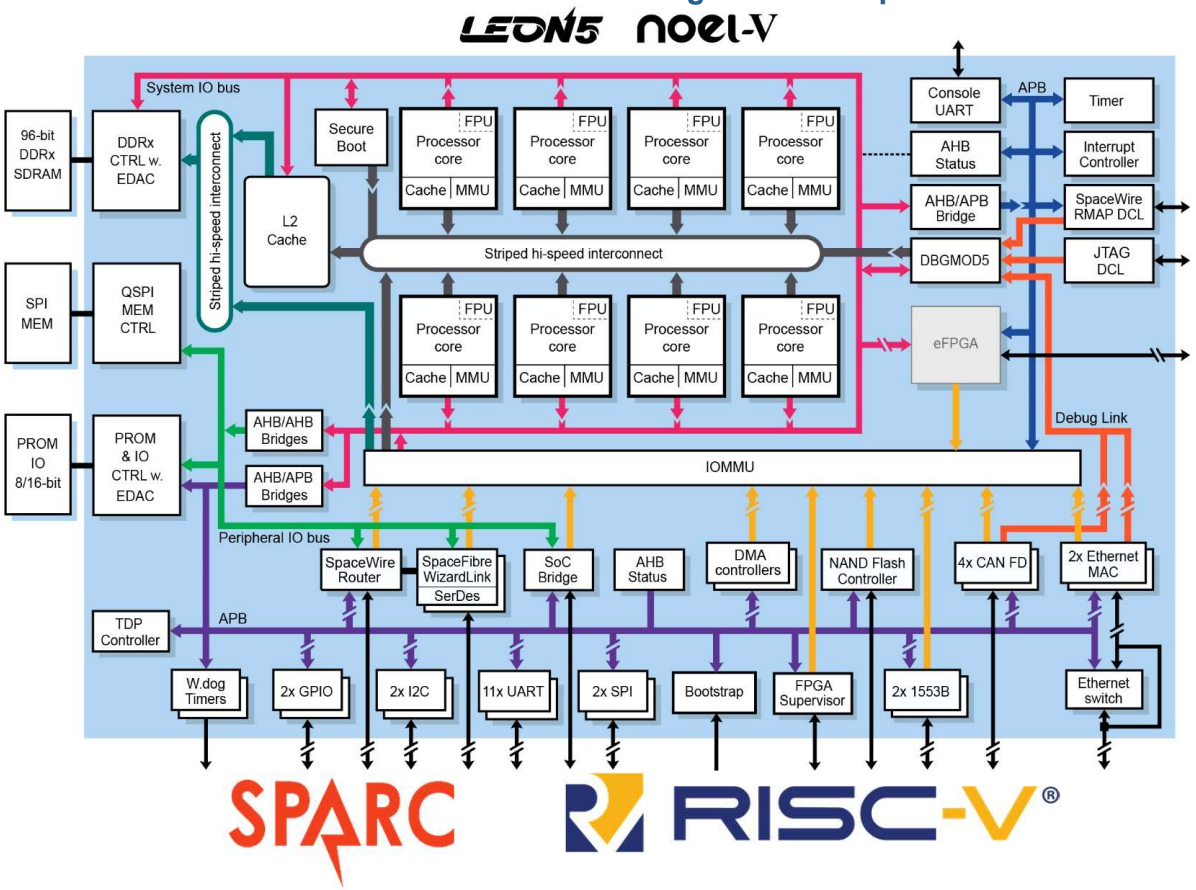


GR765 – Under evaluation

In development
No guarantee of product launch

Under evaluation

- eFPGA fabric
- Secure element
- NAND Flash NV-DDRx support and support for TLC
- Real-time instruction trace support
  - RISC-V E-Trace encoder implemented
  - evaluating Nexus
- DDR4 support



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LEON5FT and NOEL-V FT 28nm

Test Chip on STM FDSOI28 GEO P2

LEON5 and NOEL-V silicon proven on STM 28nm GEO P2

Rad-hard demonstrator with LEON5FT SPARC V8 32-bit processor and NOEL-V RISC-V 64-bit processor

- **ST 28nm FDSOI** GEO P2 technology
- Specialized design with LEON5 and NOEL-V **sharing resources**, consumes less than 1 mm^2
- Proves **implementation on target** technology
- Technology hardness and processor core fault tolerance features demonstrated through **SEE test campaign**
- Collaboration between STM and Gaisler R&D teams
- Manufactured using European supply chain, fab in Crolles (FR)

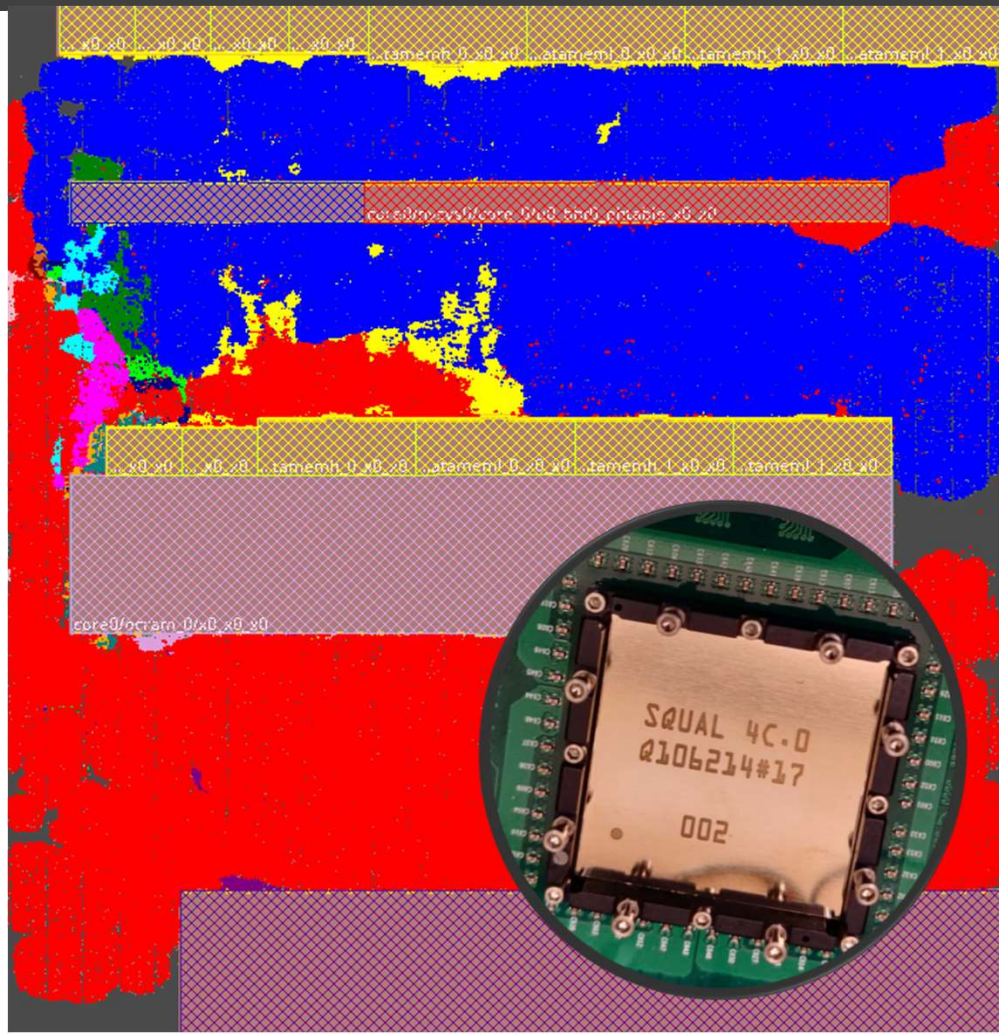
Performance attained

LEON5/NOEL-V:

- Typical corner: 1 GHz / 800* MHz
- Worst-case corner: 600 / 500* MHz

Schedule

- Test chips available at Gaisler
- Performed SEE characterization
- Test chip will be included in **GOMX-5** LEO in-orbit experiment



* Following this tape-out, NOEL-V has been further optimized and future implementations are expected to match LEON5 operating frequency.

SQUAL4C SEE results summary

Mean Time Between Events (MTBE)

Orbit**	Functional errors***
LEO (700 Km, incl. 98.7°)	28,500 years
GEO (36000 Km)	8,640 years

- Estimation from TRAD Omere 5.6
- LEO orbit refers to the GOMX-5 mission

* Not discarded that the events observed are actually test artifacts. Conservative approach taken, i.e., events treated as functional events

** AP8 solar min, Z=1-92, CREME96, Al shielding of 1 g/cm², SEE error rates due to protons not considered (due to the very low proton cross section per bit of the memories, the contribution of proton-induced functional events is less significant in majority of all space orbits)

*** An actual product can be expected to be 20x larger, and therefore the MTBE lower

Weibull parameter	Functional errors
W	6.56
S	0.93
Saturation XS	9.99E-8 cm²/device
LET threshold	7.64 MeVcm²/mg

Summary

- No silent data corruption
- Functional error saturation cross-section: 1E-7 cm²/device*
- All detected errors in memories were corrected by the fault-tolerant features of the design (on-chip RAM and L1 caches)
- No Single Event Latch-up (SEL)

Based on the results obtained, one can estimate the SEU tolerance for an actual product to be harder than the radiation-hardened GR740 SoC

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Software support

Next-Generation SoC

Software

- Complete ecosystem
- A combination of Gaisler and 3rd party software

Tool chains, Operating systems and compilers

- Bare-C
- Linux
- RTEMS
- VxWorks
- Zephyr

Hypervisors

- XtratuM/XNG (FentISS)
- PikeOS (SYSGO)
- Xvisor

Boot loaders

- MKPROM2
- GRBOOT Flight bootloader

Tools

- GRMON3
- TSIM3

ESA activity: GR765/LEON5 Software Ecosystem

- Started in March 2023
- TSIM Simulator extensions for GR765:
  - Same accuracy profile as for TSIM3-GR740
  - Focus on modelling new architecture:
    - LEON5 processor model with dual-issue
    - AHB stripes and L2-caches
    - DDR2/3 controller
  - GR765 TSIM configuration
- GRBOOT for GR765 (gaisler.com/grboot)
  - Flight boot loader software today available for GR740, GR712RC, UT700
  - Software architectural extensions for GR765
  - GR765 BSP and configuration
  - Other improvements also for GR740 and GR712RC
- GR765 Linux support
  - Analysis support for wider address space than 32-bit
  - Basic low-level drivers

(Other GR765 RISC-V/NOEL-V and LEON5 software support handled as part of other projects)

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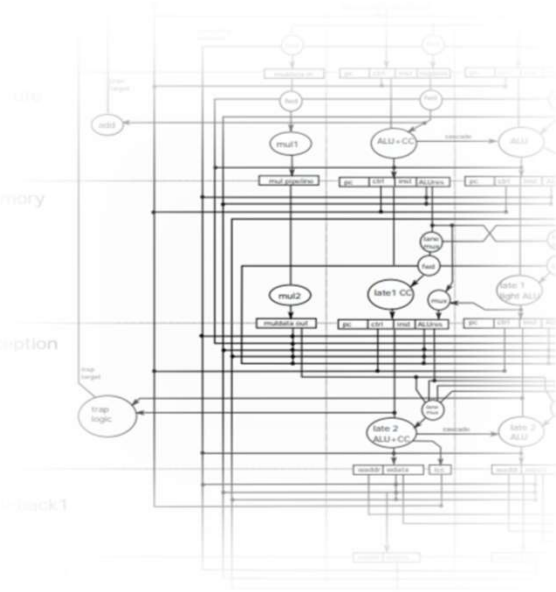
Conclusion

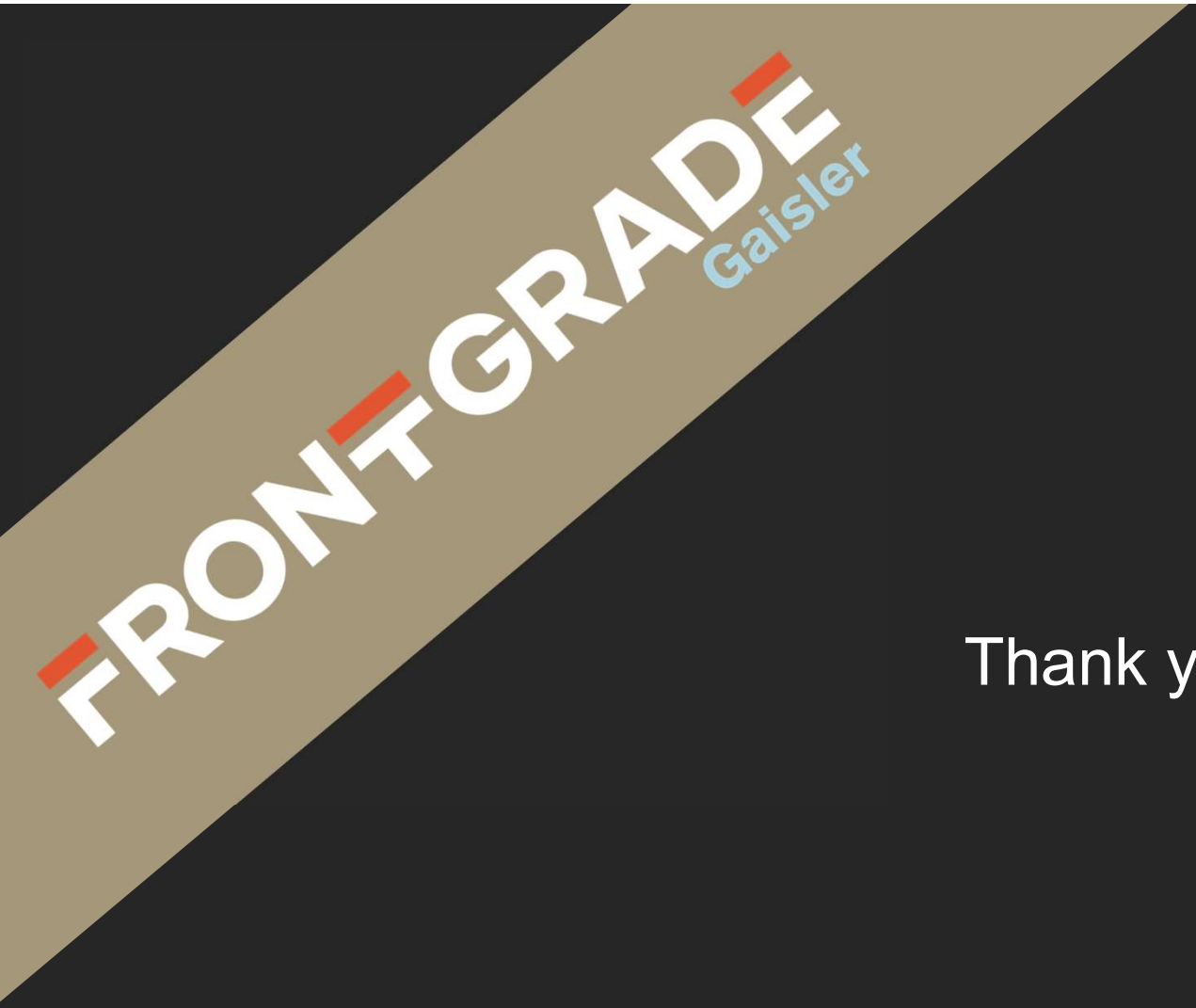
Next-Generation SoC

GR765 Conclusion

- The GR765 development builds on the successful GR740 quad-core LEON4FT component, adding numerous enhancements.
- The GR765 is an **octa-core** processor. Users can enable either eight **NOEL-VFT** RISC-V 64-bit processor cores or eight **LEON5FT** cores.
- GR765 supports **DDR2/3/4 SDRAM**, **high-speed serial link** controllers and several other extensions.
- GR765-XX (prototype) components in **2025**
- **FPGA bitfiles** to evaluate the GR765 available for GR-CPCIS-XCKU and GR-VPX-XCKU development boards
- The GR765 development puts emphasis on computational performance, power efficiency, and support for mixed criticality application.



Progress reported via www.gaisler.com/GR765



Thank you for your attention!